Triple, 6-Channel LCD Timing Delay-Locked Loop

AD8389

PRODUCT FEATURES

High speed
Up to 85 MHz clock rate
Triple (R, G, B) output
Matched delay lines
Low power dissipation: 40 mW
Reference to rising or falling edge of MONITI input
Selectable loop delay
Available in 48-lead 7 mm × 7 mm LFCSP

APPLICATIONS

LCD microdisplay horizontal timing

PRODUCT DESCRIPTION

The AD8389 is a triple 6-channel LCD microdisplay delay-locked timing loop. As part of a closed-loop system, the AD8389 maintains a constant delay between the common input, DXI, and each independent feedback reference, MONITxI.

The AD8389 consists of a selectable fixed delay element, a phase detector, a charge pump, and six matched variable delay lines per color. The phase detector, charge pump, and master delay line form a closed loop when connected to a compatible LCD microdisplay. Five additional delay lines track the master for a complete set of matched timing signals.

The AD8389 dissipates 40 mW nominal power. The AD8389 is offered in a 48-lead 7 mm × 7 mm LFCSP package and operates over the commercial temperature range of 0°C to 85°C.

FUNCTIONAL BLOCK DIAGRAM

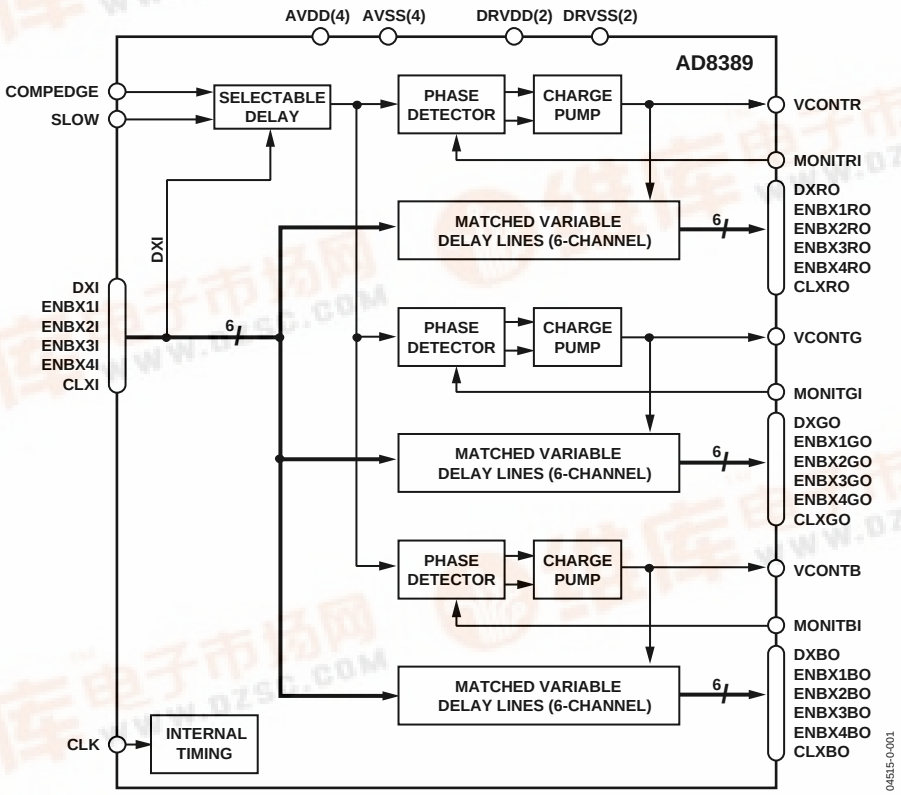

Figure 1.

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REVISION HISTORY

Revision 0: Initial Version

SPECIFICATIONS

Table 1. @ 25°C, AVDD = DRVDD = 3.3 V, T_{MIN} = 0°C, T_{MAX} = 85°C, unless otherwise noted

Parameter	Conditions	Min	Typ	Max	Unit
LOGIC INPUTS					
C_{IN}					pF
I_{IN}		−2		+2	µA
V_{IH}		2.0		AVDD	V
V_{IL}		AGND		0.8	V
V_{TH}			1.5		V
OUTPUTS					
V_{OH}	I_O = −2 µA	DRVDD − 0.4			V
V_{OL}	I_O = +2 µA			DVRSS + 0.4	V
TIMING SPECIFICATIONS					
Operating Frequency					
CLK, f_{CLK}		60	75	85	MHz
CLXI, ENBX(1–4)I				$(2t_1)^{-1}$	Hz
DXI, MONITxI				$(2t_1)^{-1}$	Hz
Input Low Pulse Width, t_1—All Inputs except CLK					
DXI, MONITxI		280			ns
ENBX(1–4)I, CLXI	$t_5 \leq$ 230ns	30			ns
CLK High Pulse Width, t_2		4.7			ns
CLK Low Pulse Width, t_3		4.7			ns
CLK to DXI Setup Time, t_4		2			ns
Output Rise, Fall Times—t_r, t_f	C_L = 30 pF			5	ns
Delay t_5	DXI to DXxO	22		350	ns
Output Skew, t_6	C_L = 30 pF				
$t_5 \leq$ 130 ns			0.3	2.5	ns
$t_5 \leq$ 170ns			0.45	3.4	ns
$t_5 \leq$ 230ns			0.7	5	ns
Loop Delay, t_7					
COMPEDGE = H, SLOW = H			$9/(f_{CLK}) + t_4$		ns
COMPEDGE = H, SLOW = L			$15/(f_{CLK}) + t_4$		ns
COMPEDGE = L, SLOW = H			$26/(f_{CLK}) + t_4$		ns
COMPEDGE = L, SLOW = L			$32/(f_{CLK}) + t_4$		ns
POWER SUPPLIES					
AVDD Operating Range		3		3.6	V
DRVDD Operating Range		3		3.6	V
Total Operating Current	f_{CLK} = 75 MHz, C_L = 30 pF		11		mA
Power Dissipation	f_{CLK} = 75 MHz, C_L = 30 pF		40		mW
Operating Temperature		0		85	℃

ABSOLUTE MAXIMUM RATINGS

Table 2. AD8389 Stress Ratings[1]

Parameter	Rating
Supply Voltages	
AVDDx – AVSSx	3.9 V
DRVDDx – DRVSSx	3.9 V
Input Voltages	
Maximum Digital Input Voltage	AVDD + 0.3 V
Minimum Digital Input Voltage	AVSS – 0.3 V
Internal Power Dissipation[2]	
LFCSP Package @ T_A = 25°C	4.8 W
Operating Temperature Range	0°C to 85°C
Storage Temperature Range	–65°C to +125°C
Lead Temperature Range (Soldering 10 sec)	300°C

[1] Stresses above those listed under the Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum ratings for extended periods may reduce device reliability.

[2] 48-Lead LFCSP Package:
θ_{JA} = 26°C/W (JEDEC Standard 4-layer PCB in still air)
θ_{JC} = 20°C/W

EXPOSED PADDLE

To ensure high reliability, the exposed paddle must be soldered to GND.

MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the AD8389 is limited by its junction temperature. The maximum safe junction temperature for plastic encapsulated devices as determined by the glass transition temperature of the plastic is approximately 150°C. Exceeding this limit temporarily may cause a shift in the parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of 175°C for an extended period can result in device failure.

To ensure operation within the specified operating temperature range, it is necessary to limit the maximum power dissipation as follows:

$$P_{DMAX} = (T_{JMAX} - T_A)/\theta_{JA}$$

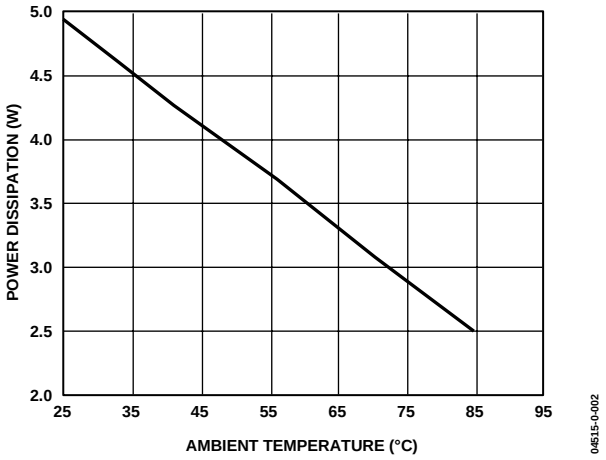


Figure 2. Maximum Power Dissipation vs. Ambient Temperature

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

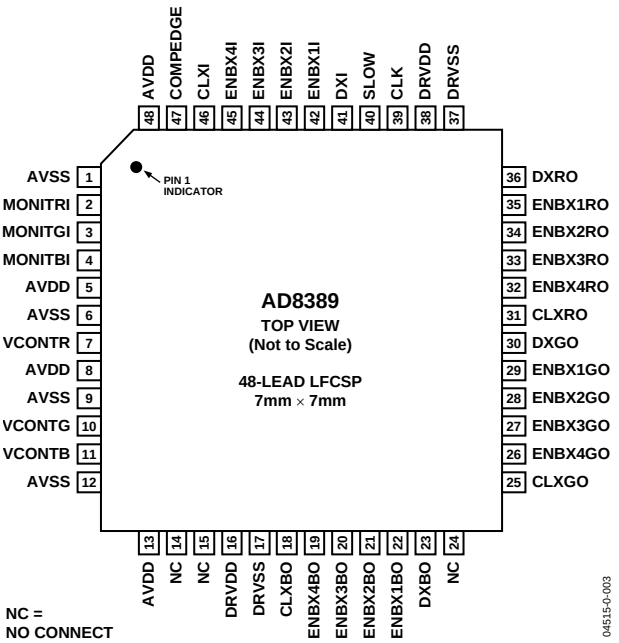


Figure 3. 48-Lead LFCSP, 7 mm × 7 mm Pin Configuration

Table 3. Pin Function Descriptions

Mnemonic	Function	Description
AVDD, DRVDD	Power Supply	Power Supply.
AVSS, DRVSS	Ground	Ground.
CLK	Clock	Clock Input. Active edge is the rising edge.
COMPEDGE	Edge Select	When set HIGH, the phase detector compares the falling edge of DXIN with the rising edge of MONITxI. When set LOW, the phase detector compares the rising edge of DXIN with the falling edge of MONITxI.
SLOW	Delay Select	When set HIGH and COMPEDGE = HIGH, the delay between the falling edges of DXI and the rising edges of MONITI is maintained at $9/(f_{CLK}) + t_4$. The delay is maintained at $26/(f_{CLK}) + t_4$ when COMPEDGE = LOW. When set LOW and COMPEDGE = HIGH, the delay between the falling edges of DXI and the rising edges of MONITI is maintained at $15/(f_{CLK}) + t_4$. The delay is maintained at $32/(f_{CLK}) + t_4$ with COMPEDGE = LOW.
DXI	Reference Input	LCD Timing Input from the Image Processor. Used as the input to all phase detectors.
CLXI	Input	LCD Timing Input from the Image Processor.
ENBX(1–4)I	Inputs	LCD Timing Inputs from the Image Processor.
MONITxI	Feedback Inputs	Inputs from the LCD. Used as the feedback input to each phase detector. When the AD8389 forms part of a closed loop, it maintains a constant delay between the DXI input and this reference input pin.
DXxO	Delayed Outputs	
CLXxO	Delayed Outputs	
ENBX(1–4)xO	Delayed Outputs	
VCONTx	Control Voltage	200 pF capacitors connected between these pins and the AVSS plane are required for proper operation of the internal charge pump.

TIMING

Table 4. Timing Specifications

Parameter	Conditions	Min	Typ	Max	Unit
Operating Frequency					
CLK, f_{CLK}		60	75	85	MHz
CLXI, ENBX(1–4)I				$(2t_1)^{-1}$	Hz
DXI, MONITxI				$(2t_1)^{-1}$	Hz
Input Low Pulse Width, t_1—All Inputs except CLK					
DXI, MONITxI		280			ns
ENBX(1–4)I, CLXI	$t_5 \leq 230$ns	30			ns
CLK High Pulse Width—t_2		4.7			ns
CLK Low Pulse Width—t_3		4.7			ns
CLK to DXI Setup Time—t_4		2			ns
Output Rise, Fall Time—tr, tf	C_L = 30 pF			5	ns
Delay—t_5	DXI to DXxO	22		350	ns
Output Skew— t_6	C_L = 30 pF				
$t_5 \leq 130$ ns			0.3	2.5	ns
$t_5 \leq 170$ns			0.45	3.4	ns
$t_5 \leq 230$ns			0.7	5	ns
Loop Delay, t_7					
COMPEDGE = H, SLOW = H			$9/(f_{CLK}) + t_4$		ns
COMPEDGE = H, SLOW = L			$15/(f_{CLK}) + t_4$		ns
COMPEDGE = L, SLOW = H			$26/(f_{CLK}) + t_4$		ns
COMPEDGE = L, SLOW = L			$32/(f_{CLK}) + t_4$		ns

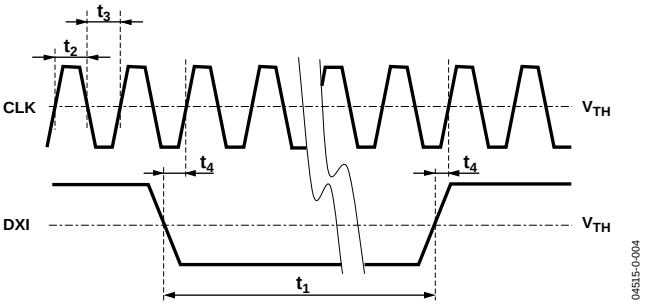


Figure 4. CLK and DXI Timing

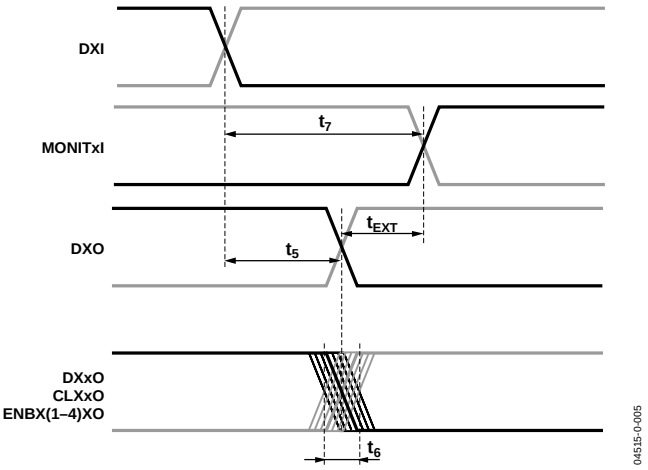


Figure 5. Input and Output Waveforms at COMPEDGE = HIGH

OPERATING PRINCIPLES

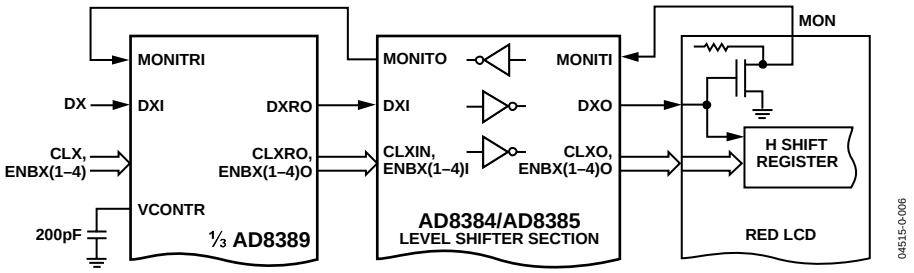


Figure 6. AD8389 Application in the Red Channel of an LCD Projection System

The image quality of an LCD system is dependent on the timing relationship between the control inputs, DX, CLX, ENBX(1–4), and the video channels.

TFT delay and switching speed variations, due to temperature variations and LCD aging, degrade image quality if not compensated.

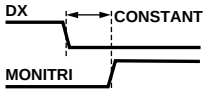
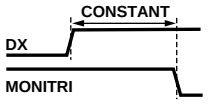
An internal reference TFT connected to an internal pull-up resistor, as shown in Figure 6, characterizes the internal S/H TFTs of the LCD and monitors switching speed and delay variations due to aging and temperature. When the MON output of an LCD that includes such an internal reference TFT is connected to the reference input of the AD8389 delay-locked timing loop, continuously optimized timing of the LCD is maintained automatically.

OPERATION

As part of a closed loop, the AD8389 maintains a constant delay between the common input, DXI, and each independent feedback reference, MONITxI. The block diagram of such closed-loop system is shown in Figure 6.

A constant delay, t_7, selected via the COMPEDGE and SLOW control inputs, is applied to the DXI input to approximate the nominal, initially expected total delay, t_7, through the level shifters and the LCD as shown in Table 5.

Table 5

COMPEDGE	SLOW	Constant Delay	
1	0	$15/f_{CLK} + t_4$	
1	1	$9/f_{CLK} + t_4$	
0	0	$32/f_{CLK} + t_4$	
0	1	$26/f_{CLK} + t_4$	

The phase detector compares the delayed DX and MONITxI reference inputs and automatically adjusts the variable delay (t_5), maintaining the constant delay (t_7) between the active edges of DX and MONITxI. Five matched delay lines maintain the phase relationship between DXxO, CLXxO, and ENBX(1–4)xO.

When the loop is locked, $t_7 = t_5 + t_{EXT}$, where t_{EXT} is the total delay through the level shifter and the LCD.

The external delay of a typical system is the sum of the level shifter delay (20 ns typical) and the LCD delay, (typically in the range of 20 ns to 120 ns). At a 75 MHz operating clock frequency, the maximum expected total delay of 140 ns is equal to 10.5 clock cycles, requiring COMPEDGE = 1, SLOW = 0 for systems using negative active edge for DX.

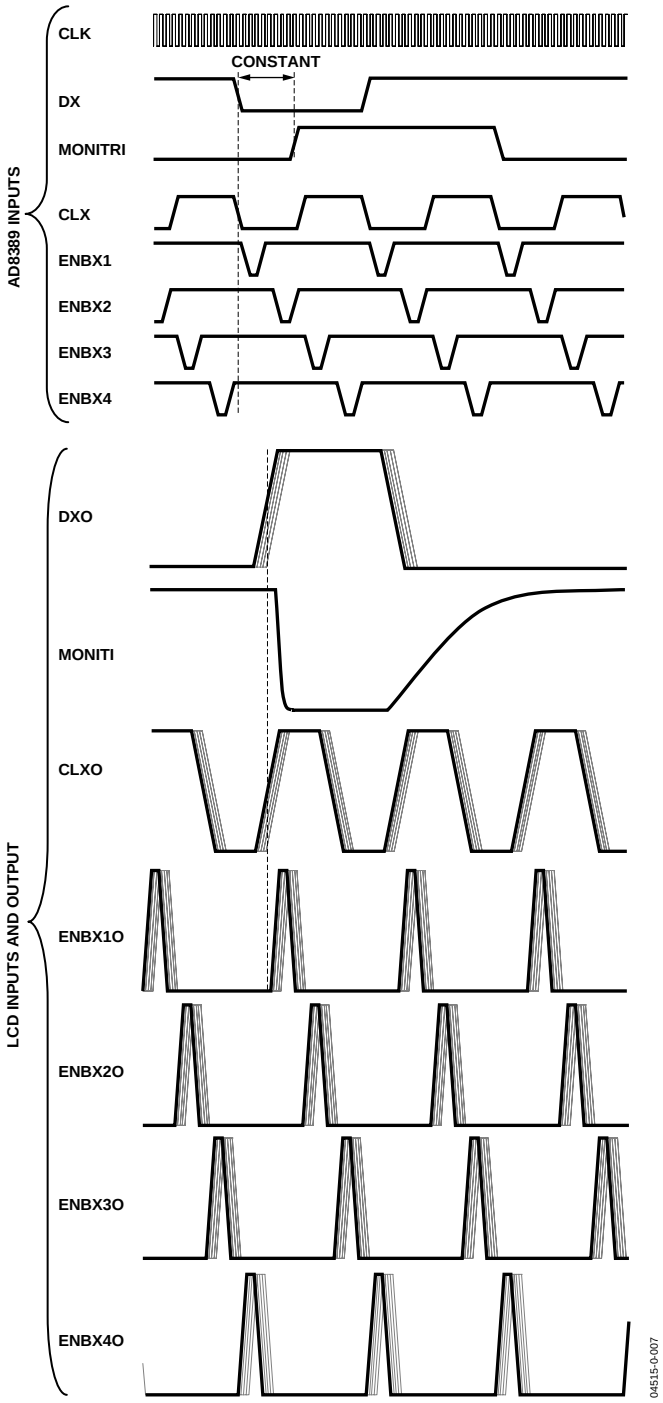


Figure 7. Typical Input Waveforms at the AD8389 and at the LCD. COMPEDGE = HIGH.

OUTLINE DIMENSIONS

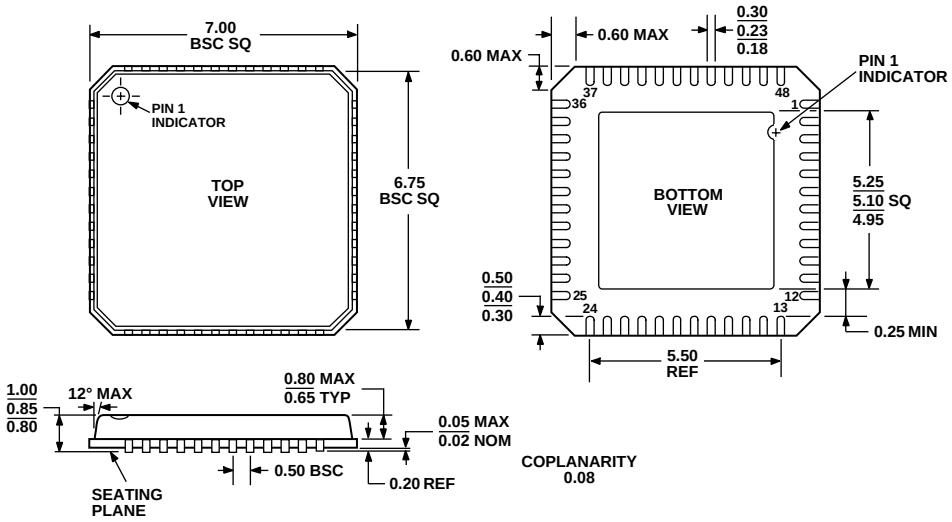


Figure 8. 48-Lead Frame Chip Scale Package [LFCSP] (CP-48)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD8389ACPZ[1]	0°C to 85°C	48-Lead Lead Frame Chip Scale Package	CP-48

[1] Z = lead-free.

NOTES

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D04515–0–10/03(0)