16 V Rail-to-Rail Buffer Amplifiers

AD8568/AD8569/AD8570

FEATURES

Single-Supply Operation: 4.5 V to 16 V
Input Capability Beyond the Rails
Rail-to-Rail Output Swing
Continuous Output Current: 35 mA
Peak Output Current: 250 mA
Offset Voltage: 10 mV Max
Slew Rate: 6 V/μs
Stable with 1 μF Loads
Supply Current

APPLICATIONS

LCD Reference Drivers
Portable Electronics
Communications Equipment

GENERAL DESCRIPTION

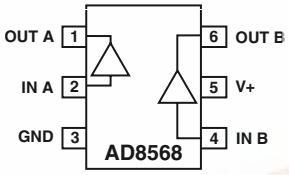
The AD8568, AD8569, and AD8570 are low-cost, single-supply buffer amplifiers with rail-to-rail input and output capability. They are optimized for LCD monitor applications and built on an advanced high voltage CBCMOS process. The AD8568 includes two buffers, the AD8569 includes four buffers, and the AD8570 includes eight buffers.

These LCD buffers have high slew rates, 35 mA continuous output drive, and high capacitive load drive capability. They have a wide supply range and offset voltages below 10 mV.

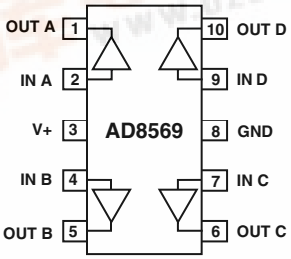
The AD8568, AD8569, and AD8570 are specified over the –40°C to +85°C temperature range. They are available on tape and reel, with the AD8568 packaged in a 6-lead SOT-23, the AD8569 in a 10-lead MSOP, and the AD8570 in a 32-lead LFCSP and 20-lead TSSOP.

PIN CONFIGURATIONS

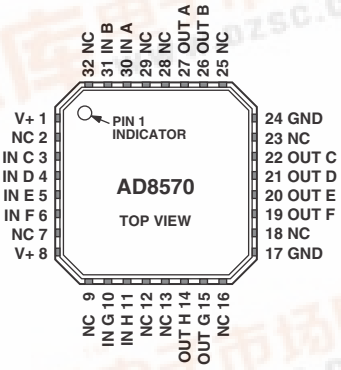
6-Lead SOT-23
(RT Suffix)



10-Lead MSOP
(RM Suffix)

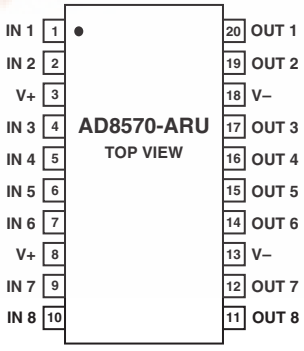


32-Lead LFCSP
(CP Suffix)



NC = NO CONNECT

20-Lead TSSOP



REV. C

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AD8568/AD8569/AD8570–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (4.5 V ≤ V_S ≤ 16 V, V_{CM} = V_S/2, T_A = 25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			2	10	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	–40°C ≤ T_A ≤ +85°C		5		µV/°C
Input Bias Current	I_B			80	600	nA
		–40°C ≤ T_A ≤ +85°C			800	nA
Input Voltage Range			–0.5		$–V_S$ + 0.5	V
Input Impedance	Z_{IN}			400		kΩ
Input Capacitance	C_{IN}			1		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L = 100 µA		V_S – 0.005		V
		V_S = 16 V, I_L = 5 mA	15.85	15.95		V
		–40°C ≤ T_A ≤ +85°C	15.75			V
		V_S = 4.5 V, I_L = 5 mA	4.2	4.38		V
		–40°C ≤ T_A ≤ +85°C	4.1			V
Output Voltage Low	V_{OL}	I_L = 100 µA		5		mV
		V_S = 16 V, I_L = 5 mA		42	150	mV
		–40°C ≤ T_A ≤ +85°C			250	mV
		V_S = 4.5 V, I_L = 5 mA		95	300	mV
		–40°C ≤ T_A ≤ +85°C			400	mV
Continuous Output Current	I_{OUT}			35		mA
Peak Output Current	I_{PK}	V_S = 16 V		250		mA
TRANSFER CHARACTERISTICS						
Gain	A_{VCL}	R_L = 2 kΩ	0.995	0.9985	1.005	V/V
		–40°C ≤ T_A ≤ +85°C	0.995	0.9980	1.005	V/V
Gain Linearity	NL	R_L = 2 kΩ, V_O = 0.5 to (V_S – 0.5 V)		0.01		%
POWER SUPPLY						
Supply Voltage	V_S		4.5		16	V
Power Supply Rejection Ratio	PSRR	V_S = 4 V to 17 V				
		–40°C ≤ T_A ≤ +85°C	70	90		dB
Supply Current/Amplifier	I_{SY}	V_O = V_S/2, No Load		700	850	µA
		–40°C ≤ T_A ≤ +85°C			1	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ, C_L = 200 pF	4	6		V/µs
Bandwidth	BW	–3 dB, R_L = 10 kΩ, C_L = 10 pF		6		MHz
Phase Margin	Øo	R_L = 10 kΩ, C_L = 10 pF		65		Degrees
Channel Separation				75		dB
NOISE PERFORMANCE						
Voltage Noise Density	e_n	f = 1 kHz		26		nV/$\sqrt{\text{Hz}}$
	e_n	f = 10 kHz		25		nV/$\sqrt{\text{Hz}}$
Current Noise Density	i_n	f = 10 kHz		0.8		pA/$\sqrt{\text{Hz}}$

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage (V_S) . . . . . 18 V
Input Voltage . . . . . –0.5 V to V_S + 0.5 V
Differential Input Voltage . . . . . V_S
Storage Temperature Range . . . . . –65°C to +150°C
Operating Temperature Range . . . . . –40°C to +85°C
Junction Temperature Range . . . . . –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) . . . . . 300°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Type	θ_{JA}[1]	θ_{JC}	Ψ_{JB}[2]	Unit
6-Lead SOT-23 (RT)	250	140		°C/W
10-Lead MSOP (RM)	200	44		°C/W
20-Lead TSSOP (RU)	72	45		°C/W
32-Lead LFCSP (CP)	35		13	°C/W

NOTES
[1]θ_{JA} is specified for worst-case conditions, i.e., θ_{JA} is specified for a device soldered onto a circuit board for surface-mount packages.
[2]Ψ_{JB} is applied for calculating the junction temperature by reference to the board temperature.

ORDERING GUIDE

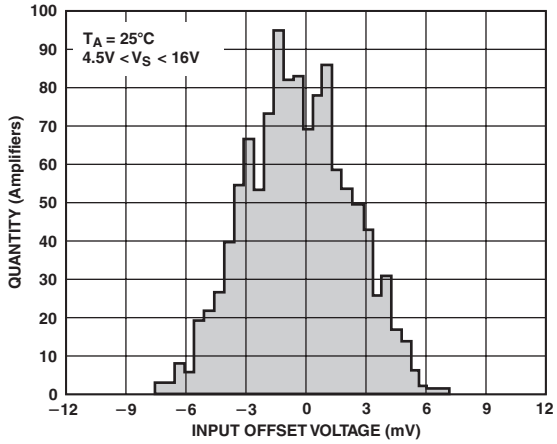
Model	Temperature Range	Package Description	Package Option	Branding Information
AD8568ART-R2	–40°C to +85°C	6-Lead SOT-23	RT-6	AWA
AD8568ART-REEL	–40°C to +85°C	6-Lead SOT-23	RT-6	AWA
AD8568ART-REEL7	–40°C to +85°C	6-Lead SOT-23	RT-6	AWA
AD8569ARM-R2	–40°C to +85°C	10-Lead MSOP	RM-10	AXA
AD8569ARM-REEL	–40°C to +85°C	10-Lead MSOP	RM-10	AXA
AD8569ARMZ-REEL*	–40°C to +85°C	10-Lead MSOP	RM-10	AXA
AD8570ACP-R2	–40°C to +85°C	32-Lead LFCSP	CP-32-2	
AD8570ACP-REEL	–40°C to +85°C	32-Lead LFCSP	CP-32-2	
AD8570ACP-REEL7	–40°C to +85°C	32-Lead LFCSP	CP-32-2	
AD8570ARU	–40°C to +85°C	20-Lead TSSOP	RU-20	
AD8570ARU-REEL	–40°C to +85°C	20-Lead TSSOP	RU-20	

*Z = Pb-free part.

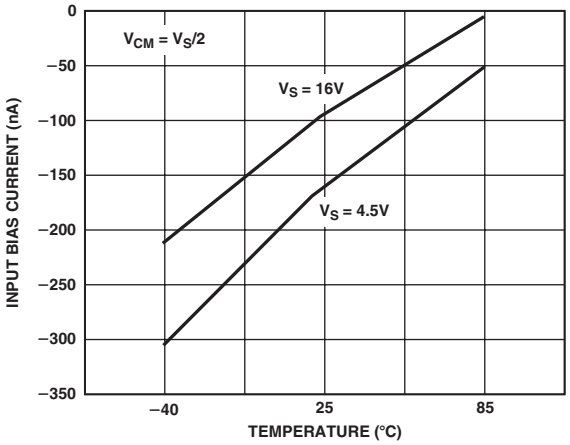
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8568/AD8569/AD8570 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

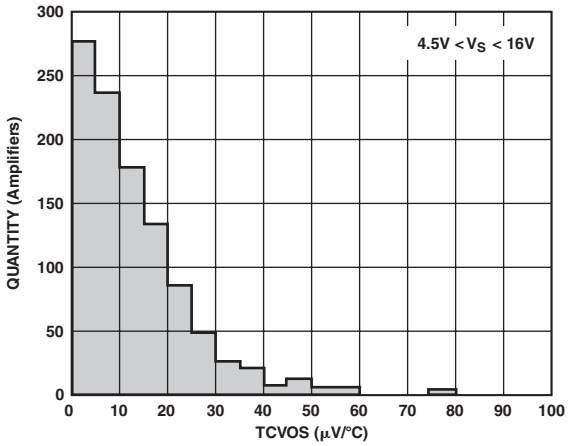
AD8568/AD8569/AD8570–Typical Performance Characteristics



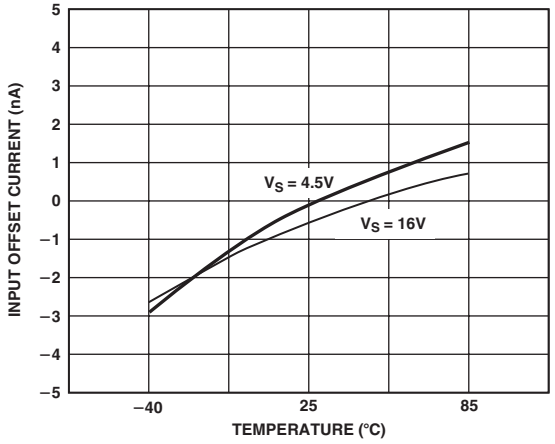
TPC 1. Input Offset Voltage Distribution



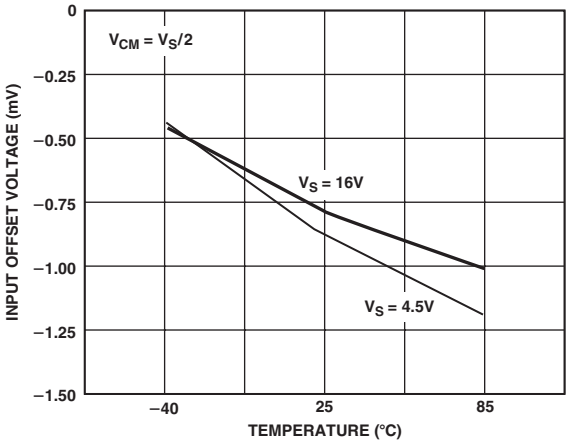
TPC 4. Input Bias Current vs. Temperature



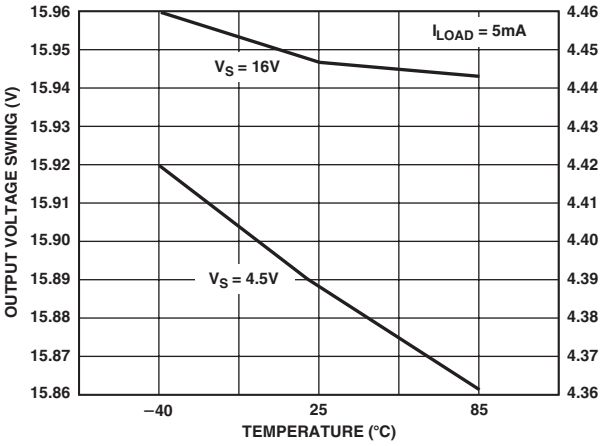
TPC 2. Input Offset Voltage Drift Distribution



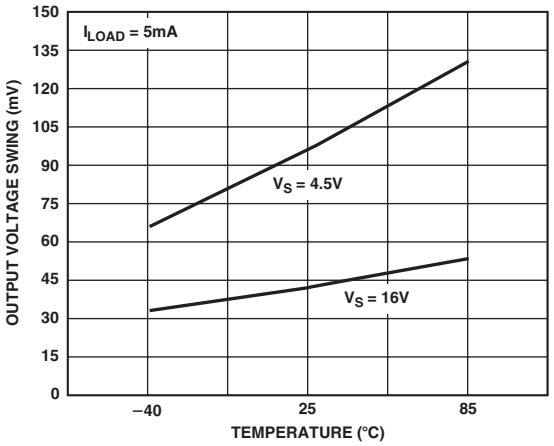
TPC 5. Input Offset Current vs. Temperature



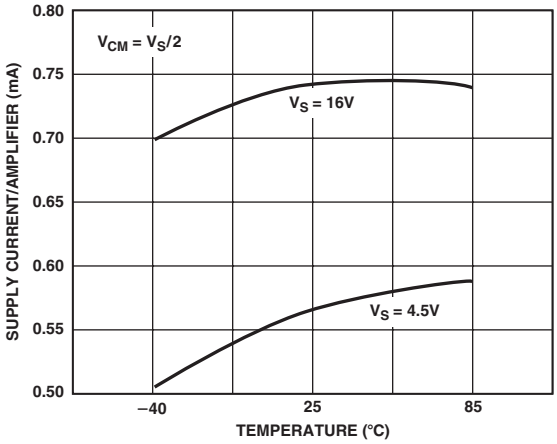
TPC 3. Input Offset Voltage vs. Temperature



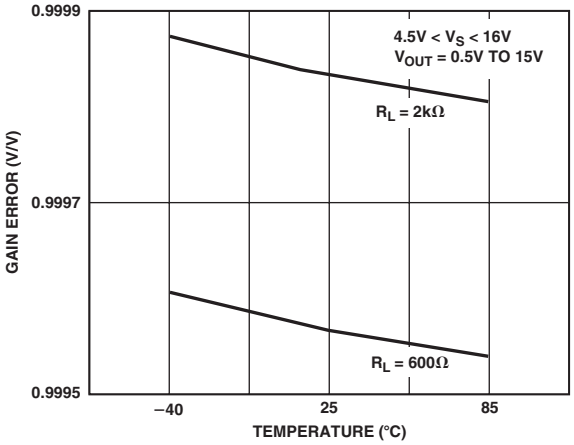
TPC 6. Output Voltage Swing vs. Temperature



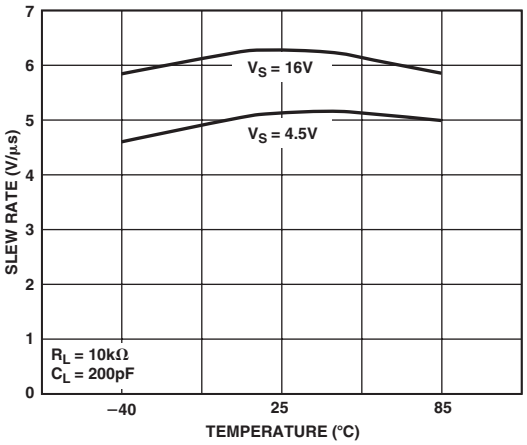
TPC 7. Output Voltage Swing vs. Temperature



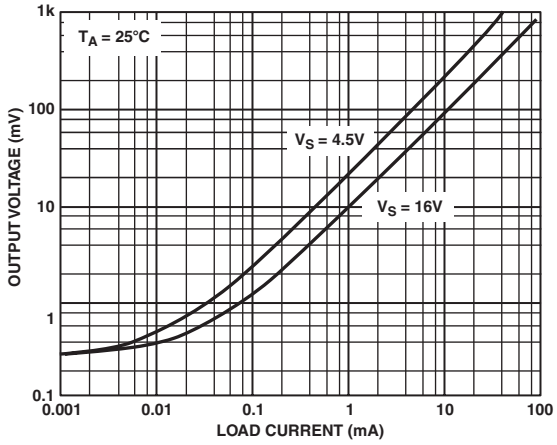
TPC 10. Supply Current/Amplifier vs. Temperature



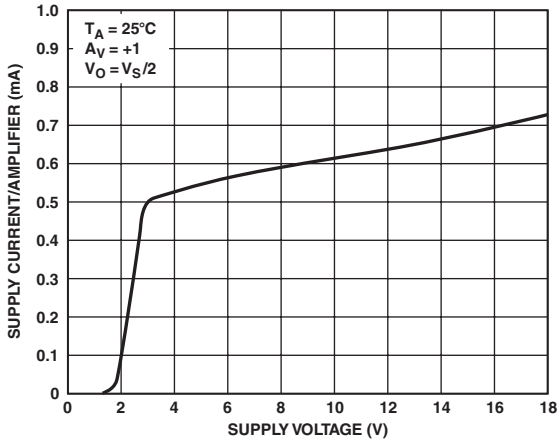
TPC 8. Voltage Gain vs. Temperature



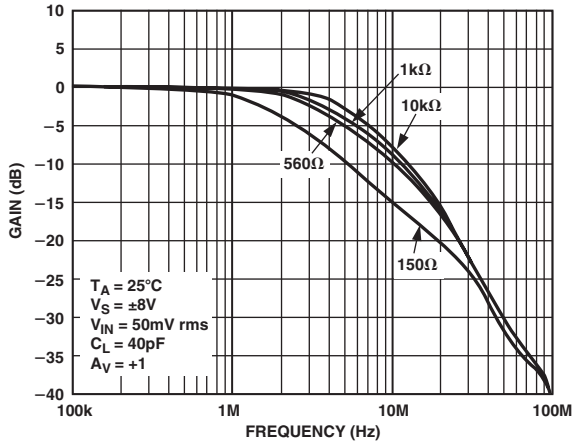
TPC 11. Slew Rate vs. Temperature



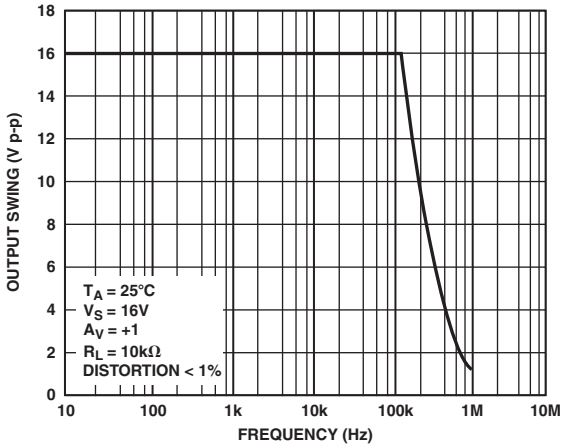
TPC 9. Output Voltage to Supply Rail vs. Load Current



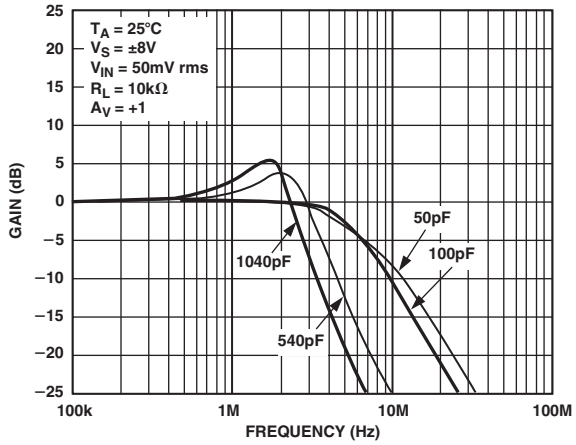
TPC 12. Supply Current/Amplifier vs. Supply Voltage



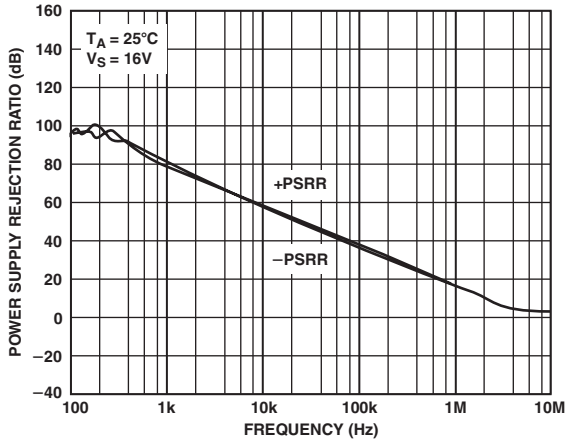
TPC 13. Frequency Response vs. Resistive Loading



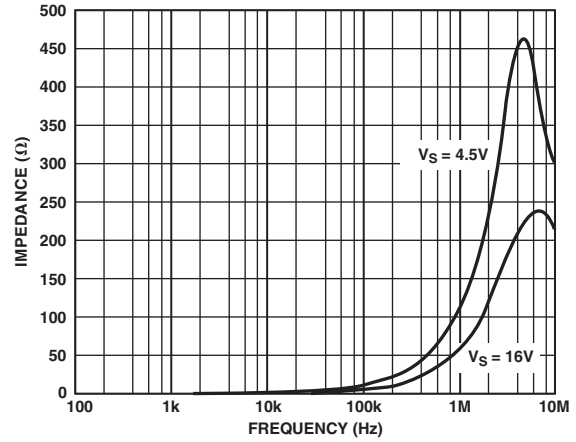
TPC 16. Closed-Loop Output Swing vs. Frequency



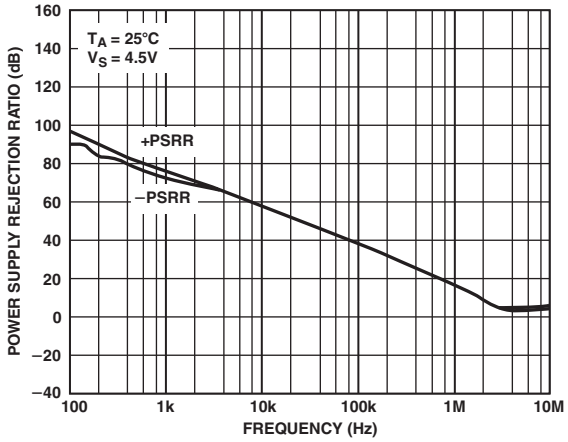
TPC 14. Frequency Response vs. Capacitive Loading



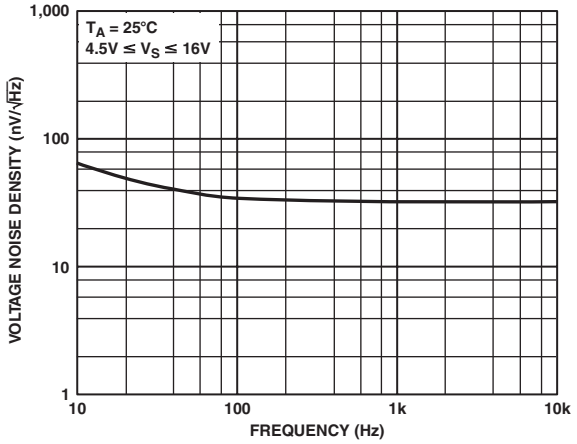
TPC 17. Power Supply Rejection Ratio vs. Frequency



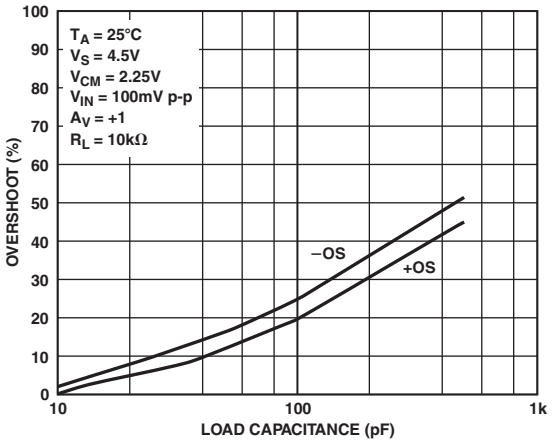
TPC 15. Closed-Loop Output Impedance vs. Frequency



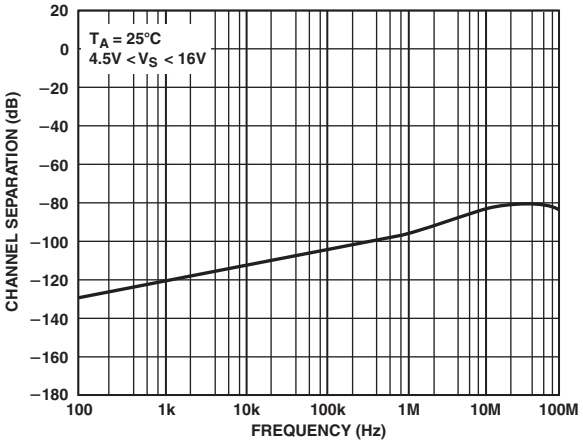
TPC 18. Power Supply Rejection Ratio vs. Frequency



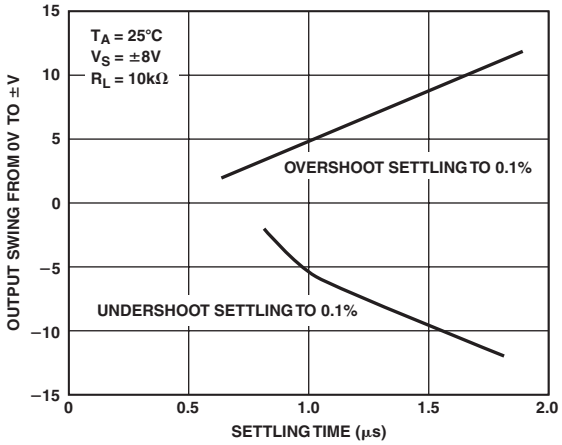
TPC 19. Voltage Noise Density vs. Frequency



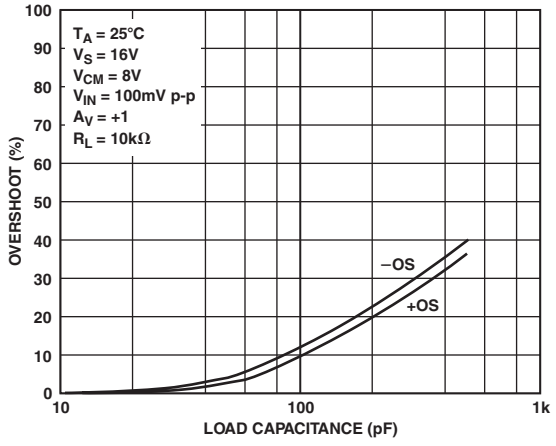
TPC 22. Small Signal Overshoot vs. Load Capacitance



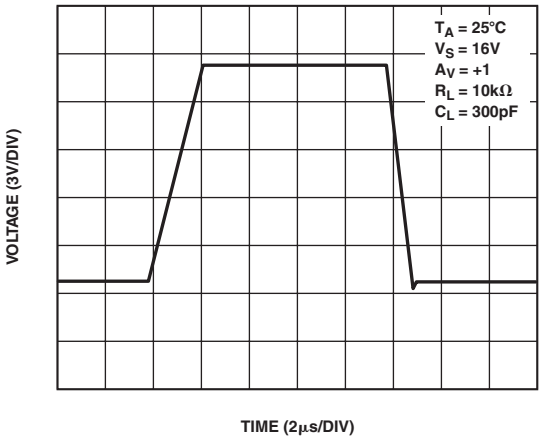
TPC 20. Channel Separation vs. Frequency



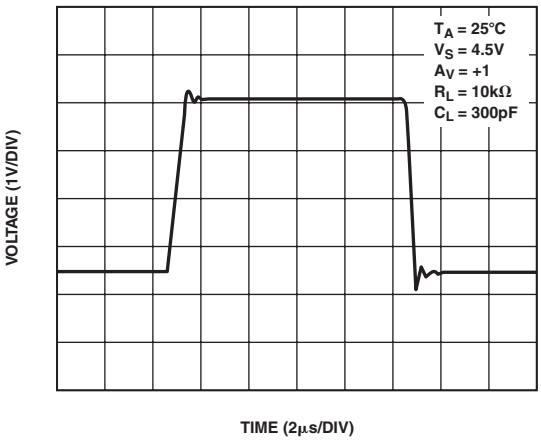
TPC 23. Settling Time vs. Step Size



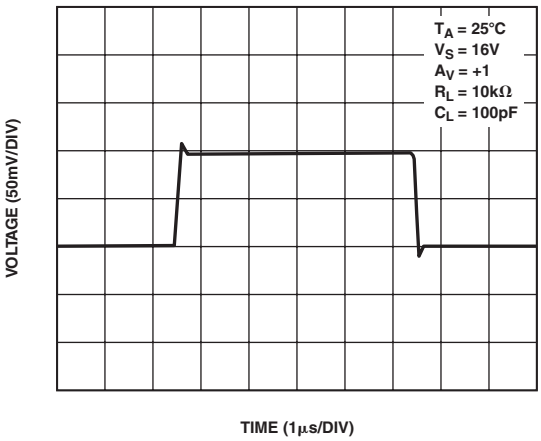
TPC 21. Small Signal Overshoot vs. Load Capacitance



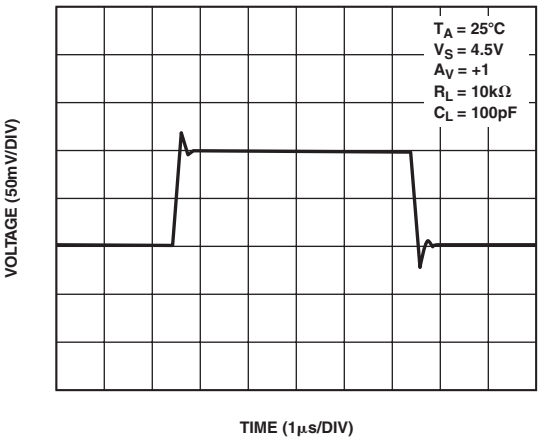
TPC 24. Large Signal Transient Response



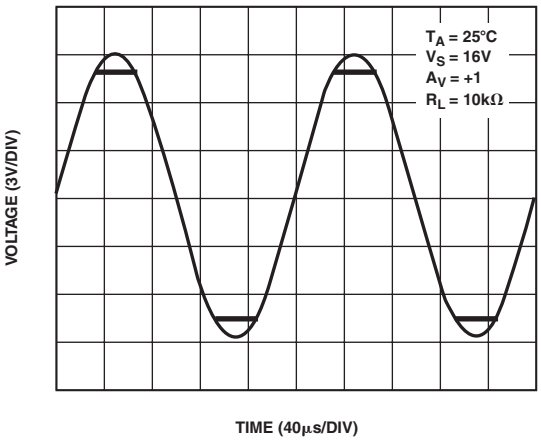
TPC 25. Large Signal Transient Response



TPC 26. Small Signal Transient Response



TPC 27. Small Signal Transient Response



TPC 28. No Phase Reversal

APPLICATIONS

Theory of Operation

This family of buffers is designed to drive large capacitive loads in LCD applications. Each has high output current drive and rail-to-rail input/output operation and can be powered from a single 16 V supply. They are also intended for other applications where low distortion and high output current drive are needed.

Input Overvoltage Protection

As with any semiconductor device, whenever the input exceeds either supply voltage, attention needs to be paid to the input overvoltage characteristics. As an overvoltage occurs, the amplifier could be damaged, depending on the voltage level and the magnitude of the fault current. When the input voltage exceeds either supply by more than 0.6 V, the internal pn junctions will allow current to flow from the input to the supplies.

This input current is not inherently damaging to the device as long as it is limited to 5 mA or less. If a condition exists using the buffers where the input exceeds the supply by more than 0.6 V, an external series resistor should be added. The size of the resistor can be calculated by using the maximum overvoltage divided by 5 mA. This resistance should be placed in series with the input exposed to an overvoltage.

Output Phase Reversal

The buffer family is immune to phase reversal. Although the device's output will not change phase, large currents due to input overvoltage could damage the device. In applications where the possibility exists of an input voltage exceeding the supply voltage, overvoltage protection should be used as described in the previous section.

Power Dissipation

The maximum allowable internal junction temperature of 150°C limits the device's maximum power dissipation. As the ambient temperature increases, the maximum power dissipated by the device must decrease linearly to maintain the maximum junction temperature. If this maximum junction temperature is exceeded momentarily, the device will still operate properly once the junction temperature is reduced below 150°C. If the maximum junction temperature is exceeded for an extended period of time, overheating could lead to permanent damage of the device.

The maximum safe junction temperature, T_{JMAX}, is 150°C. Using the following formula, we can obtain the maximum power that the buffer family can safely dissipate as a function of temperature.

$$P_{DISS} = \left(T_{JMAX} - T_A\right) / \theta_{JA}$$

where:

P_{DISS} = the power dissipation.
T_{JMAX} = the maximum allowable junction temperature (150°C).
T_A = the ambient temperature of the circuit.
θ_{JA} = the AD856x package thermal resistance, junction-to-ambient.

The power dissipated by the device can be calculated as

$$P_{DISS} = \left(V_S - V_{OUT}\right) \times I_{LOAD}$$

where:

V_S = the supply voltage.
V_{OUT} = the output voltage.
I_{LOAD} = the output load current.

Figure 1 shows the maximum power dissipation versus temperature. To achieve proper operation, use the previous equation to calculate P_{DISS} for a specific package at any given temperature, or see Figure 1.

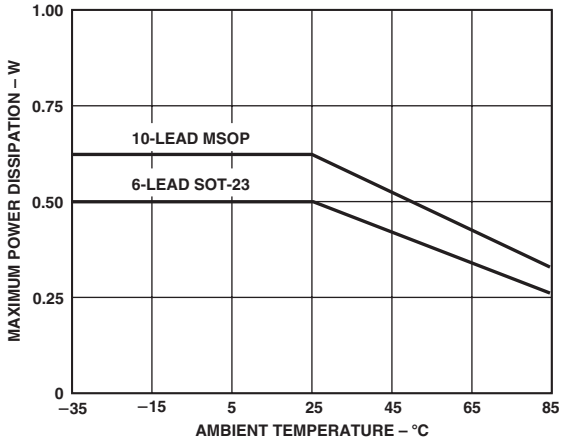


Figure 1. Maximum Power Dissipation vs. Temperature for 6- and 10-Lead Packages

Total Harmonic Distortion + Noise (THD+N)

The buffer family features low THD+N. The total harmonic distortion plus noise for the buffer over the entire supply range is below 0.08%. When the device is powered from a 16 V supply, the THD+N stays below 0.03%. Figure 2 shows the AD8568 THD+N versus frequency performance.

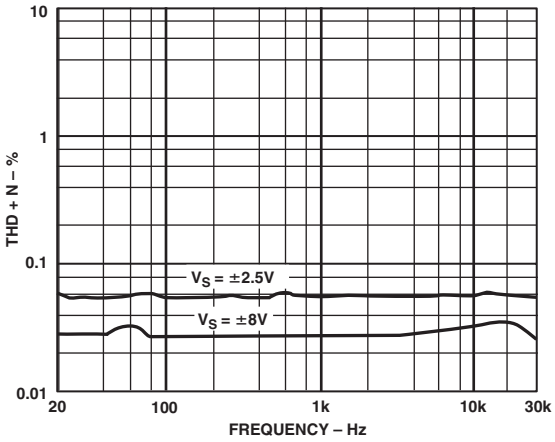


Figure 2. AD8568 THD+N vs. Frequency

Short-Circuit Output Conditions

The buffer family does not have internal short-circuit protection circuitry. As a precautionary measure, do not short the output directly to the positive power supply or to ground.

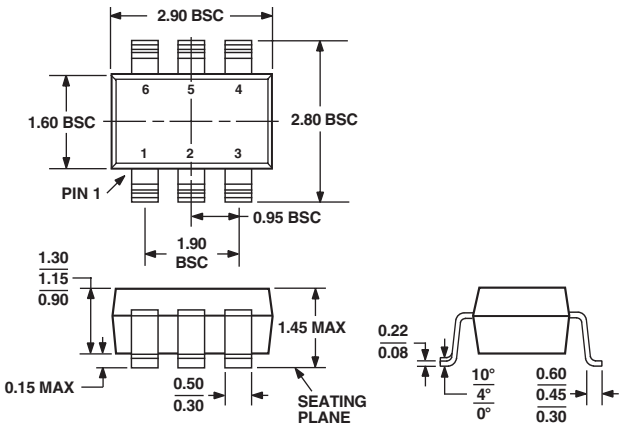
It is not recommended to operate the AD856x with more than 35 mA of continuous output current. The output current can be limited by placing a series resistor at the output of the amplifier whose value can be derived using the following equation.

$$R_X \geq \frac{V_S}{35\,mA}$$

For a 5 V single-supply operation, R_X should have a minimum value of 143 Ω.

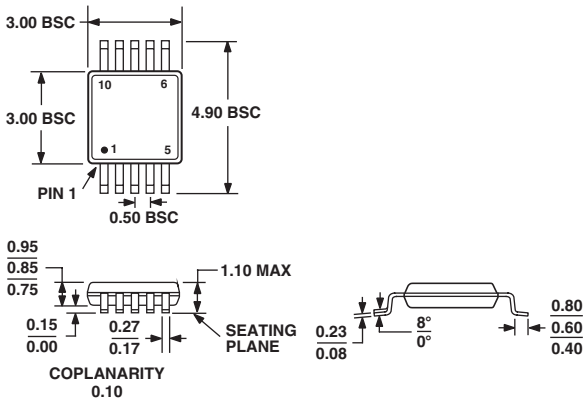
OUTLINE DIMENSIONS

6-Lead Small Outline Transistor Package [SOT-23]
(RT-6)
Dimensions shown in millimeters



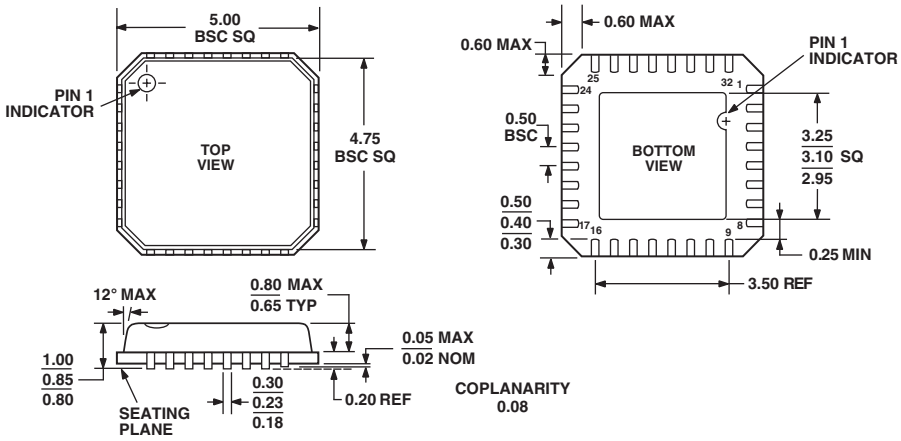
COMPLIANT TO JEDEC STANDARDS MO-178AB

10-Lead Micro Small Outline Package [MSOP]
(RM-10)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-187BA

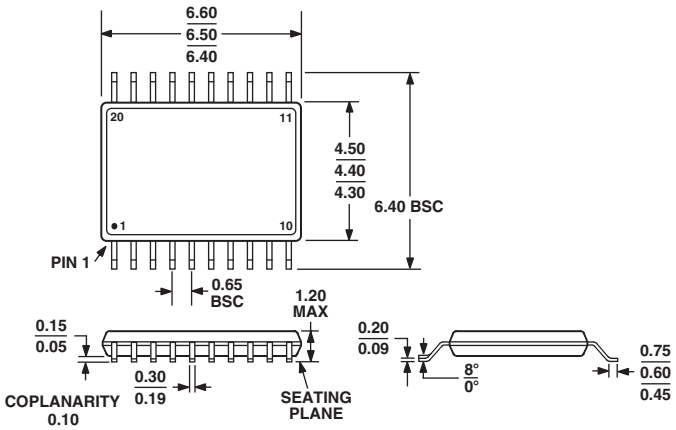
32-Lead Lead Frame Chip Scale Package [LFCSP]
5 x 5 mm Body
(CP-32-2)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-VHHD-2

OUTLINE DIMENSIONS

20-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-20)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-153AC

Revision History

Location	Page

12/03—Data Sheet changed from REV. B to REV. C.

5/02—Data Sheet changed from REV. A to REV. B.