



Dual Ultralow Distortion, Ultralow Noise Op Amp

AD8599

FEATURES

- Low noise: 1 nV/√Hz at 1kHz
- Low distortion: -105 dB THD @ 20 kHz
- <80 nV p-p input noise, 0.1 Hz to 10 Hz
- Slew rate: 16 V/μs
- Wide bandwidth: 10 MHz
- Supply current: 4.7 mA/amp typical
- Low offset voltage: 10 μV typical
- CMRR: 120 dB
- Unity-gain stable
- ±15 V operation

APPLICATIONS

- Professional audio preamplifiers
- ATE/precision testers
- Imaging systems
- Medical/physiological measurements
- Precision detectors/instruments
- Precision data conversion

GENERAL DESCRIPTION

The AD8599 is a dual, very low noise, low distortion operational amplifier ideal for use as a preamplifier. The low noise of 1 nV/√Hz and low harmonic distortion of -105 dB (or better) at audio bandwidths give the AD8599 the wide dynamic range necessary for preamps in audio, medical, and instrumentation applications. The AD8599's excellent slew rate of 16 V/μs and

FUNCTIONAL BLOCK DIAGRAM

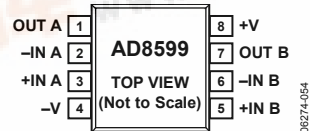


Figure 1. 8-Lead SOIC (R-8)

10 MHz gain bandwidth make it highly suitable for medical applications. The low distortion and settling time of the AD8599 make it ideal for buffering of high resolution data converters.

The AD8599 is available in an 8-Lead SOIC package and is specified over the -40°C to +125°C temperature range.



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REVISION HISTORY

2/07—Revision 0: Initial Version

SPECIFICATIONS

$V_S = \pm 15\text{ V}$, $V_{CM} = 0\text{ V}$, $V_O = 0\text{ V}$, $T_A = +25^\circ\text{C}$, unless otherwise specified.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		10	120	μV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			180	μV
Input Bias Current	I_B	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		0.8	2.2	$\mu\text{V}/^\circ\text{C}$
Input Offset Current	I_{OS}	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		25	180	nA
Input Voltage Range	IVR	$V_{DD} = \pm 15\text{ V}$	-12.5		+12.5	V
Common-Mode Rejection Ratio	CMRR	$-12.5\text{ V} \leq V_{CM} \leq +12.5\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	120	140		dB
Large Signal Voltage Gain	A_{VO}	$R_L \geq 600\ \Omega$, $V_O = -11\text{ V to } +11\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	115	116		dB
Input Capacitance	C_{DIFF} C_{CM}			4.8		pf
				4.5		pf
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	$R_L = 600\ \Omega$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	13.1	13.4		V
		$R_L = 2\ \text{k}\Omega$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	12.8	13.7		V
Output Voltage Low	V_{OL}	$R_L = 600\ \Omega$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	13.5		-13.2	V
		$R_L = 2\ \text{k}\Omega$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	13.2		-12.9	V
Output Source Circuit	I_{SC}			± 52		mA
Closed-Loop Output Impedance	Z_{OUT}	At 1 MHz, $A_V = +1$		5		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_{DD} = \pm 18\text{ V to } \pm 4.5\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	120	140		dB
Supply Current per Amplifier	I_{SY}	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	118	4.7	5.7	dB
					6.75	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	$A_V = -1$, $R_L = 2\ \text{k}\Omega$ $A_V = 1$, $R_L = 2\ \text{k}\Omega$		16.8		V/ μs
Settling Time	t_s	To 0.01%, step = 10 V		15		V/ μs
Gain Bandwidth Product	GBP			2		μs
Phase Margin	ϕ_M			10		MHz
				68		Degrees
NOISE PERFORMANCE						
Peak-to-Peak Noise	$e_n\text{ p-p}$	0.1 Hz to 10 Hz		76		nV
Voltage Noise Density	e_n	$f = 1\ \text{kHz}$ $f = 10\ \text{kHz}$		1.07	1.15	nV/ $\sqrt{\text{Hz}}$
Current Noise		$f = 1\ \text{kHz}$			1.5	nV/ $\sqrt{\text{Hz}}$
Total Harmonic Distortion + Noise	THD + N	$G = 1$, $R_L \geq 1\ \text{k}\Omega$, $f = 1\ \text{kHz}$, $V_{RMS} = 3\text{ V}$, $\pm 15\text{ V}$ $G = 1$, $R_L \geq 1\ \text{k}\Omega$, $f = 20\ \text{kHz}$, $V_{RMS} = 3\text{ V}$, $\pm 15\text{ V}$		1.5		pA/ $\sqrt{\text{Hz}}$
Channel Separation	CS	$f = 10\ \text{kHz}$		-108		dB
				-105		dB
				-120		dB

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ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	±18 V
Input Voltage	GND to V_{DD}
Differential Input Voltage	±1 V
Output Short-Circuit to GND	Indefinite
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +125°C
Lead Temperature Range (Soldering 60 sec)	300°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead SOIC (R-8)	120	36	°C/W

POWER SEQUENCING

The op amp supplies must be established simultaneously with, or before, any input signals are applied.

If this is not possible, the input current must be limited to 10 mA.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

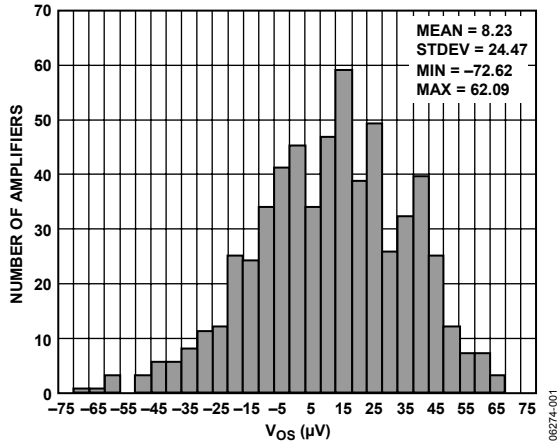


Figure 2. Input Offset Voltage Distribution $V_S = \pm 5 V$

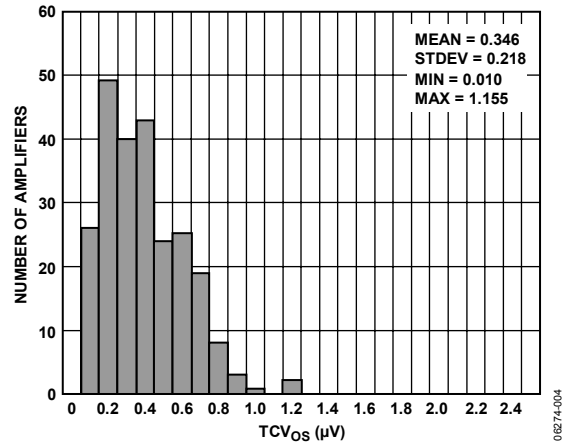


Figure 5. TCV_{OS} Distribution $V_S = \pm 5 V, -40^\circ C \leq T_A \leq +125^\circ C$

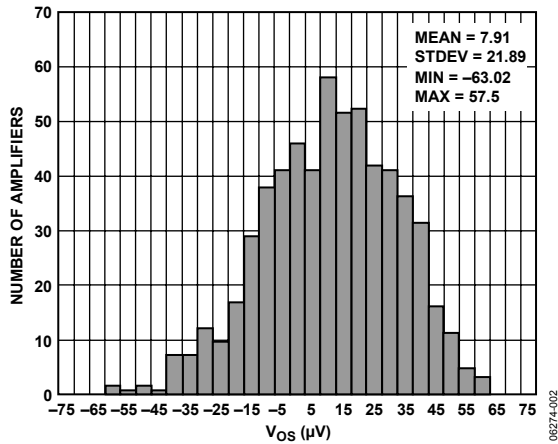


Figure 3. Input Offset Voltage Distribution $V_S = \pm 15 V$

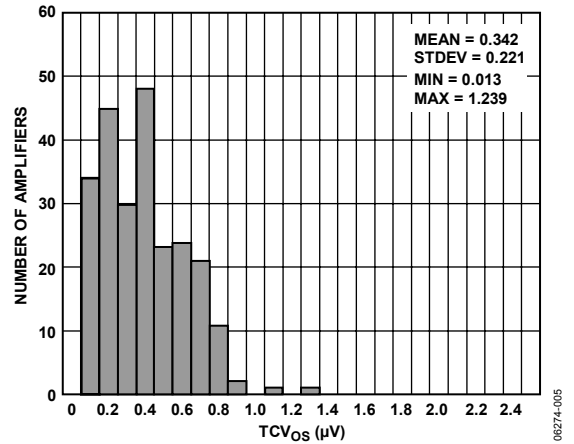


Figure 6. TCV_{OS} Distribution $V_S = \pm 15 V, -40^\circ C \leq T_A \leq +85^\circ C$

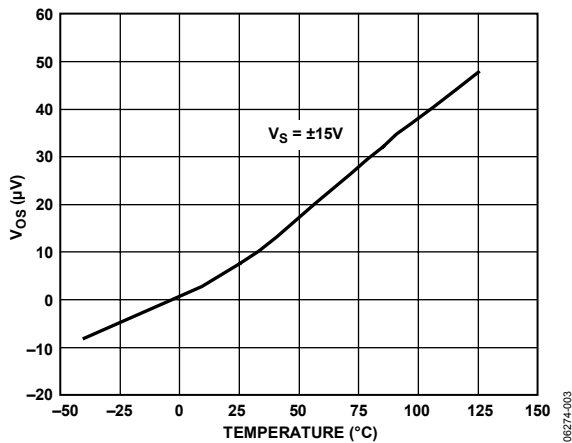


Figure 4. Input Offset Voltage vs. Temperature

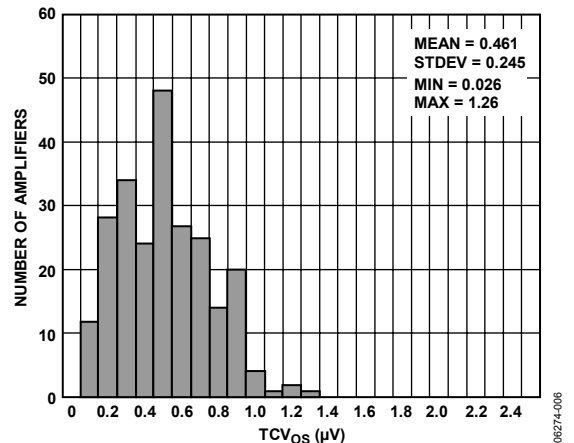


Figure 7. TCV_{OS} Distribution $V_S = \pm 5 V, -40^\circ C \leq T_A \leq +85^\circ C$

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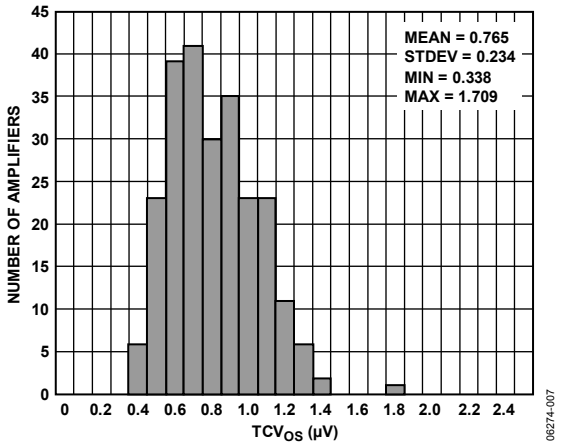


Figure 8. TCV_{OS} Distribution, $V_S = \pm 15\text{ V}$, $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$

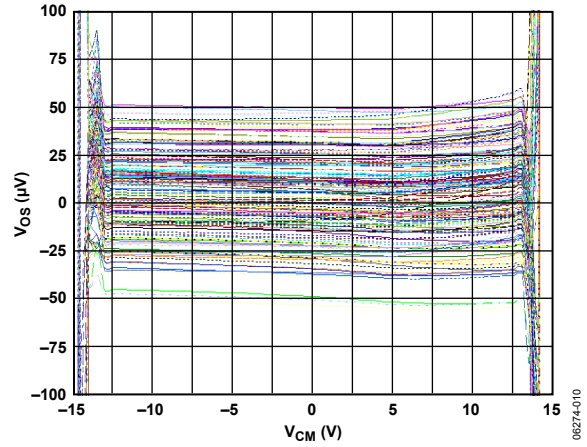


Figure 11. Offset Voltage vs. V_{CM} , $V_S = \pm 15\text{ V}$

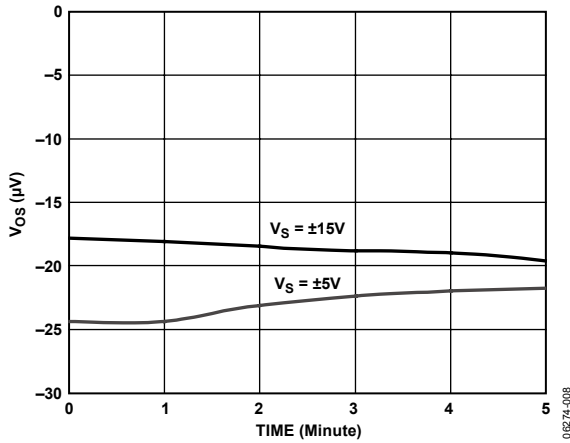


Figure 9. Offset Voltage vs. Time

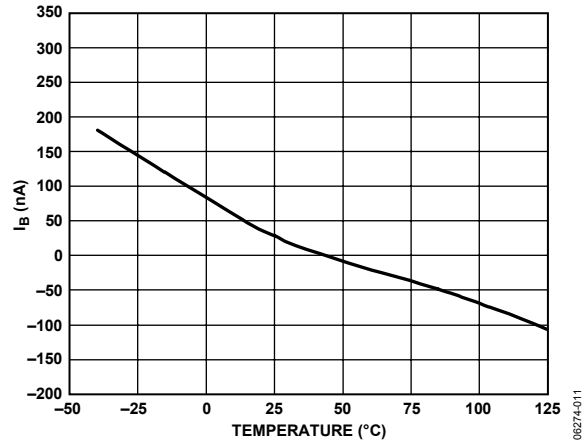


Figure 12. Input Bias Current vs. Temperature $V_S = \pm 5\text{ V}$, $V_{CM} = 0\text{ V}$

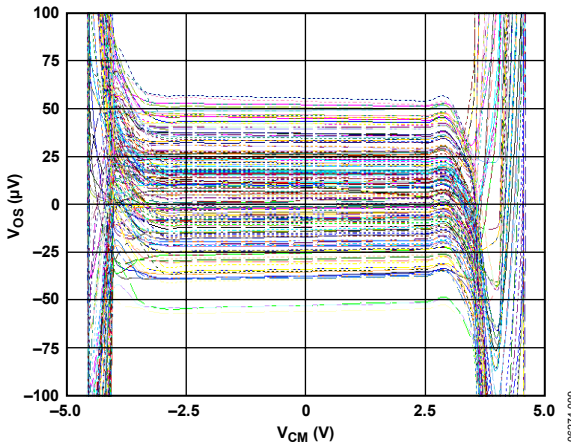


Figure 10. Offset Voltage vs. V_{CM} , $V_S = \pm 5\text{ V}$

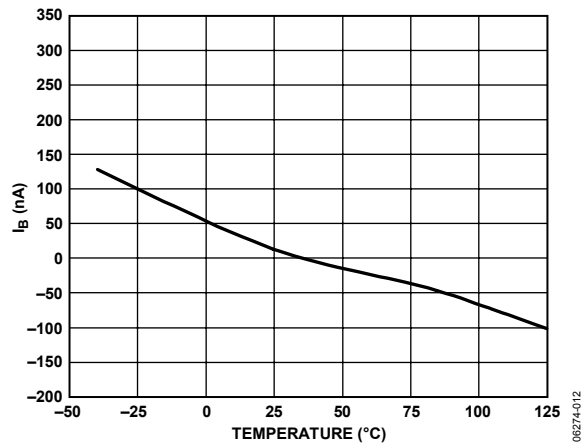


Figure 13. Input Bias Current vs. Temperature $V_S = \pm 15\text{ V}$, $V_{CM} = 0\text{ V}$

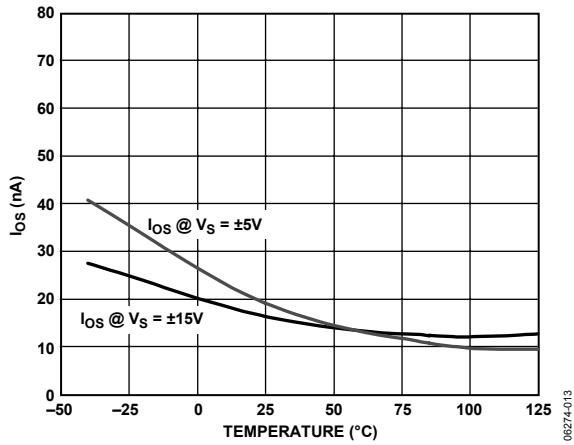


Figure 14. Input Offset Current vs. Temperature

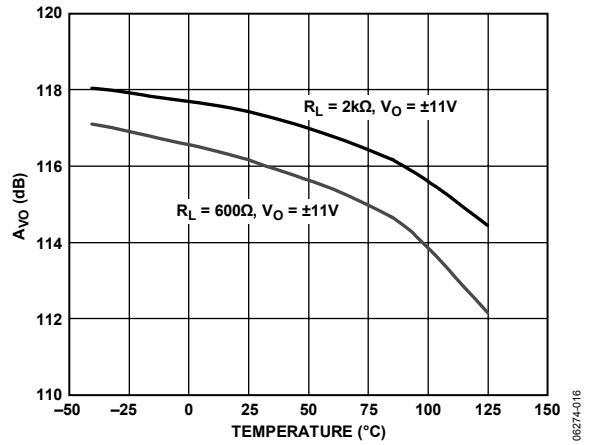


Figure 17. Large Signal Voltage Gain vs. Temperature, $V_S = \pm 15 V$

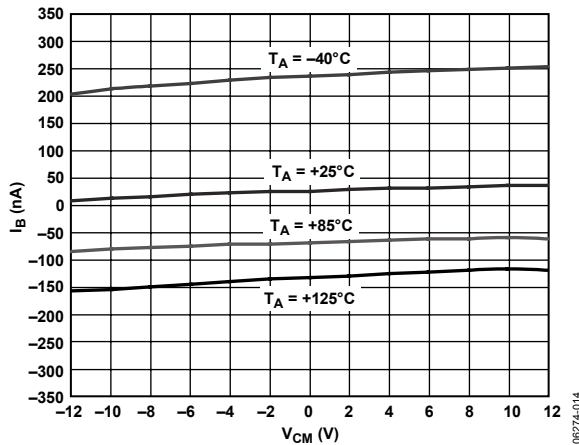


Figure 15. Input Bias Current vs. V_{CM} , $V_S = \pm 15 V$

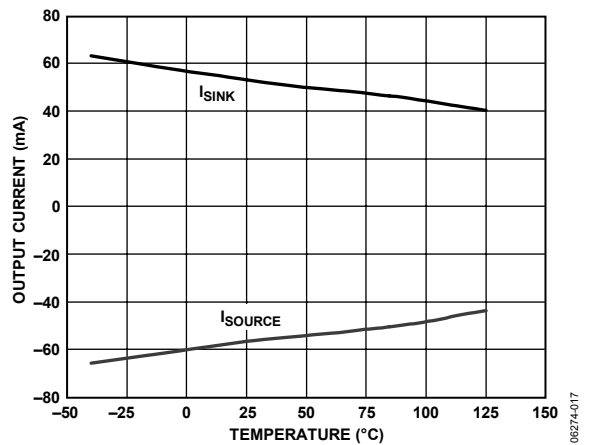


Figure 18. Output Current vs. Temperature, $V_S = \pm 15 V$

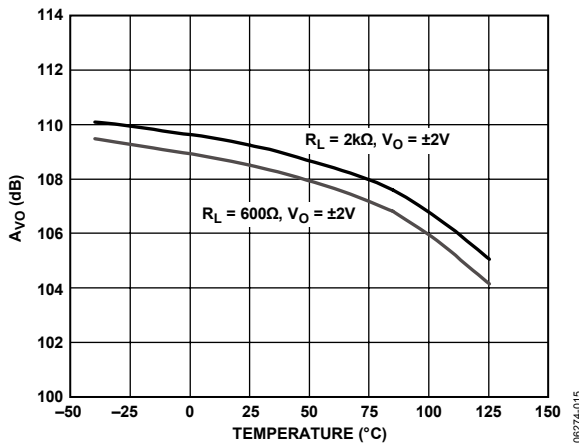


Figure 16. Large Signal Voltage Gain vs. Temperature $V_S = \pm 5 V$

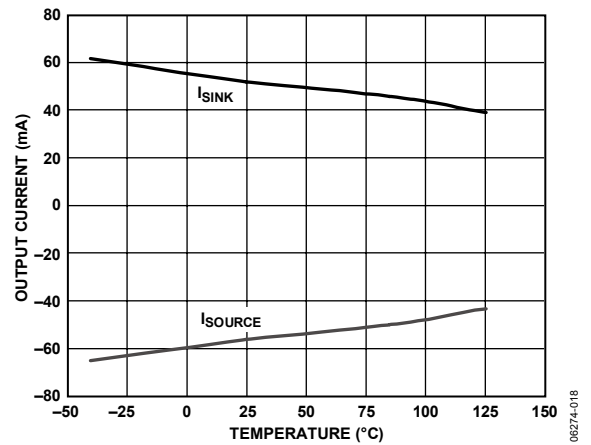


Figure 19. Output Current vs. Temperature, $V_S = \pm 15 V$

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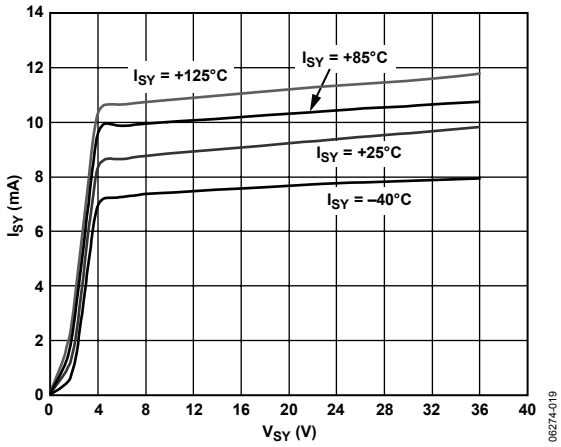


Figure 20. Supply Current vs. Supply Voltage

06274-019

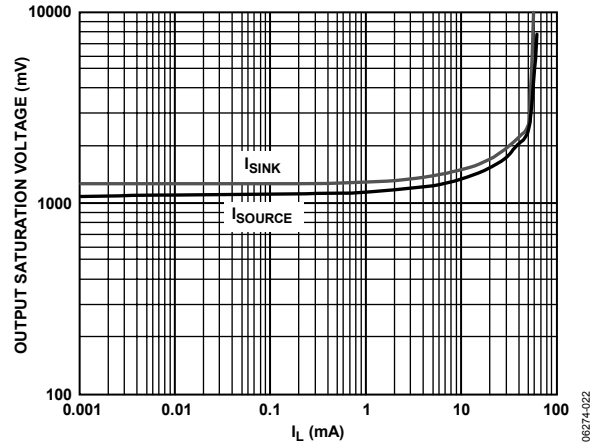


Figure 23. Output Saturation Voltage vs. Current Load, $V_S = \pm 15 V$

06274-022

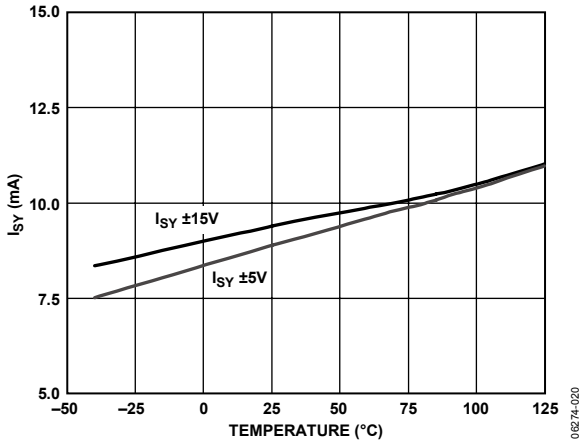


Figure 21. Supply Current vs. Temperature

06274-020

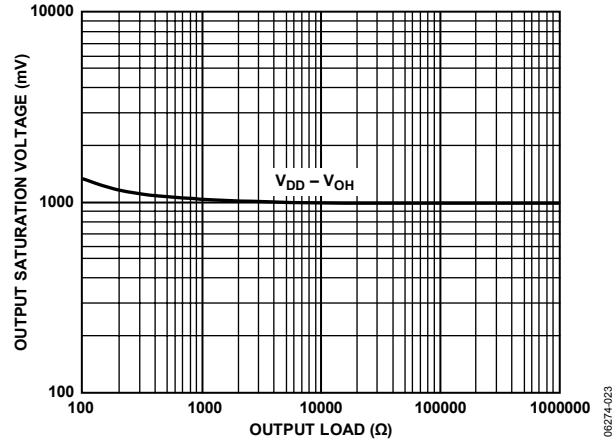


Figure 24. Output Saturation Voltage vs. R_L , $V_S = \pm 15 V$

06274-023

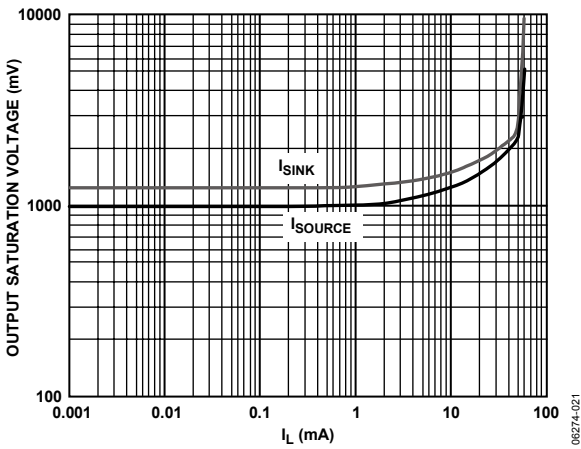


Figure 22. Output Saturation Voltage vs. Current Load, $V_S = \pm 5 V$

06274-021

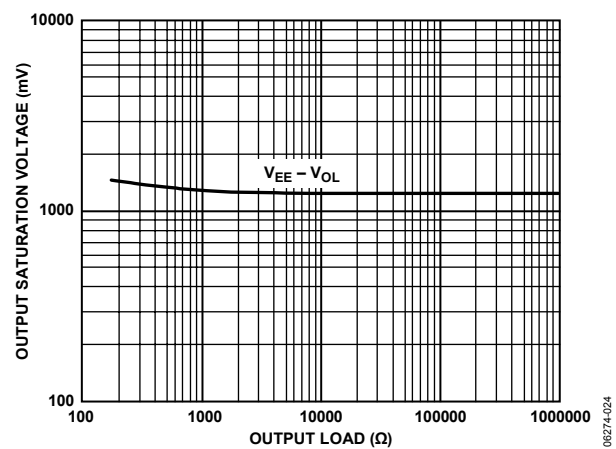


Figure 25. Output Saturation Voltage vs. R_L , $V_S = \pm 5 V$

06274-024

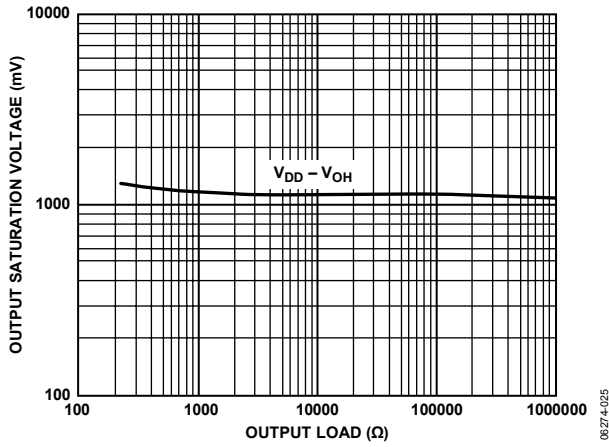


Figure 26. Output Saturation Voltage vs. R_L , $V_S = \pm 15 V$

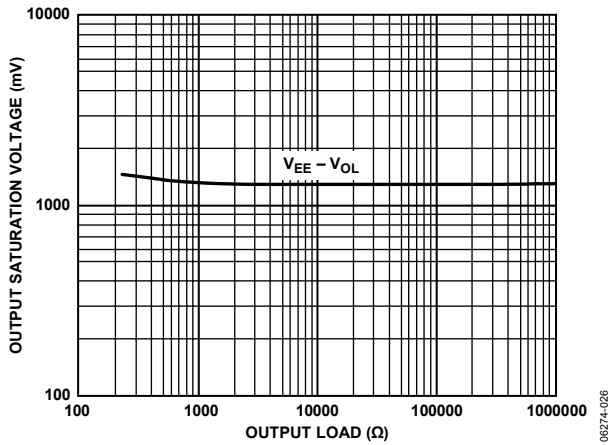


Figure 27. Output Saturation Voltage vs. R_L , $V_S = \pm 15 V$

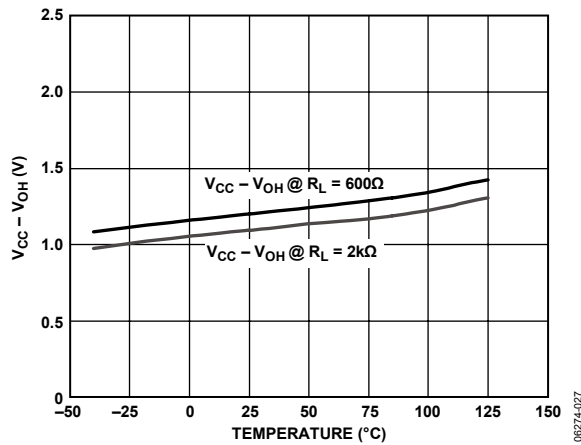


Figure 28. Output Saturation Voltage vs. Temperature, $V_S = \pm 5 V$

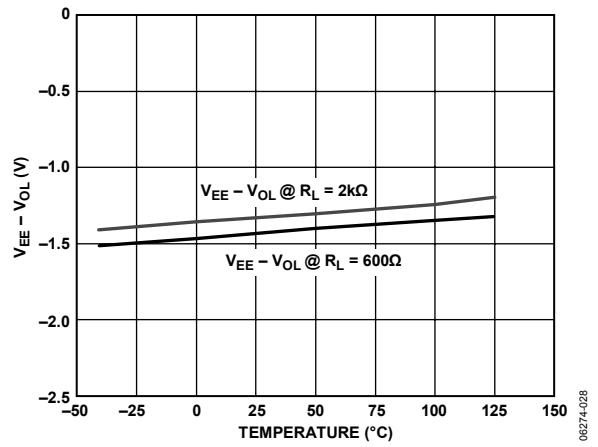


Figure 29. Output Saturation Voltage vs. Temperature, $V_S = \pm 5 V$

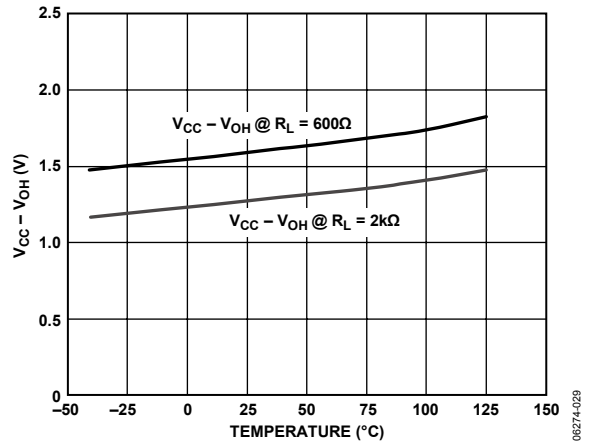


Figure 30. Output Saturation Voltage vs. Temperature, $V_S = \pm 15 V$

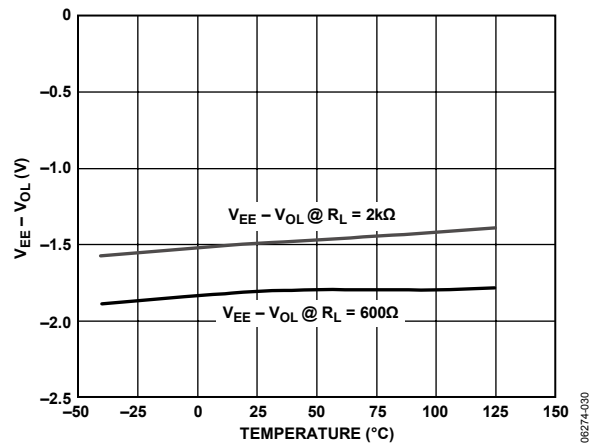


Figure 31. Output Saturation Voltage vs. Temperature, $V_S = \pm 15 V$

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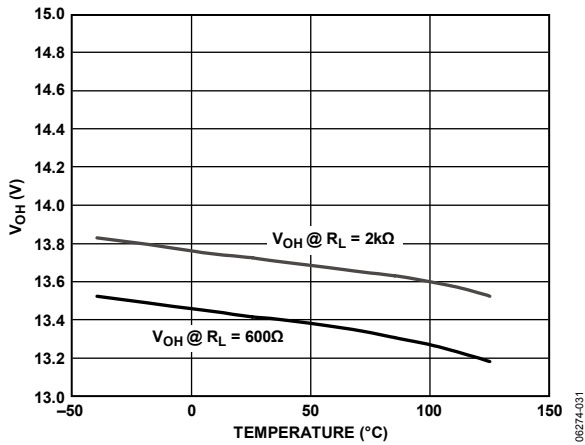


Figure 32. Output Voltage High vs. Temperature, $V_S = \pm 15 V$

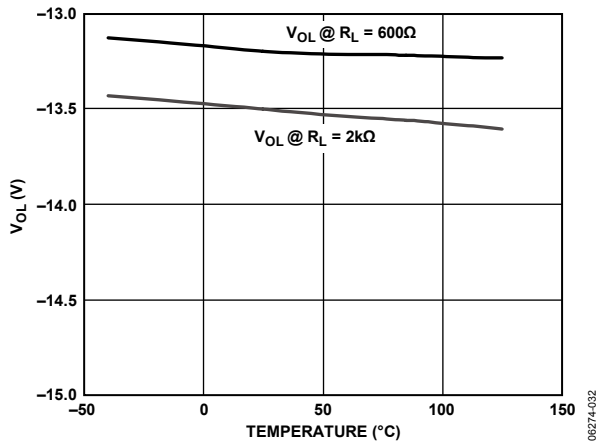


Figure 33. Output Voltage Low vs. Temperature, $V_S = \pm 15 V$

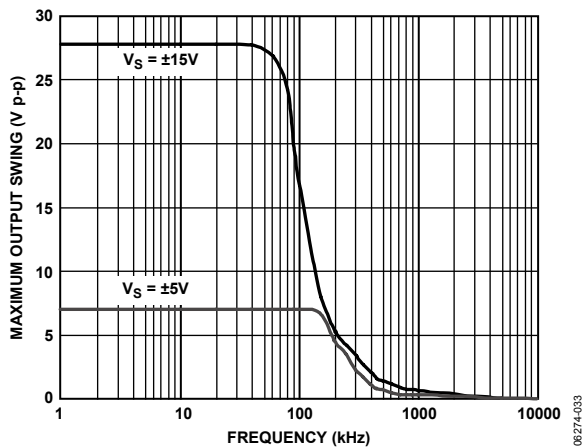


Figure 34. Maximum Output Swing vs. Frequency

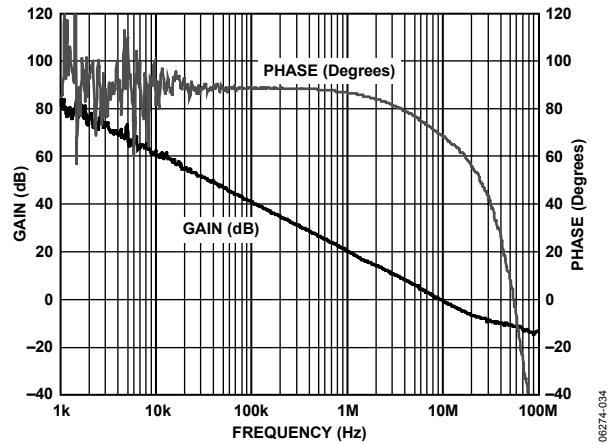


Figure 35. Gain and Phase vs. Frequency, $\pm 5 V \leq V_S \leq \pm 15 V$

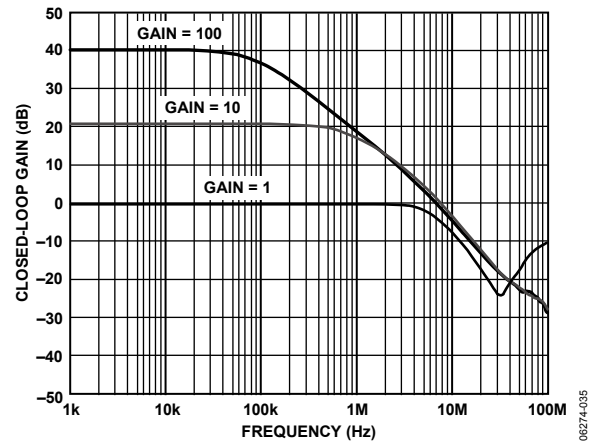


Figure 36. Closed-Loop Gain vs. Frequency, $\pm 5 V \leq V_S \leq \pm 15 V$

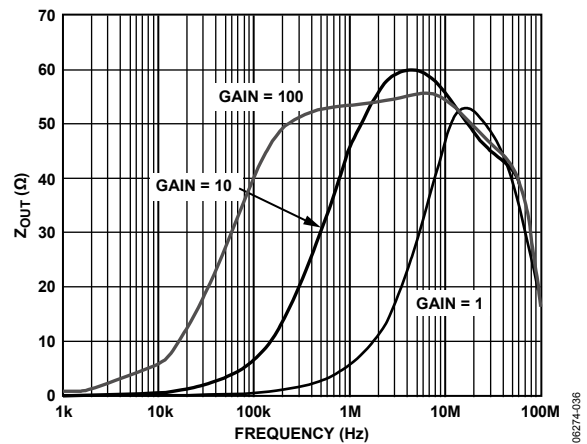


Figure 37. Closed-Loop Output Impedance vs. Frequency, $\pm 5 V \leq V_S \leq \pm 15 V$

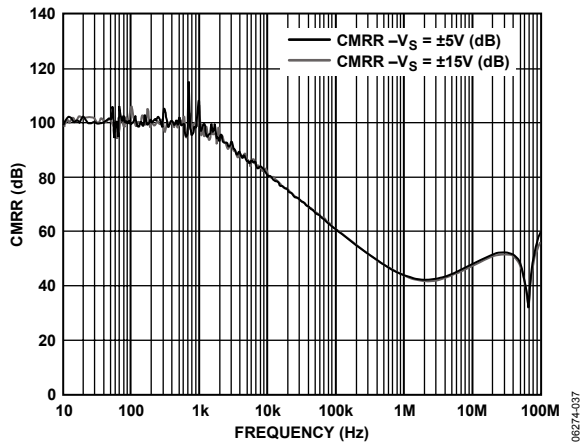


Figure 38. Common-Mode Rejection Ratio vs. Frequency

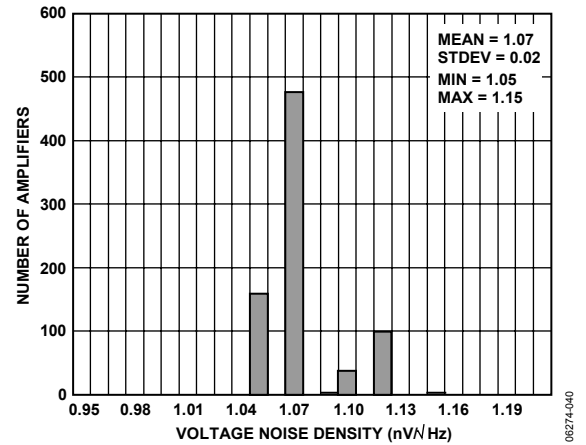


Figure 41. Voltage Noise Density @ 1 kHz, $\pm 5 V \leq V_s \leq \pm 15 V$

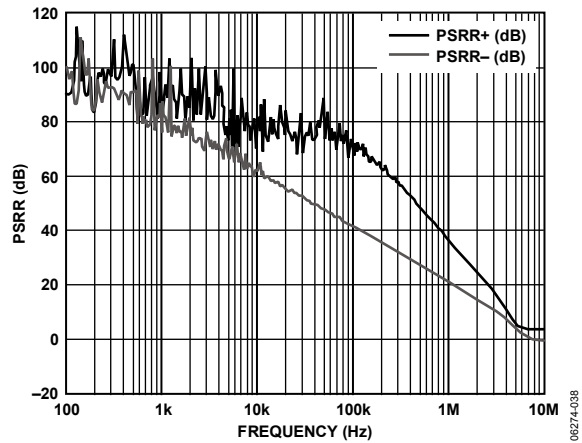


Figure 39. Power Supply Rejection Ratio vs. Frequency, $\pm 5 V \leq V_s \leq \pm 15 V$

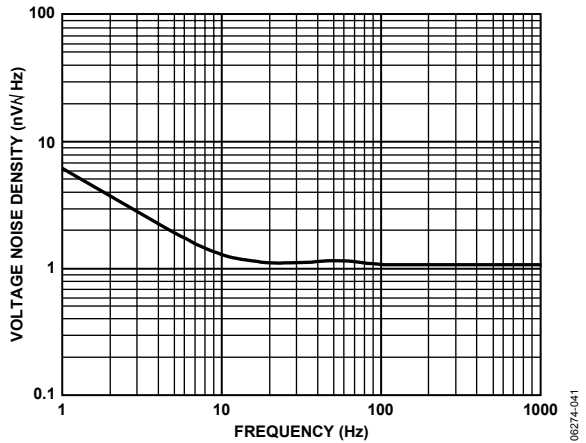


Figure 42. Voltage Noise Density vs. Frequency, $\pm 5 V \leq V_s \leq \pm 15 V$

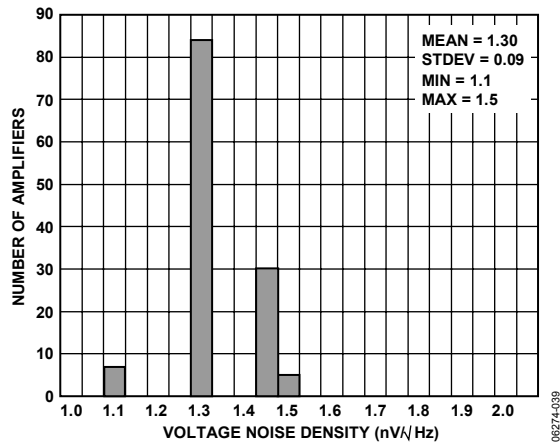


Figure 40. Voltage Noise Density @ 10 Hz, $\pm 5 V \leq V_s \leq \pm 15 V$

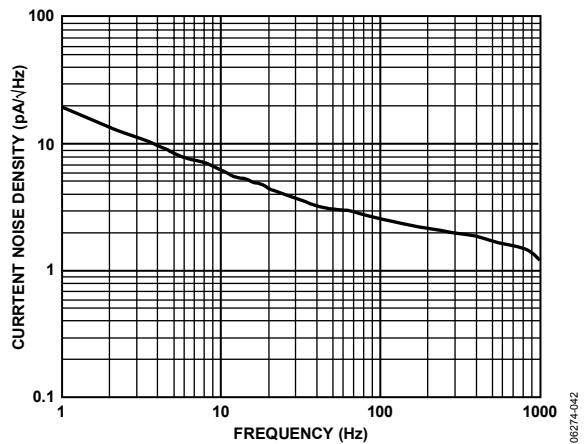


Figure 43. Current Noise Density vs. Frequency, $\pm 5 V \leq V_s \leq \pm 15 V$

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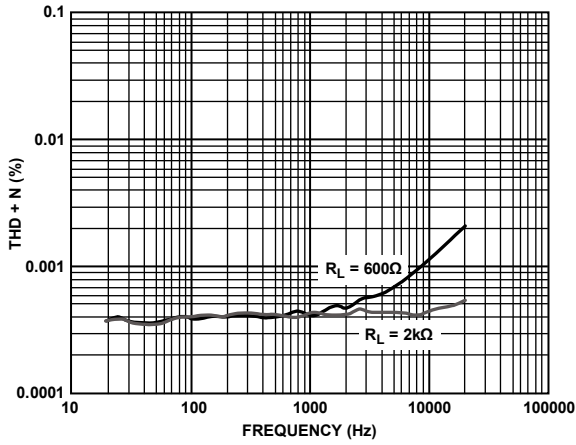


Figure 44. Total Harmonic Distortion + Noise vs. Frequency, $V_S = \pm 15\text{ V}$, $V_{IN} = 3\text{ V rms}$

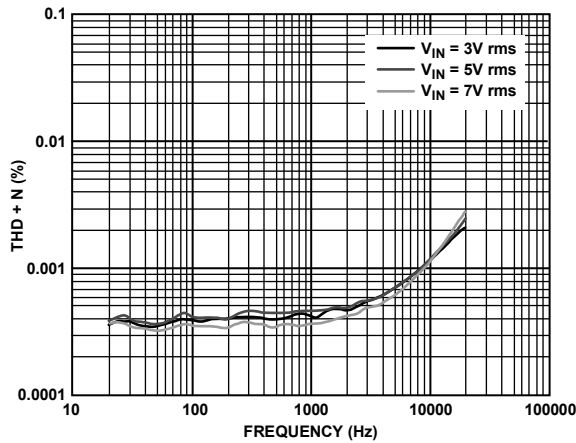


Figure 45. Total Harmonic Distortion + Noise vs. Frequency

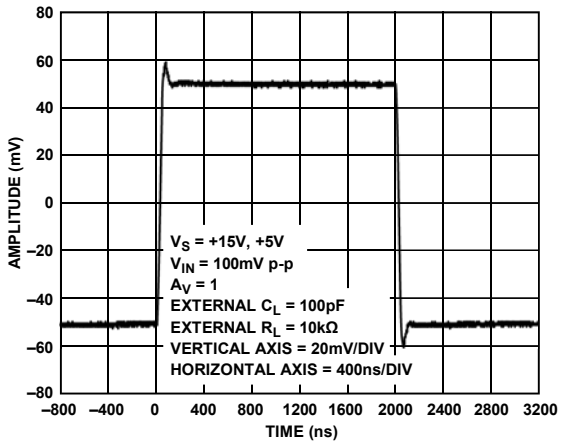


Figure 46. Small Signal Response

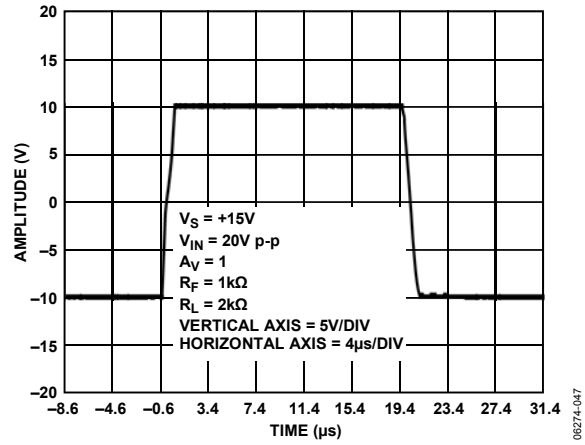


Figure 47. Large Signal Response

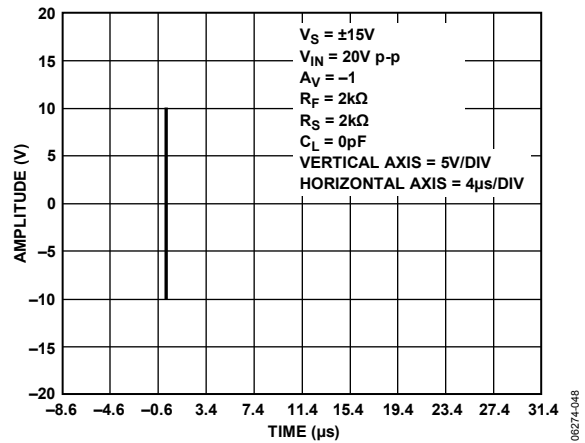


Figure 48. Large Signal Response

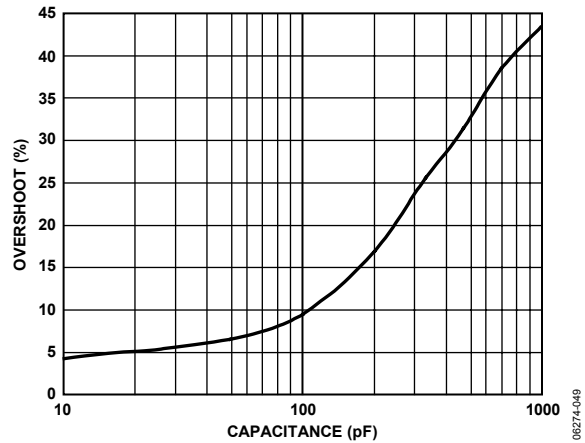


Figure 49. Overshoot vs. Capacitance, $\pm 5\text{ V} \leq V_S \leq \pm 15\text{ V}$, $A_V = 1$, $R_L = 10\text{ k}\Omega$

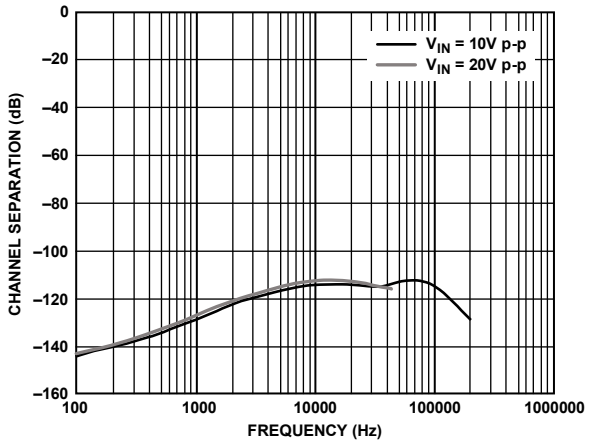


Figure 50. Channel Separation vs. Frequency, $V_S = \pm 15V$, $A_V = 100$, $R_L = 1k\Omega$

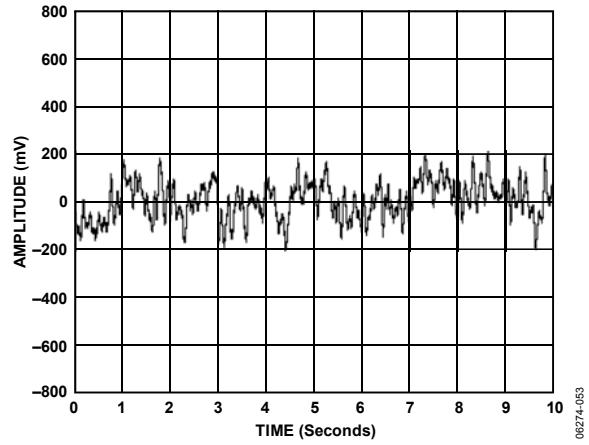
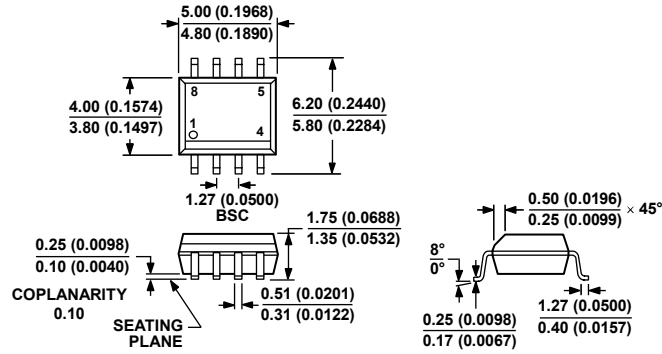


Figure 51. Peak-to-Peak Noise, $V_S \leq \pm 15V$, $A_V = 1M$, $R_L = 10k\Omega$

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OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AA
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
 (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

060916-A

Figure 52. 8-Lead Standard Small Outline Package [SOIC_N]
 Narrow Body (R-8)
 Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD8599ARZ ¹	-40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8
AD8599ARZ-REEL ¹	-40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8
AD8599ARZ-REEL7 ¹	-40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8

¹ Z = Pb-free part.

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AD8599

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