



Low Cost, 24 MHz, Rail-to-Rail, Quad Amplifiers

AD8648

FEATURES

- Low offset voltage: 2.5 mV max
- Single-supply operation: 2.7 V to 5.5 V
- Low noise: 6 nV/ $\sqrt{\text{Hz}}$
- Wide bandwidth: 24 MHz
- Slew rate: 12 V/ μs
- High output current: 150 mA
- No phase reversal
- Low input bias current: 1 pA
- Low supply current: 2 mA max
- Unity-gain stable

APPLICATIONS

- Barcode scanners
- Battery-powered instrumentation
- Multipole filters
- Sensors
- ASIC input or output amplifiers
- Audio
- Photodiode amplification

GENERAL DESCRIPTION

The AD8648 is a quad, rail-to-rail, input and output, single-supply amplifier featuring low offset voltage, wide signal bandwidth, and low input voltage and current noise.

The combination of 24 MHz bandwidth, low offset, low noise, and very low input bias current makes these amplifiers useful in a wide variety of applications. Filters, integrators, photodiode amplifiers, and high impedance sensors all benefit from the combination of performance features. AC applications benefit from the wide bandwidth and low distortion. The AD8648 family offers high output drive capability, which is excellent for audio line drivers and other low impedance applications.

PIN CONFIGURATIONS

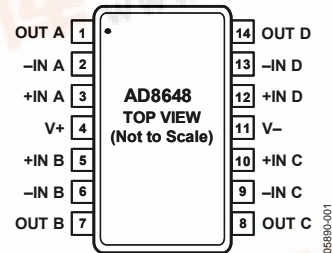


Figure 1. 14-Lead TSSOP (RU-14)

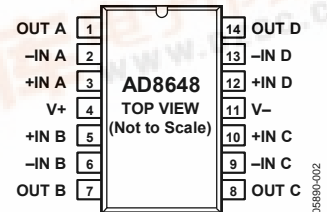


Figure 2. 14-Lead SOIC (R-14)

Applications for the part include portable and low powered instrumentation, audio amplification for portable devices, portable phone headsets, bar code scanners, and multipole filters. The ability to swing rail to rail at both the input and output enables designers to buffer CMOS ADCs, DACs, ASICs, and other wide output swing devices in single-supply systems.



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REVISION HISTORY

1/06—Rev 0: Initial Version

SPECIFICATIONS

$V_{DD} = 5.0\text{ V}$, $V_{CM} = V_{DD}/2$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	$V_{CM} = 0\text{ V to }5\text{ V}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.7	2.5	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		2.0	3.2	$\mu\text{V}/^\circ\text{C}$
Input Bias Current	I_B	$-40^\circ\text{C} < T_A < +85^\circ\text{C}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.2	1	pA
Input Offset Current	I_{OS}	$-40^\circ\text{C} < T_A < +85^\circ\text{C}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.1	0.5	pA
Input Voltage Range	V_{CM}		0		5	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = 0\text{ V to }5.0\text{ V}$	67	84		dB
Large-Signal Voltage Gain	A_{VO}	$R_L = 2\text{ k}\Omega$, $V_O = 0.5\text{ V to }4.5\text{ V}$	160	700		V/mV
Input Capacitance	C_{DIFF} C_{CM}			2.5		pF
				6.7		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	$I_{OUT} = 1\text{ mA}$ $I_{OUT} = 10\text{ mA}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	4.98 4.87 4.70	4.99 4.92		V V V
Output Voltage Low	V_{OL}	$I_{OUT} = 1\text{ mA}$ $I_{OUT} = 10\text{ mA}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		8.4 78	20 145	mV mV mV
Short-Circuit Output Current	I_{SC}			± 150		mA
Closed-Loop Output Impedance	Z_{OUT}	At 1 MHz, $A_V = 1$		3		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_{DD} = 2.7\text{ V to }5.5\text{ V}$	63	80		dB
Supply Current per Amplifier	I_{SY}	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		1.8	2.0	mA
					2.5	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	$R_L = 2\text{ k}\Omega$		12		V/ μs
Settling Time	t_s	To 0.01%		0.5		μs
Gain Bandwidth Product	GBP			24		MHz
Phase Margin	Φ_M			74		Degrees
NOISE PERFORMANCE						
Peak-to-Peak Noise	e_n p-p	0.1 Hz to 10 Hz		2.4		μV
Voltage Noise Density	e_n	$f = 1\text{ kHz}$ $f = 10\text{ kHz}$		8		$\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$
Channel Separation	CS	$f = 10\text{ kHz}$ $f = 100\text{ kHz}$		-115		dB
				-110		dB

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$V_{DD} = 2.7\text{ V}$, $V_{CM} = V_{DD}/2$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	$V_{CM} = 0\text{ V to } 2.7\text{ V}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.7	2.5	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		1.8	7.0	$\mu\text{V}/^\circ\text{C}$
Input Bias Current	I_B	$-40^\circ\text{C} < T_A < +85^\circ\text{C}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.2	1	pA
Input Offset Current	I_{OS}	$-40^\circ\text{C} < T_A < +85^\circ\text{C}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.1	0.5	pA
Input Voltage Range	V_{CM}		0		2.7	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = 0\text{ V to } 2.7\text{ V}$	62	79		dB
Large-Signal Voltage Gain	A_{VO}	$R_L = 2\text{ k}\Omega$, $V_O = 0.5\text{ V to } 2.2\text{ V}$	60	130		V/mV
Input Capacitance	C_{DIFF} C_{CM}			2.5		pF
				7.8		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	$I_{OUT} = 1\text{ mA}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	2.65 2.60	2.69		V V
Output Voltage Low	V_{OL}	$I_{OUT} = 1\text{ mA}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		11	25 30	mV mV
Short-Circuit Output Current	I_{SC}			± 50		mA
Closed-Loop Output Impedance	Z_{OUT}	At 1 MHz, $A_V = 1$		3		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_{DD} = 2.7\text{ V to } 5.5\text{ V}$	63	80		dB
Supply Current per Amplifier	I_{SY}	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		1.7	2.0 2.5	mA mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	$R_L = 2\text{ k}\Omega$		12		V/ μs
Settling Time	t_s	To 0.01%		0.3		μs
Gain Bandwidth Product	GBP			22		MHz
Phase Margin	Φ_M			52		Degrees
NOISE PERFORMANCE						
Peak-to-Peak Noise	$e_n\text{ p-p}$	0.1 Hz to 10 Hz		2.1		μV
Voltage Noise Density	e_n	$f = 1\text{ kHz}$ $f = 10\text{ kHz}$		8 6		nV/ $\sqrt{\text{Hz}}$ nV/ $\sqrt{\text{Hz}}$
Channel Separation	CS	$f = 10\text{ kHz}$ $f = 100\text{ kHz}$		-115 -110		dB dB

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	6 V
Input Voltage	GND to V_{DD}
Differential Input Voltage	± 3 V
Output Short Circuit to GND	Indefinite
Storage Temperature Range	-65°C to $+150^{\circ}\text{C}$
Operating Temperature Range	-40°C to $+125^{\circ}\text{C}$
Lead Temperature (Soldering, 60 sec)	300°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
14-Lead SOIC (R)	120	36	$^{\circ}\text{C}/\text{W}$
14-Lead TSSOP (RU)	180	35	$^{\circ}\text{C}/\text{W}$

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



TYPICAL PERFORMANCE CHARACTERISTICS

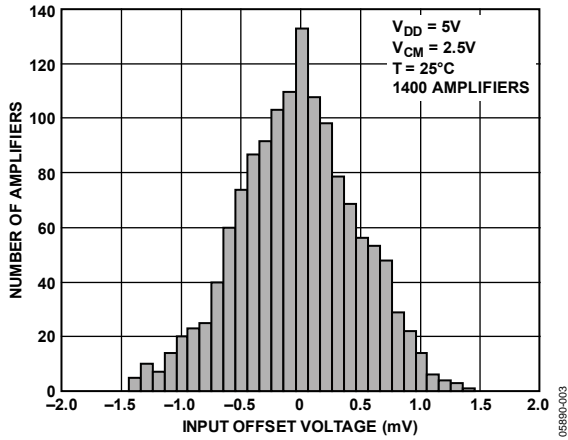


Figure 3. Input Offset Voltage Distribution

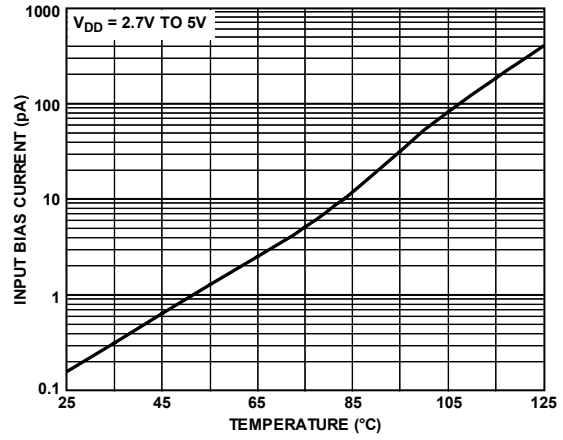


Figure 6. Input Bias Current vs. Temperature

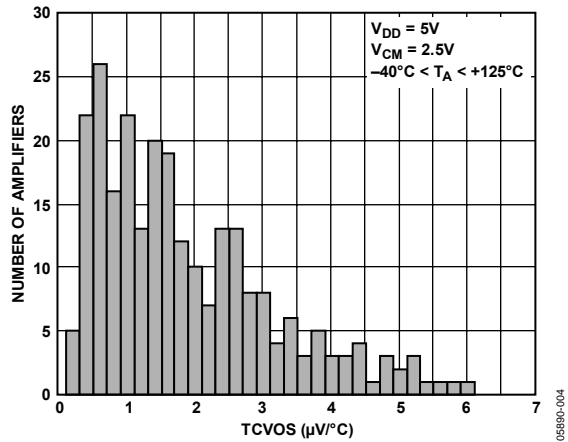


Figure 4. Vos Drift (TCVos) Distribution

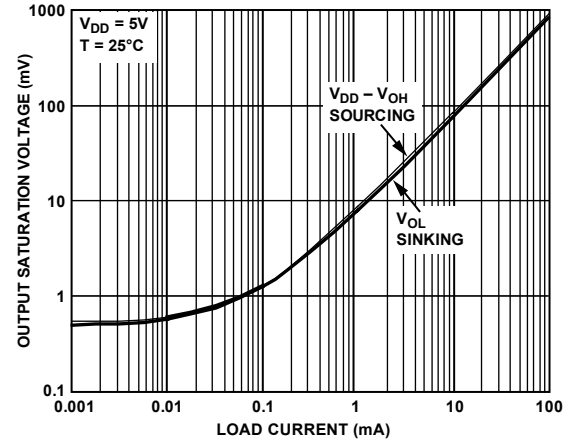


Figure 7. Output Saturation Voltage vs. Load Current

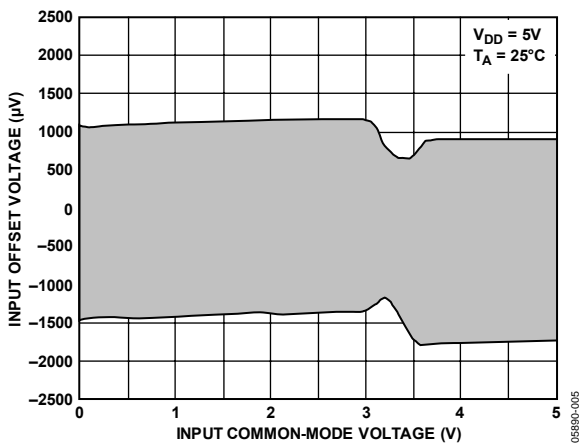


Figure 5. Input Offset Voltage vs. Input Common-Mode Voltage

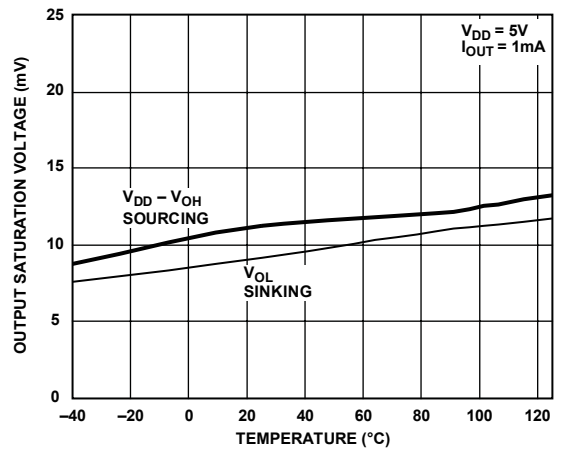


Figure 8. Output Saturation Voltage vs. Temperature

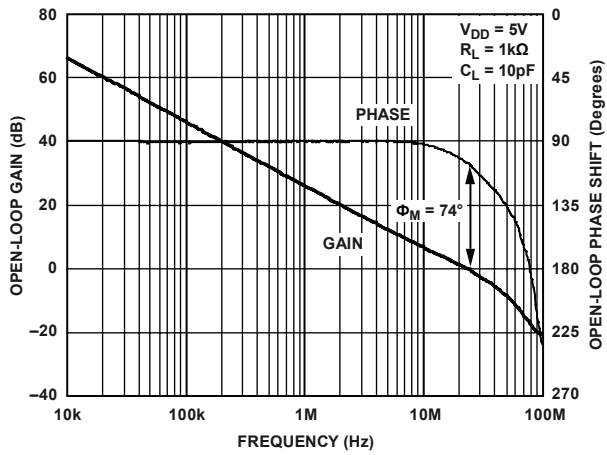


Figure 9. Open-Loop Gain and Phase vs. Frequency

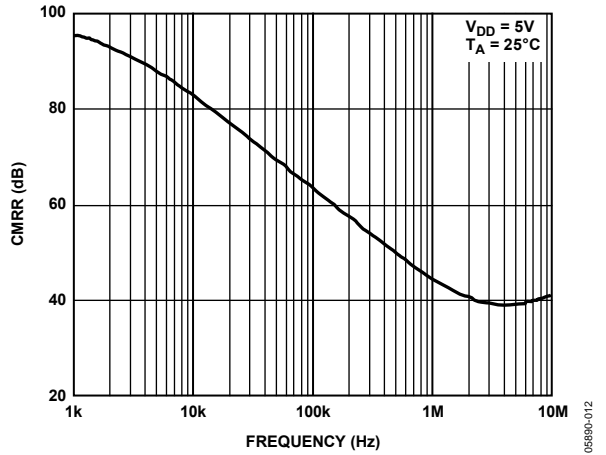


Figure 12. Common-Mode Rejection Ratio vs. Frequency

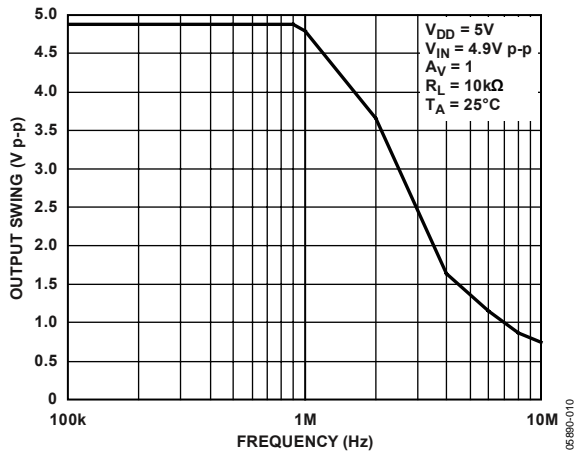


Figure 10. Maximum Output Swing vs. Frequency

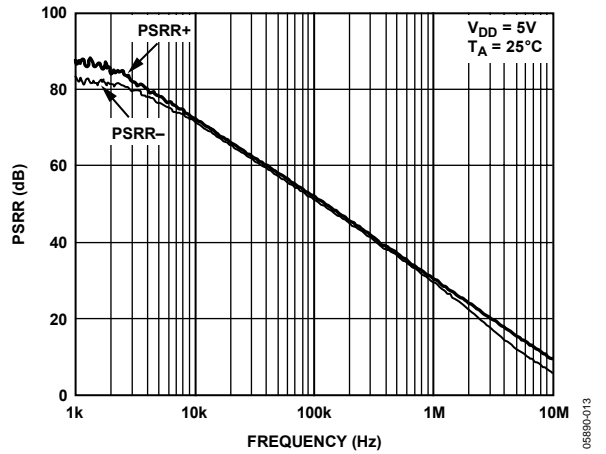


Figure 13. Power Supply Rejection Ratio vs. Frequency

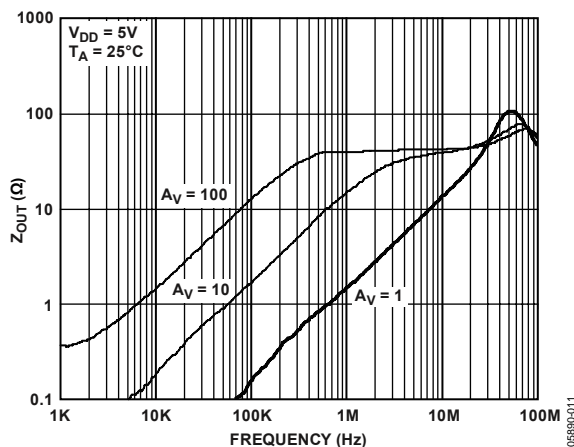


Figure 11. Closed-Loop Output Impedance vs. Frequency

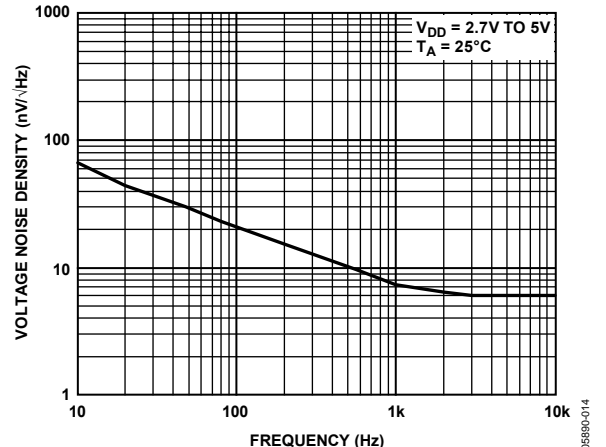


Figure 14. Voltage Noise Density vs. Frequency

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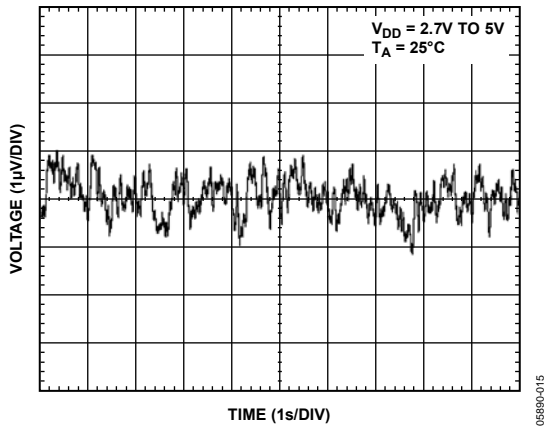


Figure 15. 0.1 Hz to 10 Hz Voltage Noise

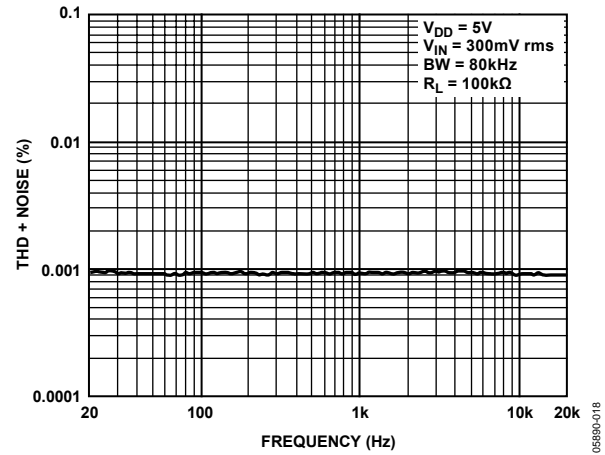


Figure 18. THD + Noise vs. Frequency

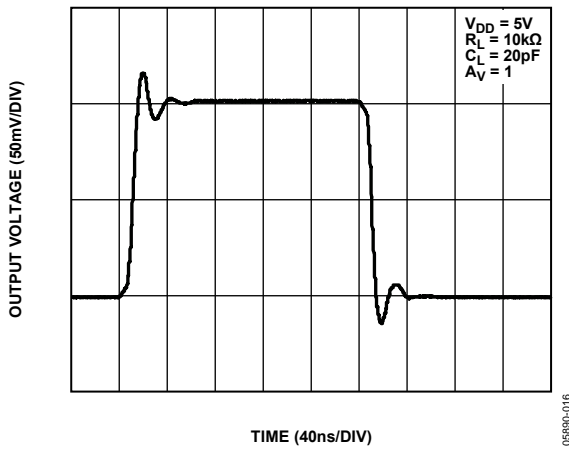


Figure 16. Small-Signal Transient Response

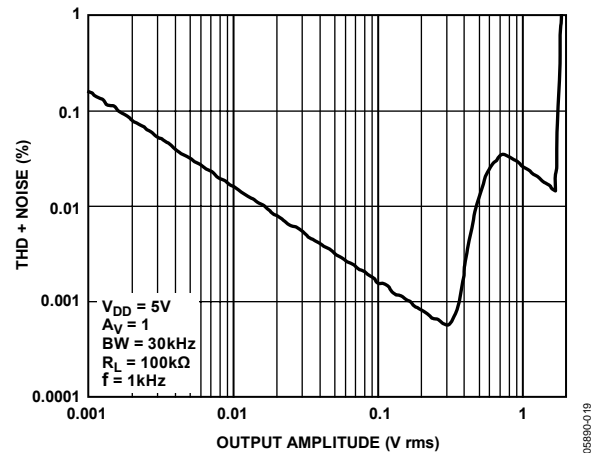


Figure 19. THD + Noise vs. Output Amplitude

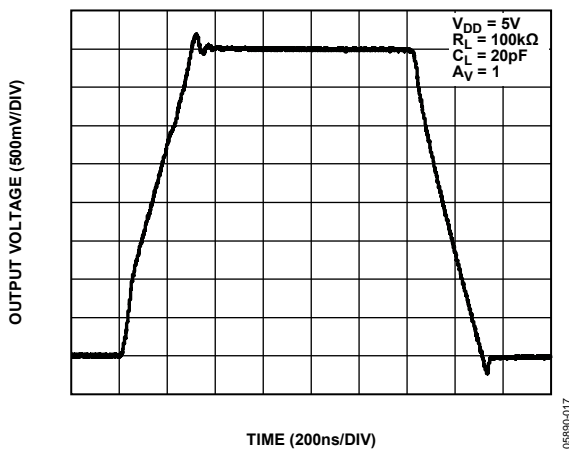


Figure 17. Large-Signal Transient Response

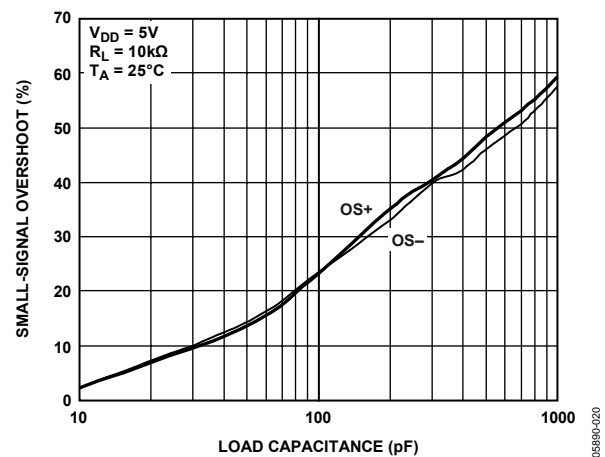


Figure 20. Small-Signal Overshoot vs. Load Capacitance

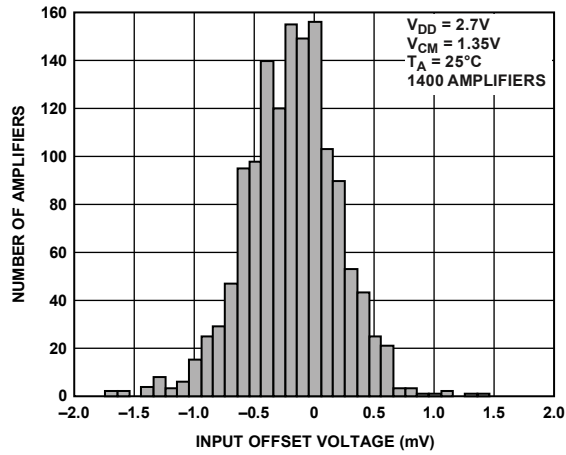


Figure 21. Input Offset Voltage Distribution

05890-021

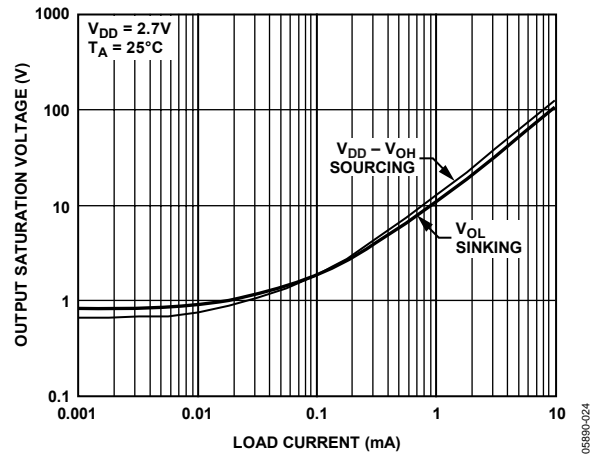


Figure 24. Output Saturation Voltage vs. Load Current

05890-024

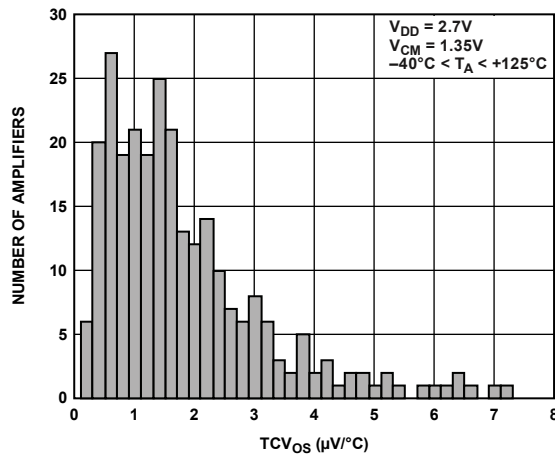


Figure 22. Vos Drift (TCVos) Distribution

05890-022

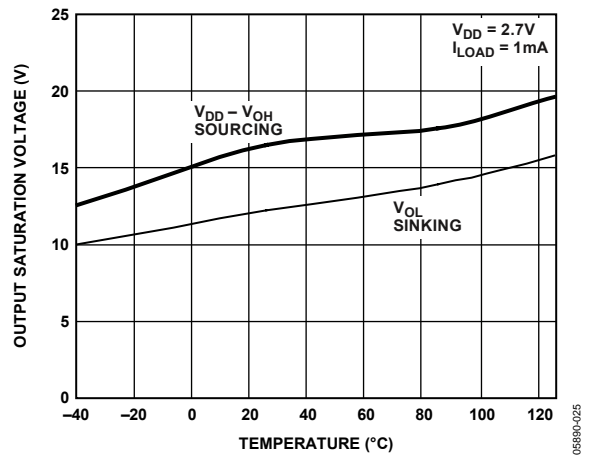


Figure 25. Output Saturation Voltage vs. Temperature

05890-025

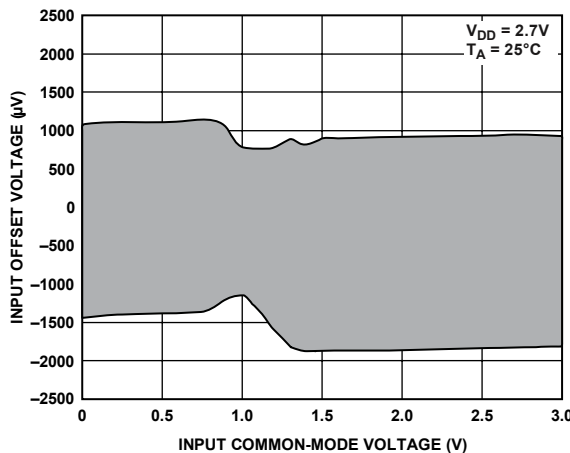


Figure 23. Input Offset Voltage vs. Input Common-Mode Voltage

05890-023

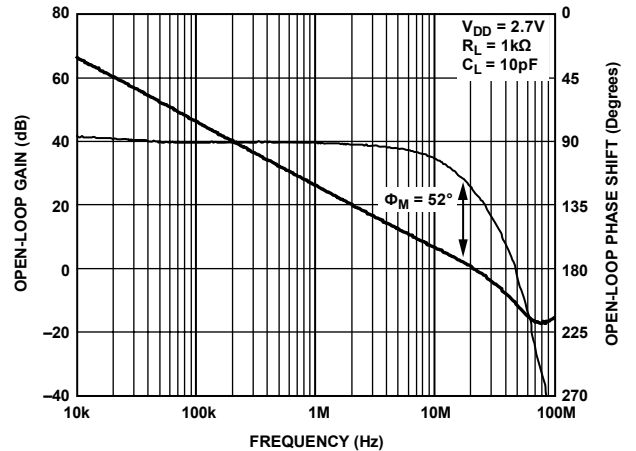


Figure 26. Open-Loop Gain and Phase vs. Frequency

05890-026

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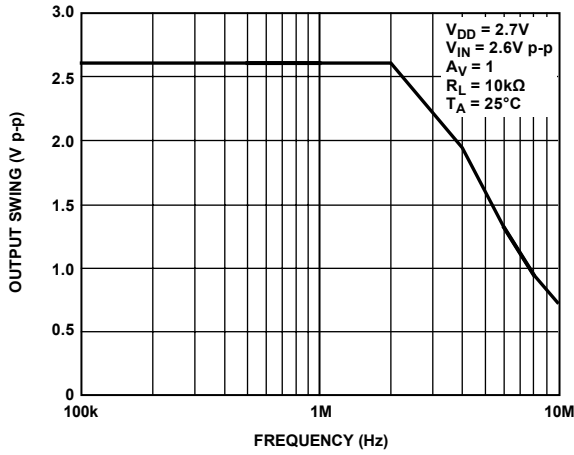


Figure 27. Maximum Output Swing vs. Frequency

05890-027

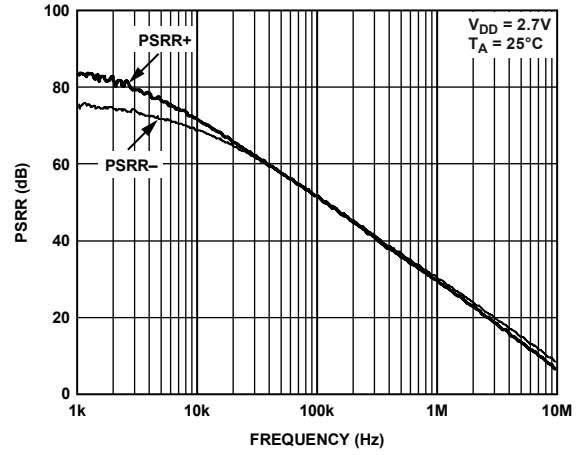


Figure 30. Power Supply Rejection Ratio vs. Frequency

05890-030

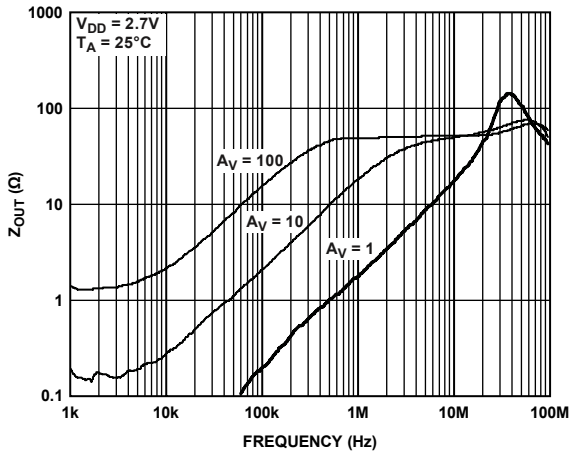


Figure 28. Closed-Loop Output Impedance vs. Frequency

05890-028

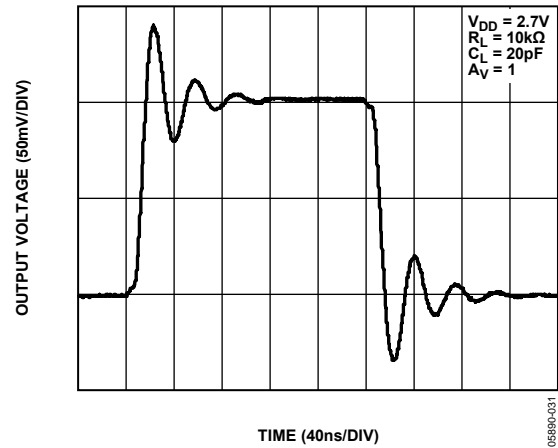


Figure 31. Small-Signal Transient Response

05890-031

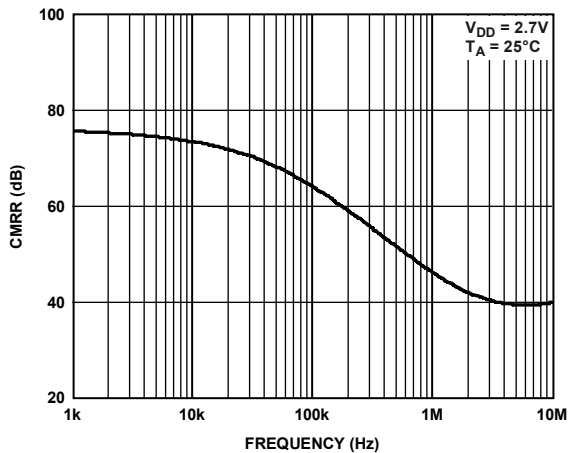


Figure 29. Common-Mode Rejection Ratio vs. Frequency

05890-029

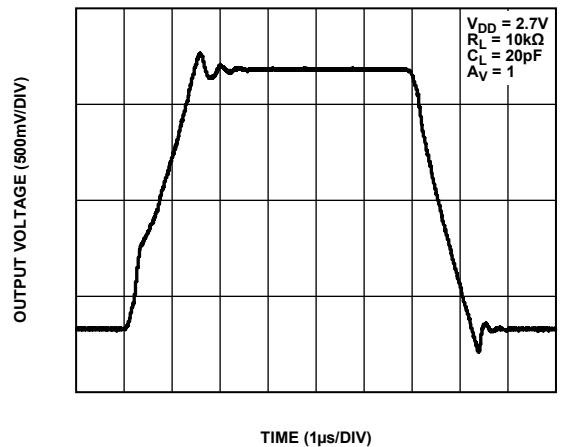


Figure 32. Large-Signal Transient Response

05890-032

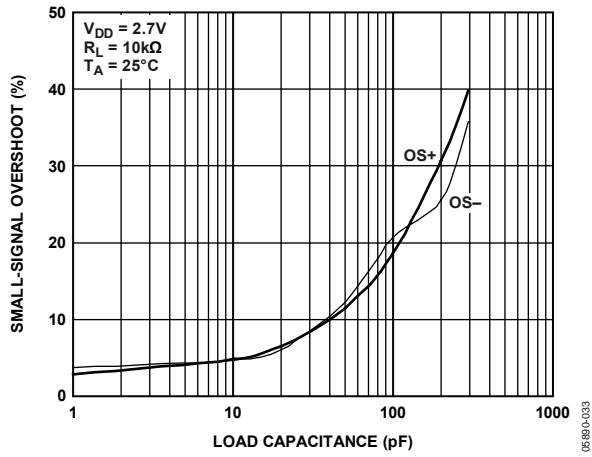


Figure 33. Small-Signal Overshoot vs. Load Capacitance

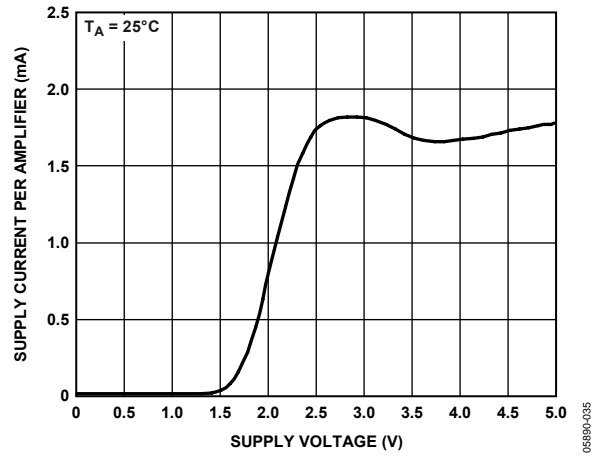


Figure 35. Supply Current per Amplifier vs. Supply Voltage

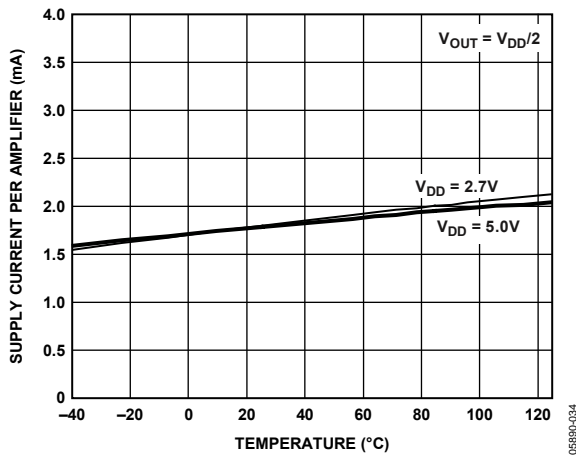


Figure 34. Supply Current per Amplifier vs. Temperature

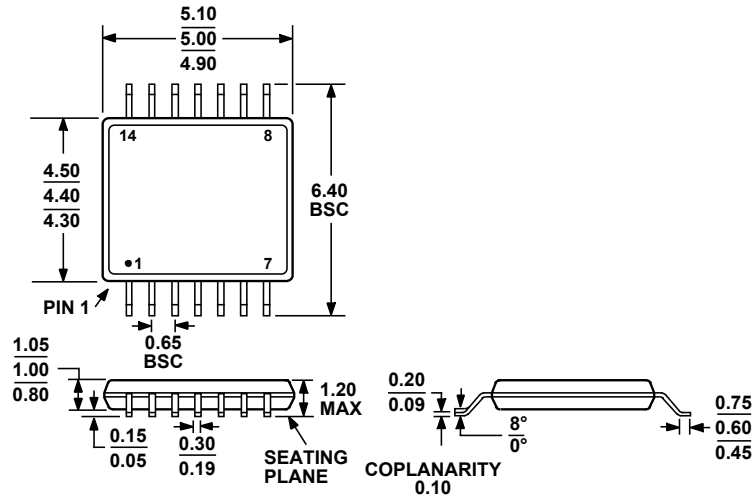
068890-033

068890-035

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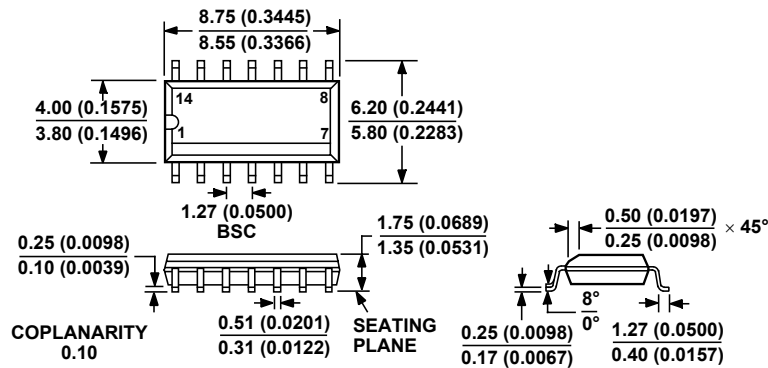
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AB-1

Figure 36. 14-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-14)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-012-AB

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 37. 14-Lead Standard Small Outline Package [SOIC_N]
Narrow Body (R-14)

Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD8648ARZ ¹	-40°C to +125°C	14-Lead SOIC_N	R-14
AD8648ARZ-REEL ¹	-40°C to +125°C	14-Lead SOIC_N	R-14
AD8648ARZ-REEL7 ¹	-40°C to +125°C	14-Lead SOIC_N	R-14
AD8648ARUZ ¹	-40°C to +125°C	14-Lead TSSOP	RU-14
AD8648ARUZ-REEL ¹	-40°C to +125°C	14-Lead TSSOP	RU-14

¹ Z = Pb-free part.