ANALOG DEVICES

130 μV Maximum Offset Voltage Op Amp in TSOT

AD8677

FEATURES

Low offset voltage: 130 μV max
Input offset drift: 1.5 μV/°C max
Low noise: 0.25 μV p-p
High gain, CMRR and PSRR: 115 dB min
Low supply current: 1.1 mA
Wide supply voltage range: ±4 V to ±18 V operation

APPLICATIONS

Medical and industrial instrumentation
Sensors and controls
- **Thermocouple**
- **RTDs**
- **Strain bridges**
- **Shunt current measurements**

Precision filters

GENERAL DESCRIPTION

The AD8677 is the next generation of precision, ultralow offset amplifiers. It builds on the high performance of the OP07 and integrates lower power (1.1 mA typical), lower input bias current (±1 nA maximum), and higher CMRR/PSRR (130 dB) in the small TSOT package. Operation is fully specified from ±5 V to ±15 V supply.

The AD8677 provides higher accuracy than industry-standard OP07-type amplifiers due to Analog Devices' iPolar™ process, which supports enhanced performance in a smaller footprint. These performance enhancements include wider output swing, lower power, and higher CMRR (common-mode rejection ratio) and PSRR (power supply rejection ratio). The AD8677 maintains stability of offsets and gain virtually regardless of variations in time or temperature. Excellent linearity and gain accuracy can be maintained at high closed-loop gains.

The AD8677 is fully specified over the extended industrial temperature range of −40°C to +125°C. The AD8677 amplifier is available in the tiny, 5-lead TSOT and the popular 8-lead, narrow SOIC lead-free packages.

PIN CONFIGURATIONS

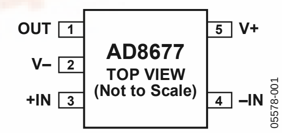

Figure 1. 5-Lead TSOT (UJ-5)

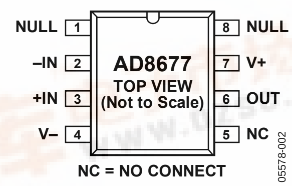

Figure 2. 8-Lead SOIC_N (R-8)

Rev. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com

TABLE OF CONTENTS

REVISION HISTORY

11/05—Revision 0: Initial Version

SPECIFICATIONS

V_S = ±5.0 V, T_A = +25°C, unless otherwise specified.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			40	130	μV
		−40°C ≤ TA ≤ +125°C			350	μV
Input Bias Current	I_B			0.2	1	nA
		−40°C ≤ TA ≤ +125°C			1	nA
Input Offset Current	I_{OS}			0.1	1	nA
		−40°C ≤ TA ≤ +125°C			1	nA
Input Voltage Range			−3.5		+3.5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±3 V	120	127		dB
		−40°C ≤ TA ≤ +125°C	120			dB
Open-Loop Gain	A_{VO}	R_L = 2 kΩ to ground, V_O = ±3 V	1000	10000		V/mV
		−40°C ≤ TA ≤ +125°C	1000			V/mV
	$\Delta V_{OS}/\Delta T$	−40°C ≤ TA ≤ +125°C		0.5	1.4	μV/°C
OUTPUT CHARACTERISTICS						
Output Voltage Swing	V_{OUT}	R_L = 10 kΩ to ground	±3.95	±4.1		V
		−40°C ≤ TA ≤ +125°C	±3.95			V
		R_L = 2 kΩ to ground	±3.9	±4		V
		−40°C ≤ TA ≤ +125°C	±3.9			V
Short-Circuit Limit	I_{SC}			27		mA
Output Current	I_O	V_O = 3.5 V		15		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±4.0 V to ±18.0 V	115	130		dB
		−40°C ≤ TA ≤ +125°C	110			dB
Supply Current/Amplifier	I_{SY}	V_O = 0 V		1.1	1.25	mA
		−40°C ≤ TA ≤ +125°C			1.7	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ		0.2		V/μs
Gain Bandwidth Product	GBP			0.6		MHz
Phase Margin				80		Degrees
NOISE PERFORMANCE						
Voltage Noise	$e_{n\ p\text{-}p}$	0.1 Hz to 10 Hz		0.28		μV p-p
Voltage Noise Density	e_n	f = 1 kHz		10		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.074		pA/√Hz

$V_S = \pm 15$ V, $T_A = +25°C$, unless otherwise specified.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			45	130	μV
		−40°C ≤ TA ≤ +125°C			350	μV
Input Bias Current	I_B			0.2	1	nA
		−40°C ≤ TA ≤ +125°C			1	nA
Input Offset Current	I_{OS}			0.2	1	nA
		−40°C ≤ TA ≤ +125°C			1	nA
Input Voltage Range			−13.5		+13.5	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13.0$ V	120	140		dB
		−40°C ≤ TA ≤ +125°C	120			dB
Open Loop Gain	A_{VO}	$R_L = 2$ kΩ to ground, $V_O = \pm 11$ V	1000	10000		V/mV
		−40°C ≤ TA ≤ +125°C	1000			V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C ≤ TA ≤ +125°C		0.5	1.5	μV/°C
OUTPUT CHARACTERISTICS						
Output Voltage Swing	V_{OUT}	$R_L = 10$ kΩ to ground	±13.95	14		V
		−40°C ≤ TA ≤ +125°C	±13.9			V
		$R_L = 2$ kΩ to ground	±13.75	13.8		V
		−40°C ≤ TA ≤ +125°C	±13.7			V
Short Circuit Limit	I_{SC}			30		mA
Output Current	I_O	$V_O = 13.5$ V		15		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.0$ V to ± 18.0 V	115	130		dB
		−40°C ≤ TA ≤ +125°C	110			dB
Supply Current/Amplifier	I_{SY}	$V_O = 0$ V		1.1	1.3	mA
		−40°C ≤ TA ≤ +125°C			1.8	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	$R_L = 10$ kΩ		0.2		V/μs
Gain Bandwidth Product	GBP			0.6		MHz
Phase Margin				80		Degrees
NOISE PERFORMANCE						
Voltage Noise	$e_{n\,p\text{-}p}$	0.1 Hz to 10 Hz		0.25		μV p-p
Voltage Noise Density	e_n	f = 1 kHz		10		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.074		pA/√Hz

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Value
Supply Voltage	±18 V
Input Voltage	±V Supply
Differential Input Voltage	±0.7 V
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	
UJ-5, R Package	−65°C to +150°C
Operating Temperature Range	−40°C to +125°C
Junction Temperature Range	
RM, R Package	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	+300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4.

Package Type	θ_{JA}	θ_{JC}	Unit
5-Lead TSOT (UJ-5)	207	61	°C/W
8-Lead SOIC (R-8)	158	43	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

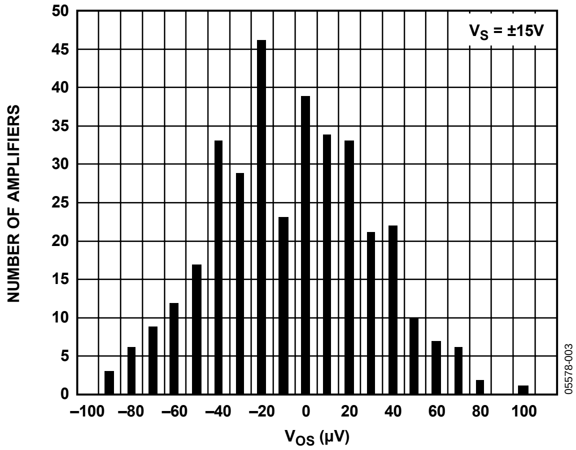

Figure 3. Input Offset Voltage Distribution

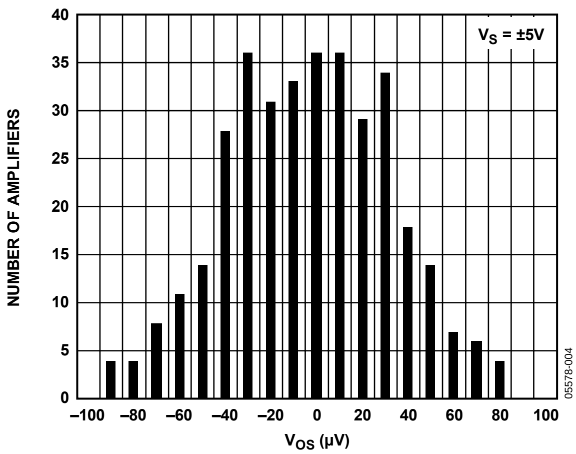

Figure 4. Input Offset Voltage Distribution

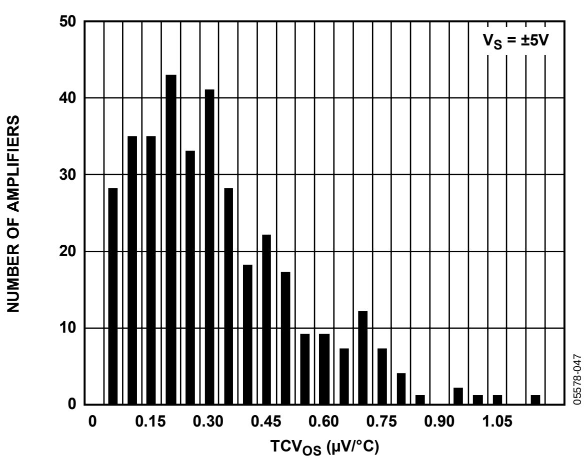

Figure 5. TCV$_{OS}$ vs. Number of Amplifiers

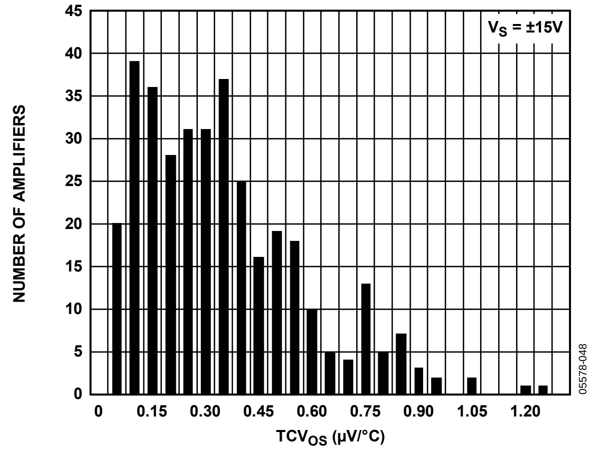

Figure 6. TCV$_{OS}$ vs. Number of Amplifiers

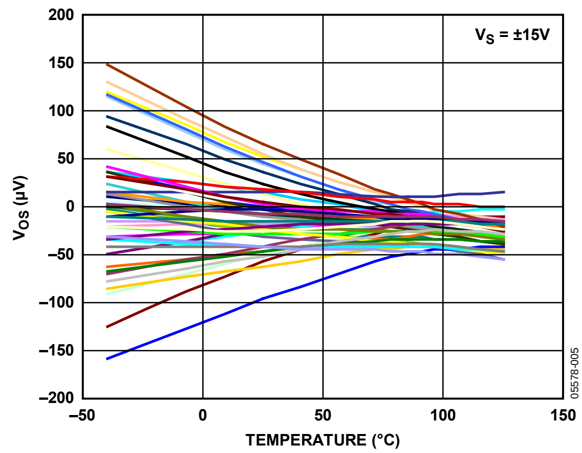

Figure 7. Offset Voltage vs. Temperature

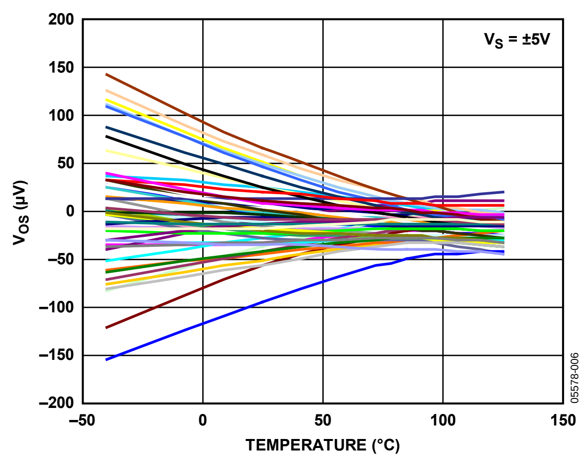

Figure 8. Offset Voltage vs. Temperature

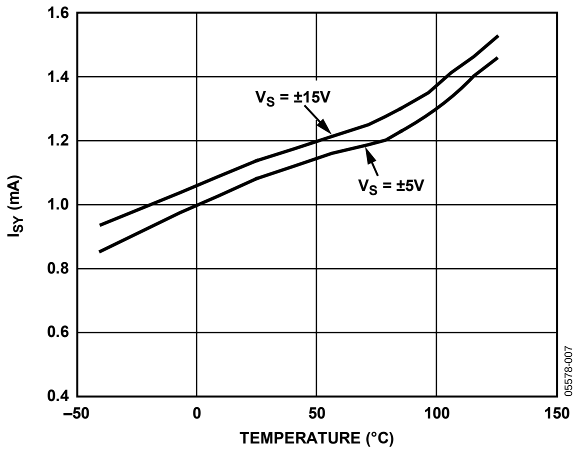

Figure 9. Supply Current vs. Temperature

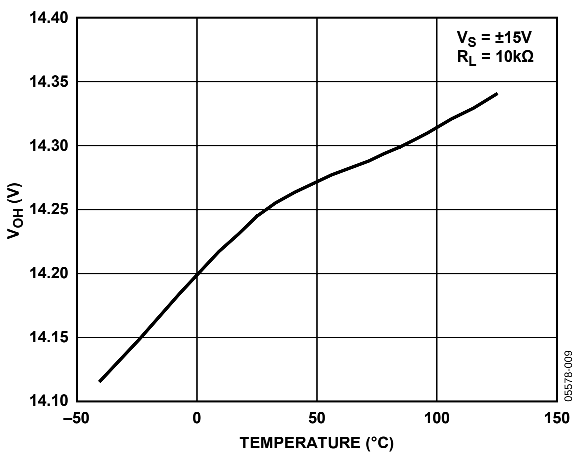

Figure 10. $+V_{OUT}$ vs. Temperature

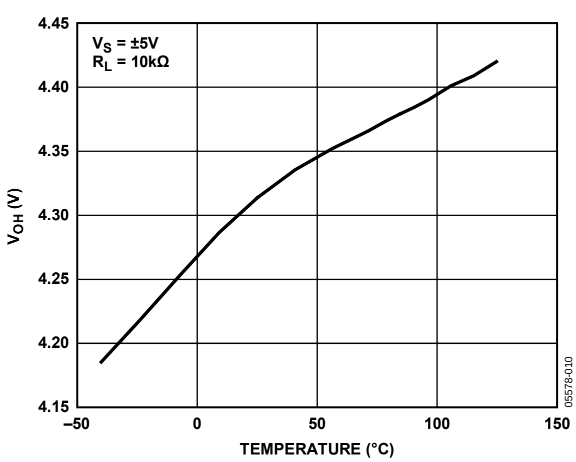

Figure 11. $+V_{OUT}$ vs. Temperature

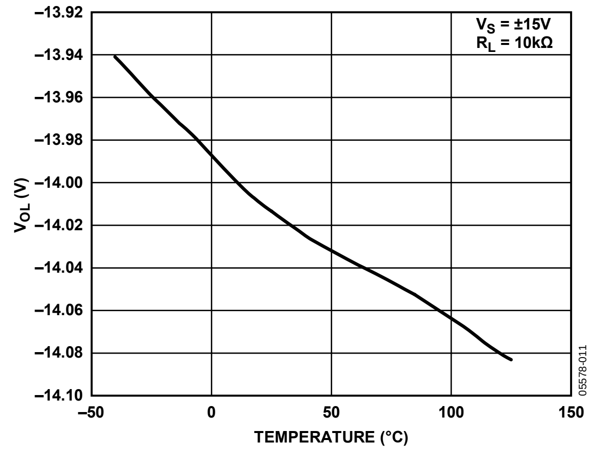

Figure 12. $-V_{OUT}$ vs. Temperature

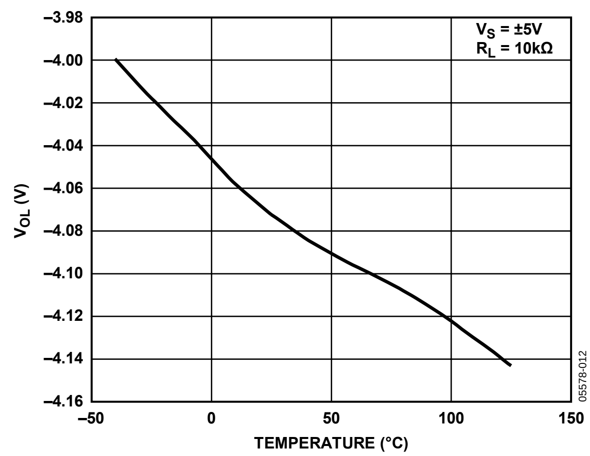

Figure 13. $-V_{OUT}$ vs. Temperature

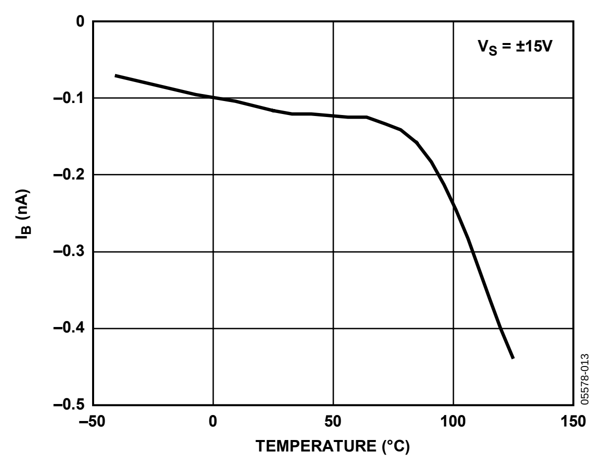

Figure 14. Input Bias Current vs. Temperature

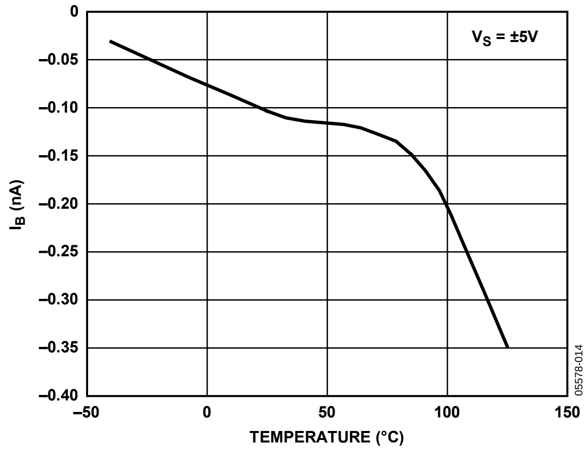

Figure 15. Input Bias Current vs. Temperature

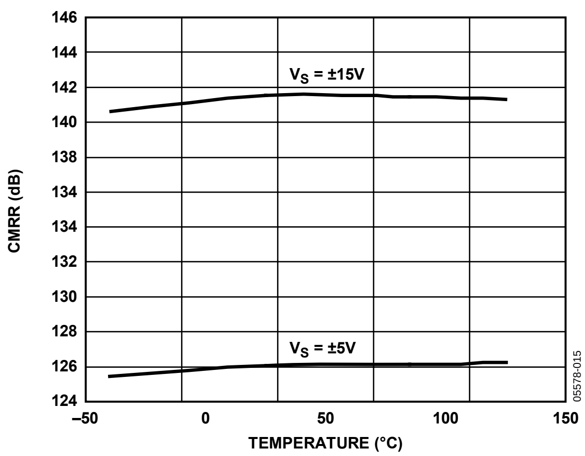

Figure 16. CMRR vs. Temperature

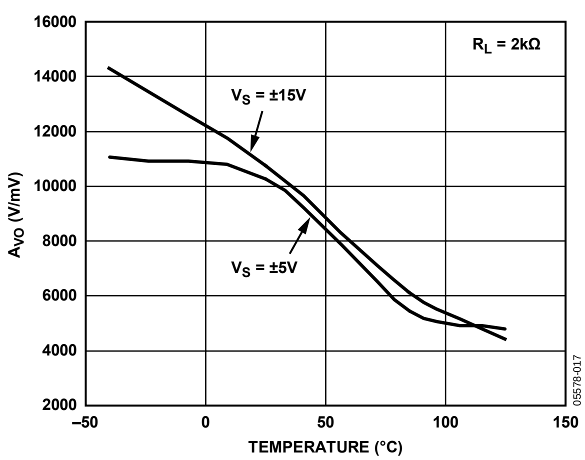

Figure 17. Open-Loop Gain vs. Temperature

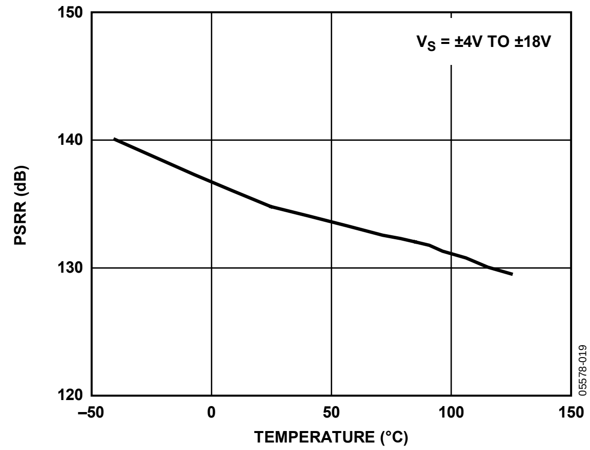

Figure 18. PSRR vs. Temperature

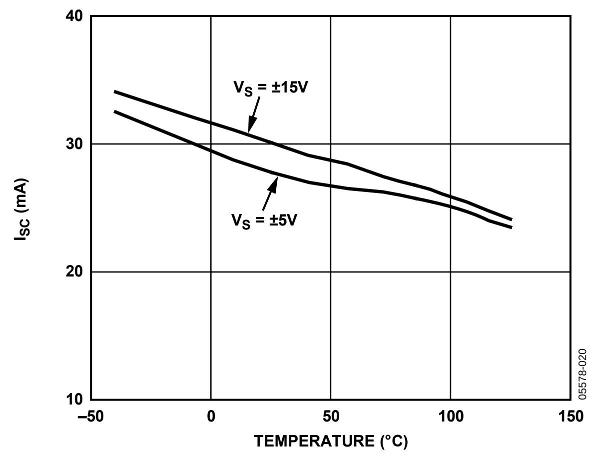

Figure 19. Short Circuit Current vs. Temperature

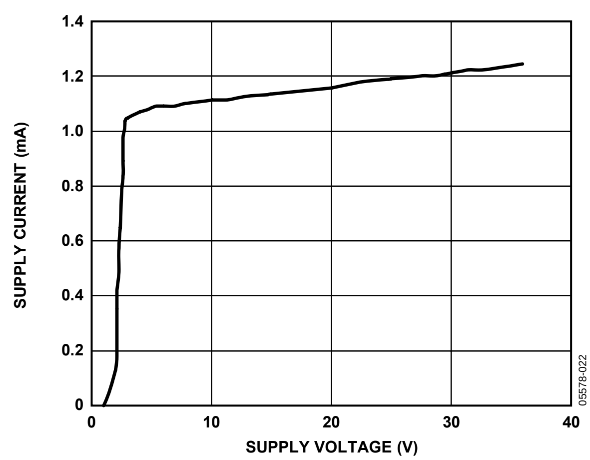

Figure 20. Supply Current vs. Total Supply Voltages

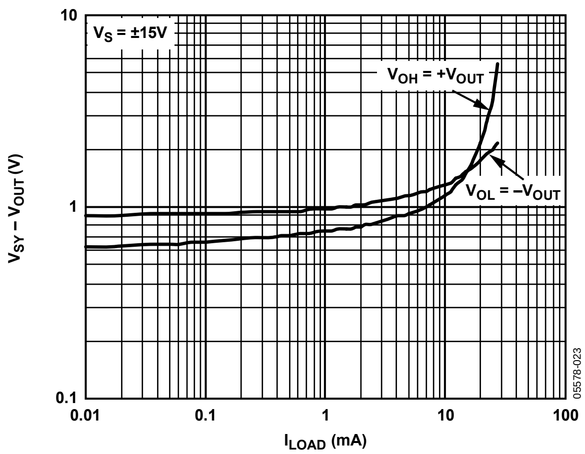

Figure 21. Output Voltage Swing vs. Load Current

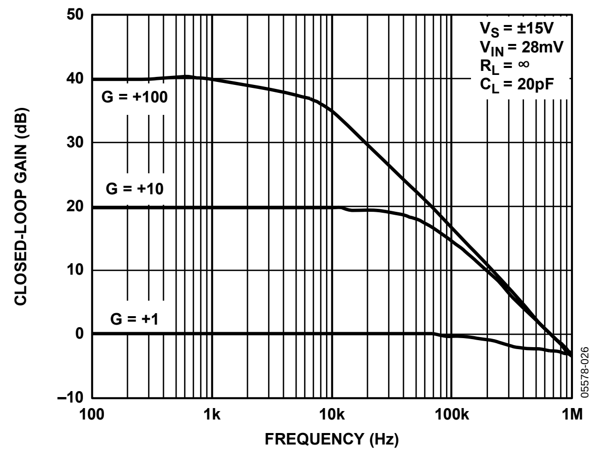

Figure 24. Closed-Loop Gain vs. Frequency

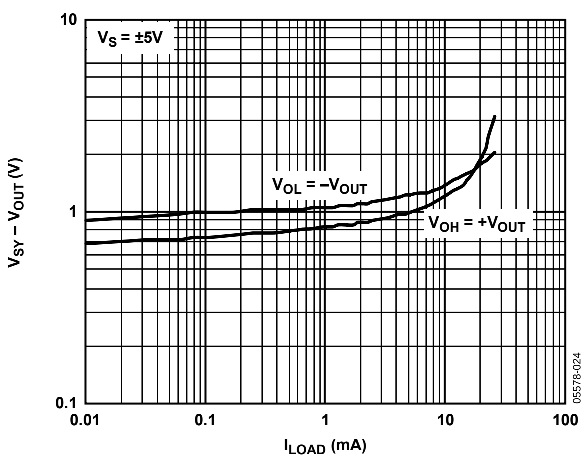

Figure 22. Output Voltage Swing vs. Load Current

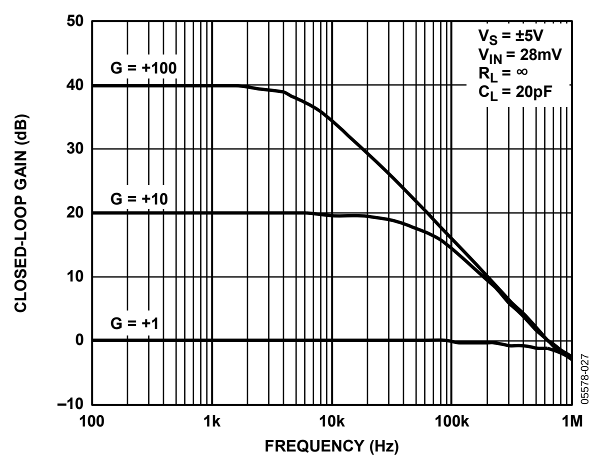

Figure 25. Closed-Loop Gain vs. Frequency

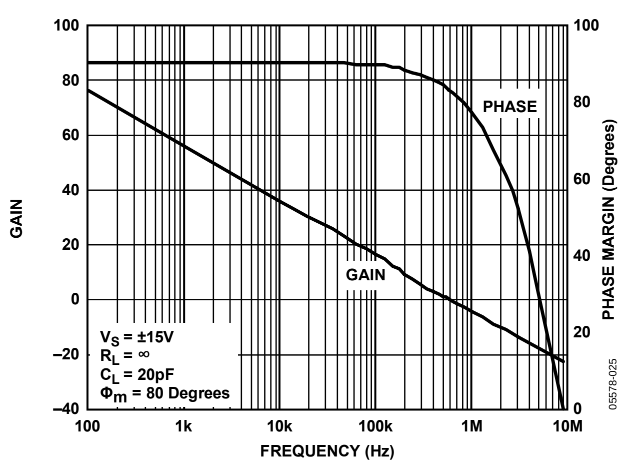

Figure 23. Open-Loop Gain and Phase vs. Frequency

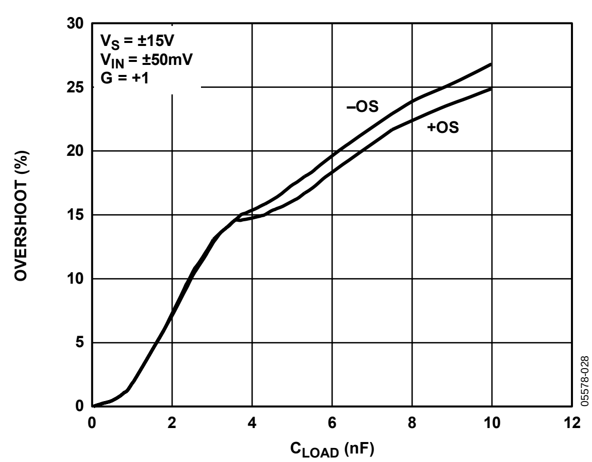

Figure 26. Overshoot vs. Capacitive Load

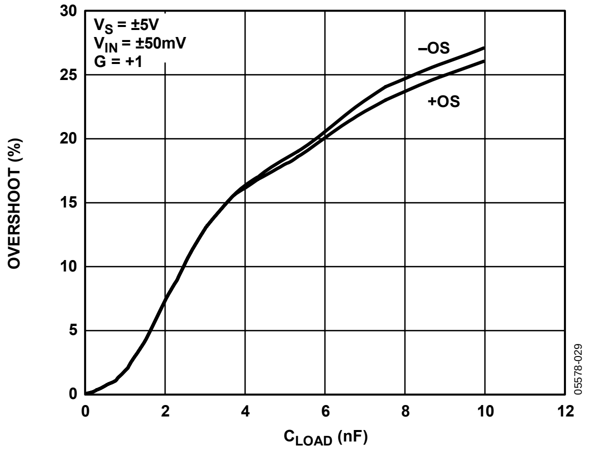

Figure 27. Overshoot vs. Capacitive Load

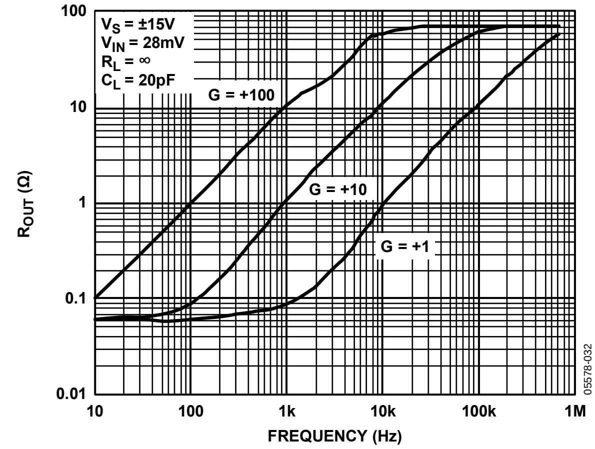

Figure 30. Output Impedance vs. Frequency

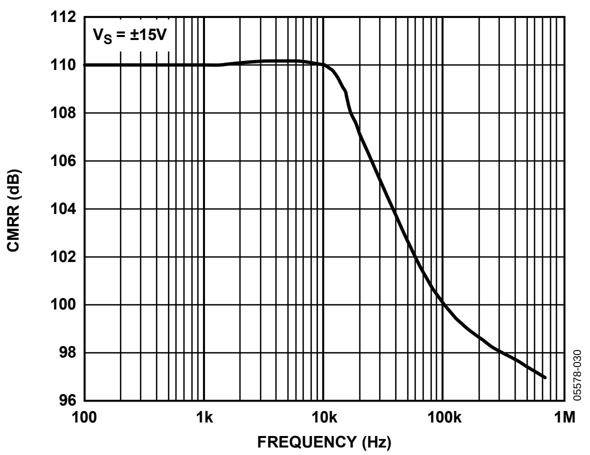

Figure 28. CMRR vs. Frequency

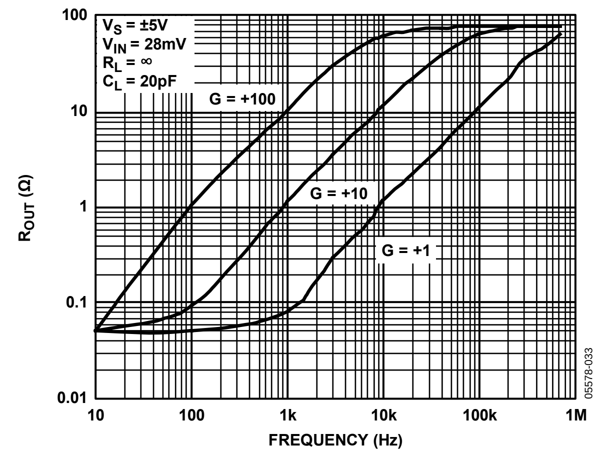

Figure 31. Output Impedance vs. Frequency

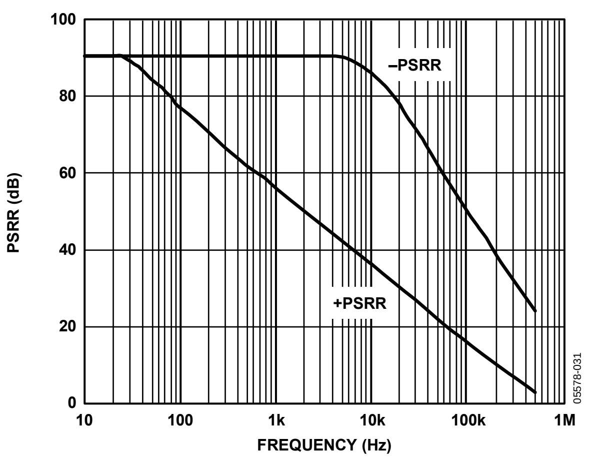

Figure 29. PSRR vs. Frequency

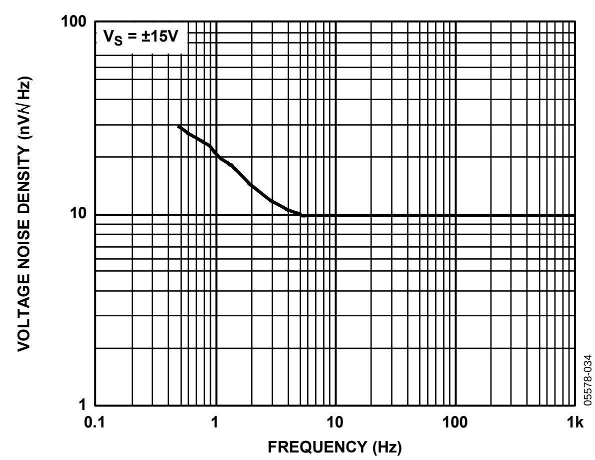

Figure 32. Voltage Noise Density vs. Frequency

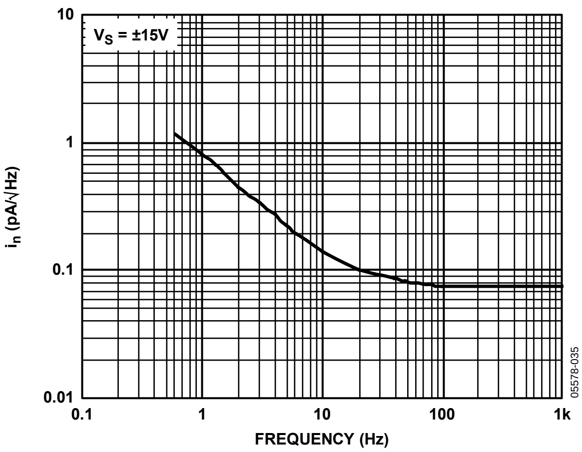

Figure 33. Current Noise Density vs. Frequency

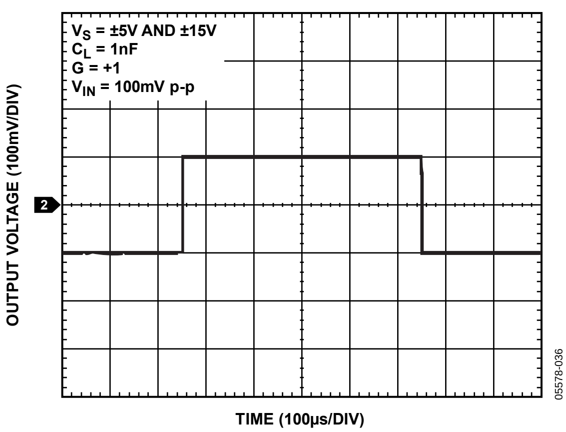

Figure 34. Small Signal Transient

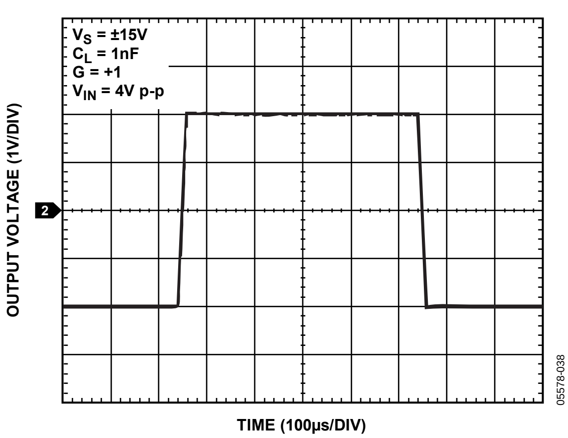

Figure 35. Large Signal Transient

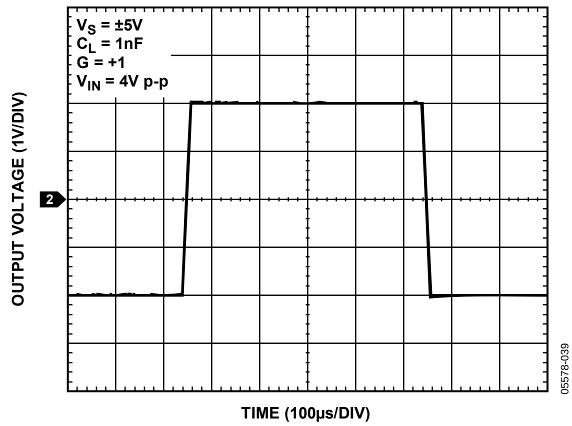

Figure 36. Large Signal Transient

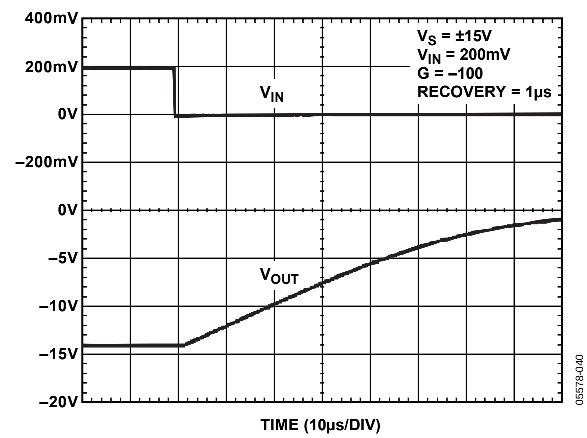

Figure 37. Positive Overload Recovery

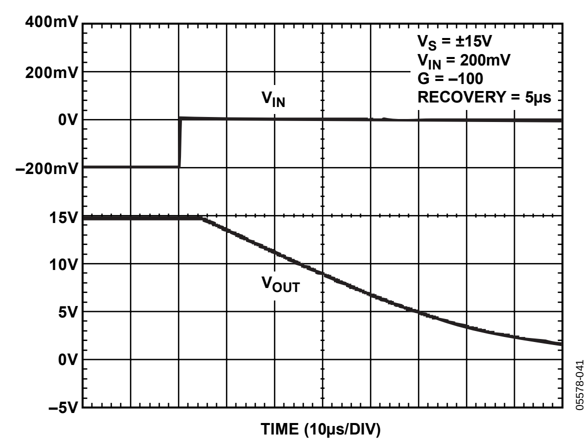

Figure 38. Negative Overload Recovery

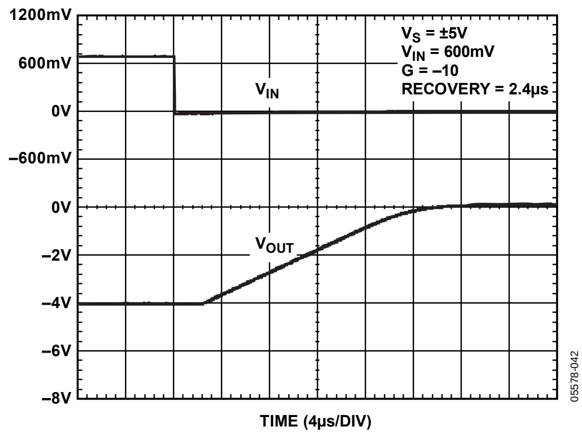

Figure 39. Positive Overload Recovery

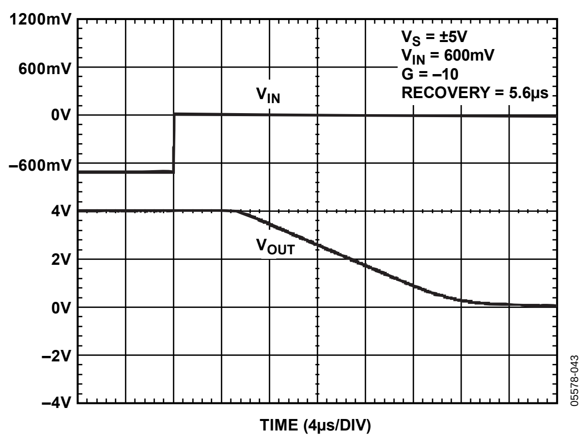

Figure 40. Negative Overload Recovery

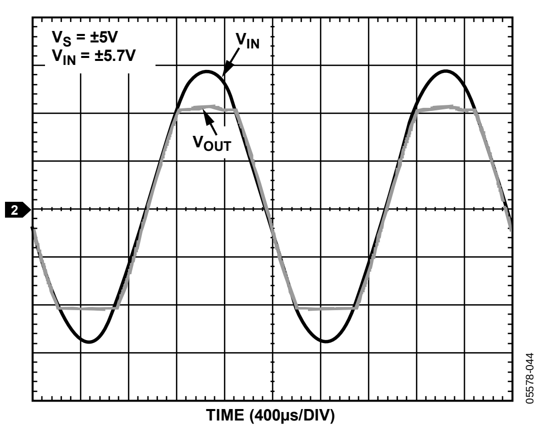

Figure 41. No Phase Reversal

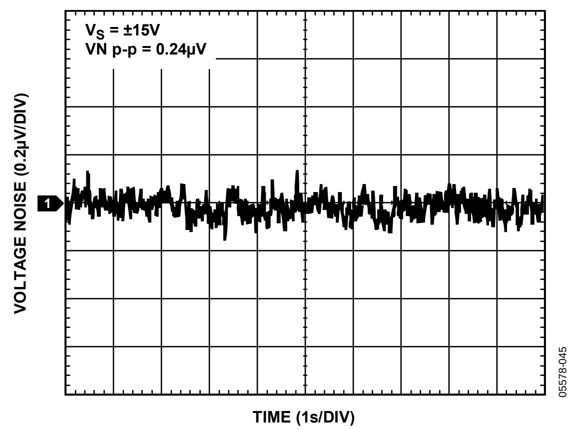

Figure 42. Voltage Noise (0.1 Hz to 10 Hz)

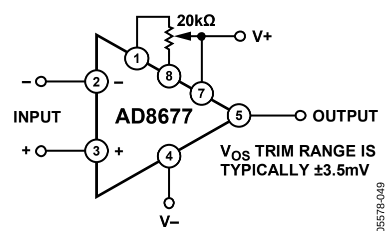

Figure 43. Optional Offset Nulling Circuit

OUTLINE DIMENSIONS

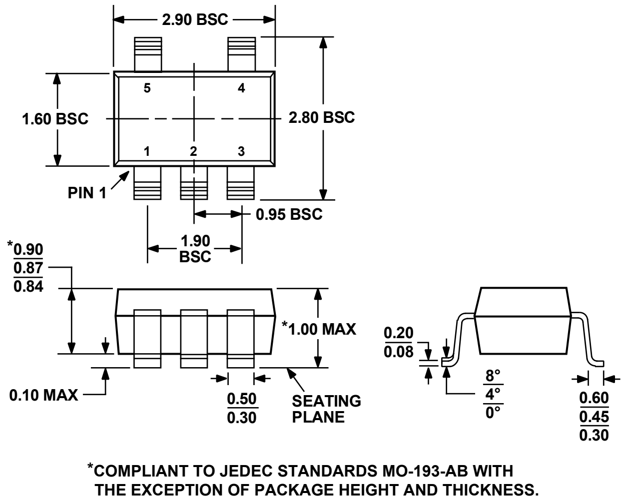

Figure 44. 5-Lead Thin Small Outline Transistor Package [TSOT]
(UJ-5)
Dimensions shown in millimeters

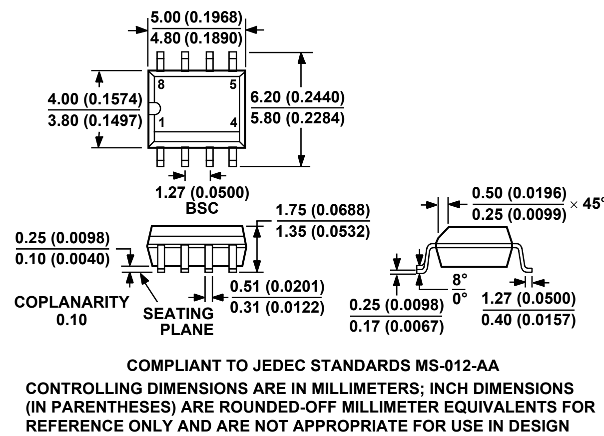

Figure 45. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
AD8677ARZ[1]	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
AD8677ARZ-REEL[1]	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
AD8677ARZ-REEL7[1]	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
AD8677AUJZ-R2[1]	−40°C to +125°C	5-Lead Thin Small Outline Transistor Package [TSOT]	UJ-5	A0E
AD8677AUJZ-REEL[1]	−40°C to +125°C	5-Lead Thin Small Outline Transistor Package [TSOT]	UJ-5	A0E
AD8677AUJZ-REEL7[1]	−40°C to +125°C	5-Lead Thin Small Outline Transistor Package [TSOT]	UJ-5	A0E

[1] Z = Pb-free part.

NOTES

NOTES

NOTES

D05578-0-11/05(0)