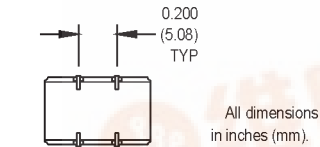
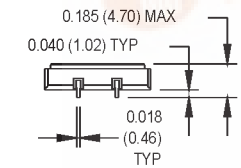
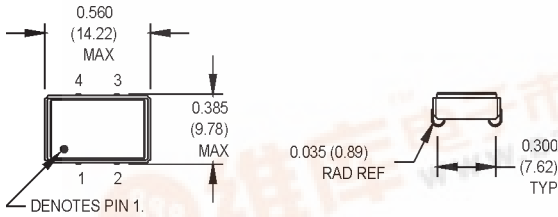


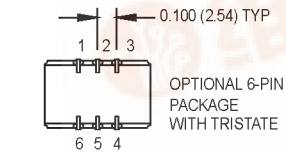
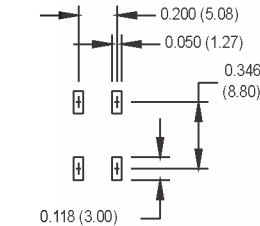


M5R Series

9x14 mm, 3.3 Volt, LVPECL/LVDS, Clock Oscillator



SUGGESTED SOLDER PAD LAYOUT



Pin Connections

FUNCTION	4 Pin	6 Pin
N/C or Output Q	1	1
Enable		2
Ground/Cover	2	3
Output Q	3	4
+Vcc	4	5
		6

Ordering Information		M5R	1	8	Z	Q	J	-R	00.0000	MHz
Product Series										
Temperature Range										
1: 0°C to +70°C		2: -40°C to +85°C								
6: -20°C to +70°C		7: -0°C to +85°C								
8: 0°C to +50°C										
Stability										
3: ±100 ppm		4: ±50 ppm		5: ±35 ppm						
6: ±25 ppm		8: ±20 ppm								
Output Type										
R: Complementary Enable		T: Single Enable								
Z: Complementary w/o Enable		X: Single w/o Enable								
Symmetry/Output Logic Type										
L: 45/55% LVDS		P: 45/55% PECL								
H: 40/60% LVDS		Q: 40/60% PECL								
Package/Lead Configurations										
J: J-lead										
RoHS Compliance										
Blank: non-RoHS compliant part										
-R: RoHS compliant part										
Frequency (customer specified)										

1. Calibration, deviation over temperature, shock, vibration, and aging.
 2. PECL load - see load circuit diagram #5. LVDS load - see load circuit diagram #9.
- M2011Sxxx - Contact factory for datasheet.

PARAMETER	Symbol	Min.	Typ.	Max.	Units	Condition/Notes	
Frequency Range	F	0.75		800	MHz		
Operating Temperature	T _A	(See ordering information)					
Storage Temperature	T _S	-55		+125	°C		
Frequency Stability	ΔF/F	(See ordering information)					
Aging						See Note 1	
1st Year			±2		ppm		
Thereafter (per year)			±1		ppm		
Input Voltage	V _{CC}	3.135	3.3	3.465	V		
PECL Input Current	I _{CC}			60	mA	0.75 to 24 MHz	
				95	mA	24 to 96 MHz	
				105	mA	96 to 800 MHz	
LVDS Input Current	I _{CC}			30	mA	0.75 to 24 MHz	
				60	mA	24 to 800 MHz	
Output Type						PECL/LVDS	
Load						See Note 2	
				50 Ohms to V _{CC} - 2 VCD		PECL Waveform	
				100 Ohm differential load		LVDS Waveform	
Symmetry (Duty Cycle)						@ V _{CC} -1.3 VDC (LVPECL)	
						@ 50% of waveform (LVDS)	
Output Skew				200	ps	PECL	
Differential Voltage		250	350	450	mV	LVDS	
Logic "1" Level	V _{OH}	V _{CC} -1.02			V	PECL	
Logic "0" Level	V _{OL}			V _{CC} -1.63	V	PECL	
Rise/Fall Time	T _r /T _f		0.35	0.55	ns	@ 20/80% LVPECL	
			0.50	1.0	ns	@ 20/80% LVDS	
Enable Function		80% V _{CC} min or N/C: output active					
		20% V _{CC} max: output disables to high-Z					"R" & "T" output types
Start up Time				10	ms		
Phase Jitter	φ _J					Integrated 12 kHz - 20 MHz	
				3	5	ps RMS	
Environmental							
Mechanical Shock		MIL-STD-202, Method 213, C (100 g's)					
Vibration		MIL-STD-202, Method 201 & 204 (10 g's from 10-2000 Hz)					
Thermal Cycle		MIL-STD-883, Method 1010, B (-55°C to +125°C, 15 min dwell, 10 cycles)					
Hermeticity		MIL-STD-202, Method 112					
Solderability		Per EIAJ-STD-002					
Max Soldering Conditions		See solder profile, Figure 1					

1. Calibration, deviation over temperature, shock, vibration and aging.
2. PECL load - see Load Circuit Diagram #5. LVDS load - see load circuit diagram #9.

MtronPTI Lead Free Solder Profile

