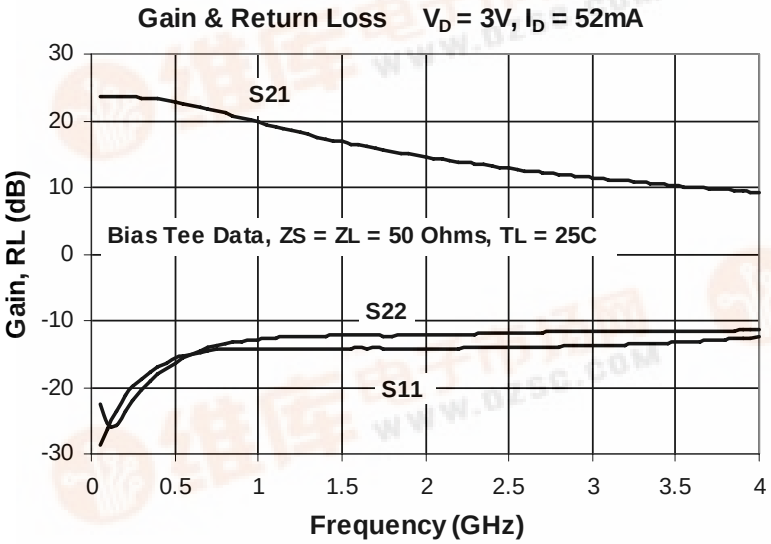
SGC-4463Z

50-4000 MHz Active Bias Silicon Germanium Cascadable Gain Block

RoHS Compliant & Green Package

Product Description

Sirenza Microdevices' SGC-4463Z is a high performance SiGe HBT MMIC amplifier utilizing a Darlington configuration with a patented active bias network. The active bias network provides stable current over temperature and process Beta variations. Designed to run directly from a 3V supply, the SGC-4463Z does not require a dropping resistor as compared to typical Darlington amplifiers. The SGC-4463Z is designed for high linearity 3V gain block applications that require small size and minimal external components. It is internally matched to 50 ohms.



Product Features

- Single Fixed 3V Supply
- No Dropping Resistor Required
- Patented Self-Bias Circuitry
- P1dB = 12.9 dBm at 1950 MHz
- OIP3 = 27 dBm at 1950 MHz
- Robust 1000V ESD, Class 1C HBM

Applications

- PA Driver Amplifier
- Cellular, PCS, GSM, UMTS, WCDMA
- IF Amplifier
- Wireless Data, Satellite

Symbol	Parameters	Units	Frequency	Min.	Typ.	Max.
G	Small Signal Gain	dB	850 MHz 1950 MHz 2400 MHz	19.0 12.9	20.5 14.4 13.3	22.0 15.9
P_{1dB}	Output Power at 1dB Compression	dBm	850 MHz 1950 MHz 2400 MHz	11.9	13.8 12.9 12.5	
OIP_3	Output Third Order Intercept Point	dBm	850 MHz 1950 MHz 2400 MHz	25.0	28.0 27.0 26.0	
IRL	Input Return Loss	dB	1950 MHz	10.0	13.0	
ORL	Output Return Loss	dB	1950 MHz	7.0	11.0	
NF	Noise Figure	dB	1930 MHz		3.7	4.7
V_D	Device Operating Voltage	V			3	
I_D	Device Operating Current	mA		46	52	58
Rth, j-l	Thermal Resistance (junction to lead)	°C/W			180	

Test Conditions: V_D = 3.0V I_D = 52mA Typ. T_L = 25°C OIP_3 Tone Spacing = 1MHz
Bias Tee Data $Z_S = Z_L$ = 50 Ohms Pout per tone = -5 dBm

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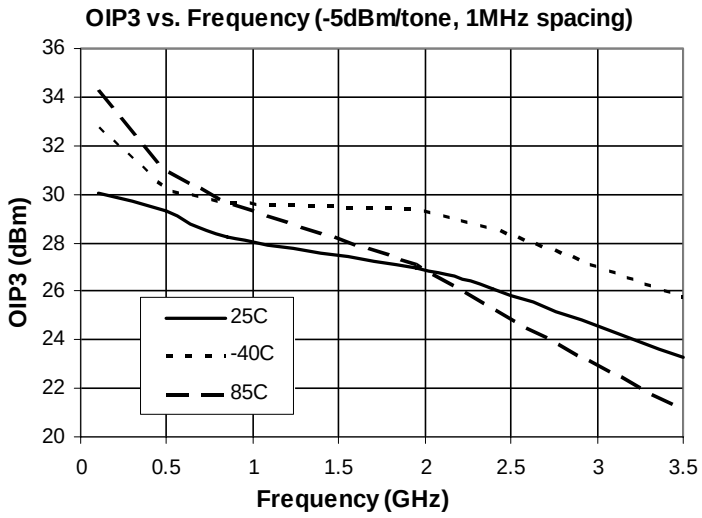
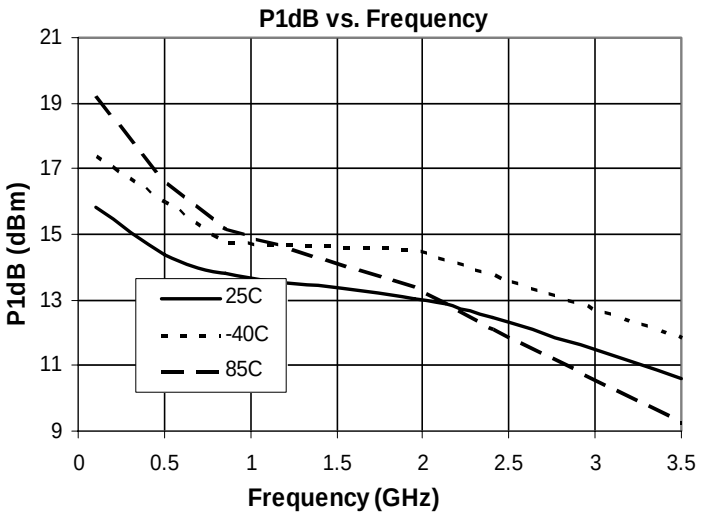
Typical RF Performance at Key Operating Frequencies (Bias Tee)

Symbol	Parameter	Unit	Frequency (MHz)					
			100	500	850	1950	2400	3500
G	Small Signal Gain	dB	23.6	23.0	20.5	14.4	13.3	10.4
OIP_3	Output Third Order Intercept Point	dBm	30.0	29.5	28.0	27.0	26.0	23.5
P_{1dB}	Output Power at 1dB Compression	dBm	16.0	14.4	13.8	12.9	12.5	10.6
IRL	Input Return Loss	dB	25.0	16.0	15.0	13.0	13.0	12.0
ORL	Output Return Loss	dB	24.5	16.0	13.0	11.0	10.0	10.0
S_{12}	Reverse Isolation	dB	25.0	26.0	25.5	21.5	20.5	19.0
NF	Noise Figure	dB	2.8	2.8	3.1	3.7	3.6	4.4

Test Conditions: V_D = 3V I_D = 52mA OIP_3 Tone Spacing = 1MHz, Pout per tone = -5 dBm
T_L = 25°C $Z_S = Z_L$ = 50 Ohms

Typical Performance with Bias Tee, V_D = 3V, I_D = 52mA





Absolute Maximum Ratings

Parameter	Absolute Limit
Max Device Current (I_{CE})	110 mA
Max Device Voltage (V_{CE})	4.5 V
Max. RF Input Power* (See Note)	+18 dBm
Max. Junction Temp. (T_J)	+150°C
Operating Temp. Range (T_L)	-40°C to +85°C
Max. Storage Temp.	+150°C

***Note:** Load condition, Z_L = 50 Ohms

Operation of this device beyond any one of these limits may cause permanent damage. For reliable continuous operation, the device voltage and current must not exceed the maximum operating values specified in the table on page one.

Bias Conditions should also satisfy the following expression:

$I_D V_D < (T_J - T_L) / R_{TH, j-l}$ $T_L = T_{LEAD}$

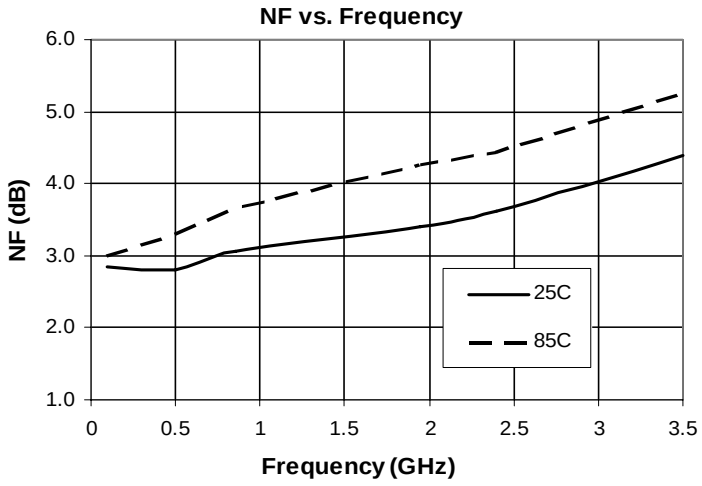
Reliability & Qualification Information

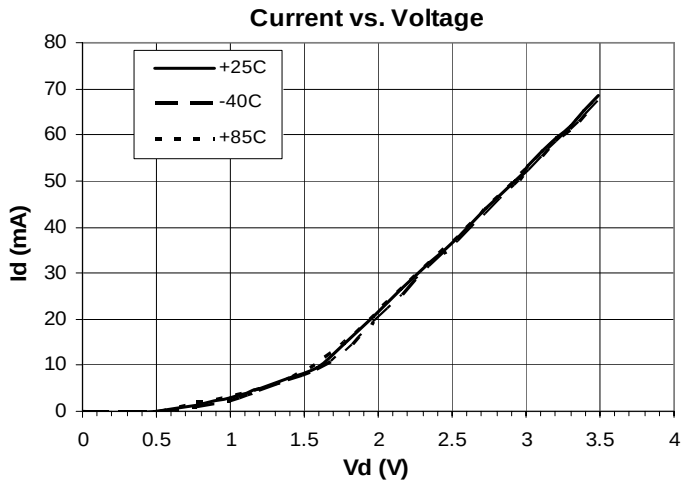
Parameter	Rating
ESD Rating - Human Body Model (HBM)	Class 1C
Moisture Sensitivity Level	MSL 1

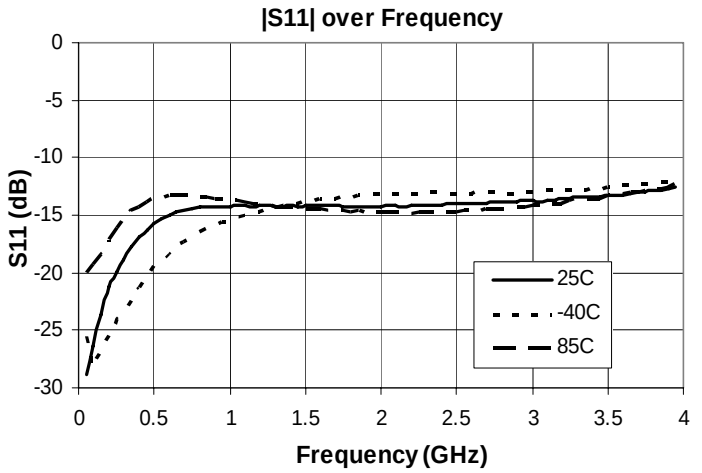
This product qualification report can be downloaded at *www.sirenza.com*

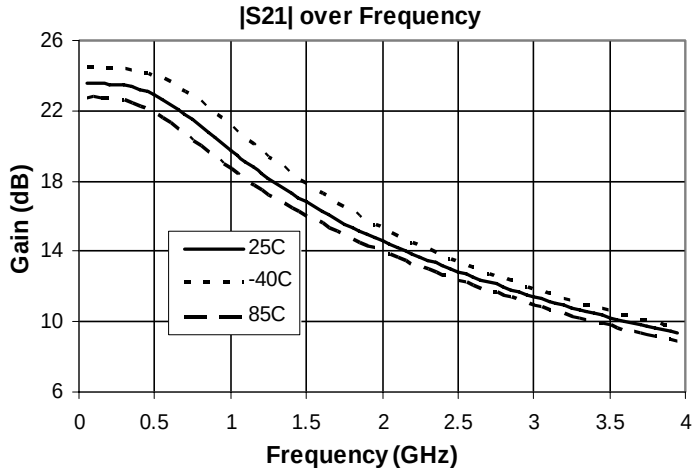
Caution: ESD sensitive
Appropriate precautions in handling, packaging and testing devices must be observed.

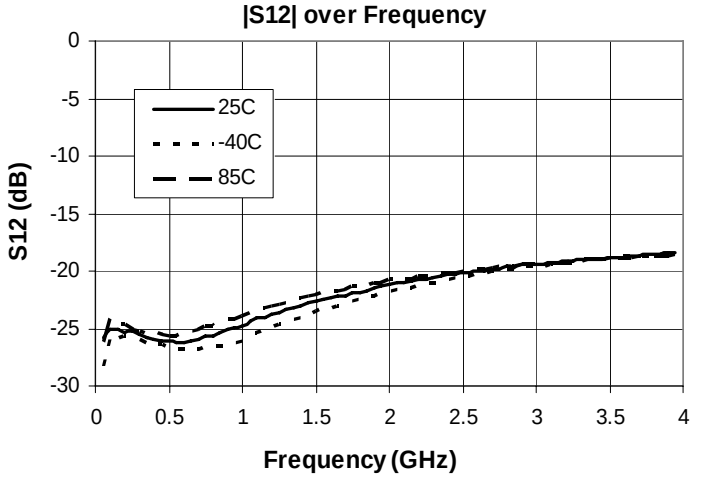
Typical Performance with Bias Tee, V_D = 3V, I_D = 52mA

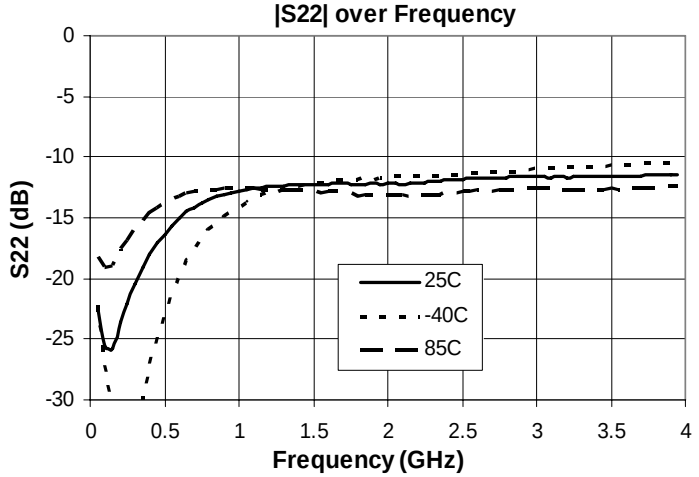




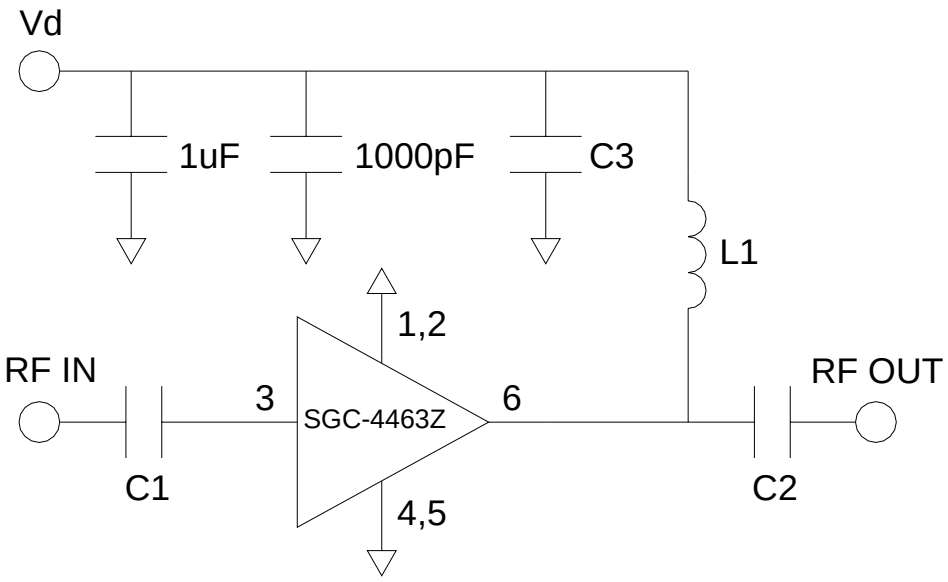




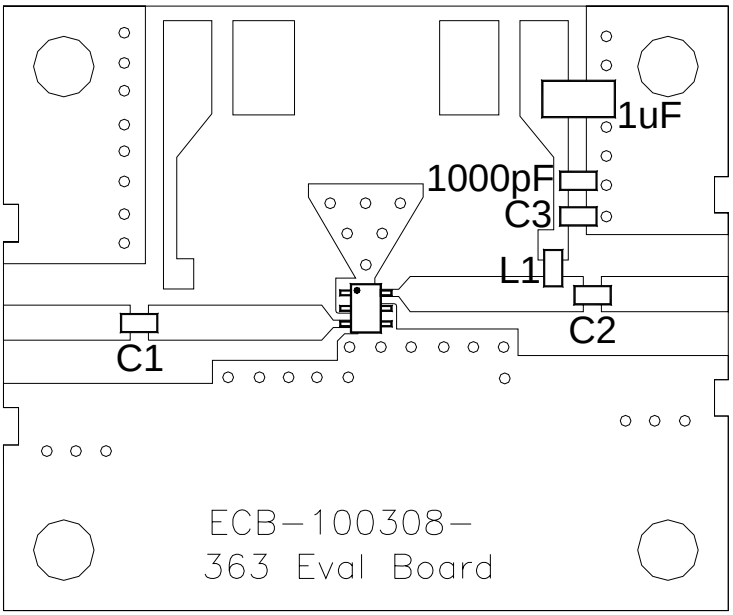




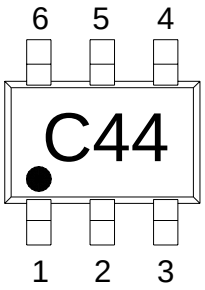
Basic Application Circuit



Application Circuit Element Values		
Reference Designator	**100-2000MHz**	**2000-4000MHz**
C1	1000pF	2.7pF
C2	100pF	6.8pF
C3	100pF	6.8pF
L1	120nH	39nH



Part Identification Marking & Pinout

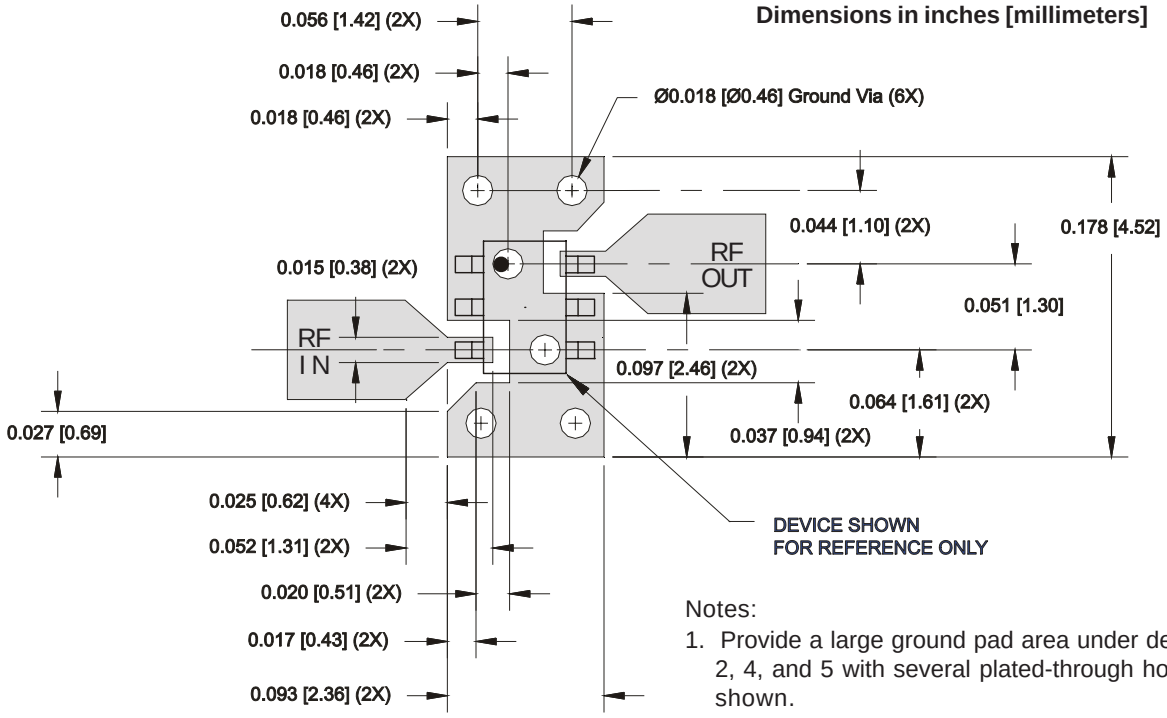


Pin #	Function	Description
3	RF IN	RF input pin. This pin requires the use of an external DC blocking capacitor chosen for the frequency of operation
1,2,4,5	GND	Connection to ground. Use via holes as close to the device ground leads as possible to reduce ground inductance and achieve optimum RF performance
6	RF OUT / DC BIAS	RF output and bias pin. This pin requires the use of an external DC blocking capacitor chosen for the frequency of operation.

Part / Evaluation Board Ordering Information			
Part Number	**Description**	**Reel Size**	**Devices / Reel**
SGC-4463Z	Lead Free, RoHs Compliant	7"	3000
SGC-4463Z-EVB1	100-2000 MHz Evaluation Board	N/A	N/A
SGC-4463Z-EVB2	2000-4000 MHz Evaluation Board	N/A	N/A

SOT-363 PCB Pad Layout

Dimensions in inches [millimeters]



Notes:

1. Provide a large ground pad area under device pins 1, 2, 4, and 5 with several plated-through holes placed as shown.
2. 1-2 ounce finished copper thickness is recommended.
3. RF I/O lines are 50Ω

SOT-363 Nominal Package Dimensions

Dimensions in inches [millimeters]

A link to the SOT-363 package outline drawing with full dimensions and tolerances may be found on the product web page at www.sirenza.com.