Automotive-Grade ProASIC^{PLUS} Flash Family FPGAs

FlashLock™

Features and Benefits

High Capacity
- 75,000 to 1 Million System Gates
- 27k to 198kbits of Two-Port SRAM
- 66 to 642 User I/Os

Reprogrammable Flash Technology
- 0.22µ 4LM Flash-based CMOS Process
- Live at Power-Up, Single-Chip Solution
- No Configuration Device Required
- Retains Programmed Design during Power-Down/Power-Up Cycles

Extended Temperature Range
- Supports Automotive Temperature Range -40 to 125°C (Junction)

Performance
- 3.3V, 32-Bit PCI (up to 50 MHz)
- Two Integrated PLLs
- External System Performance up to 150 MHz

Secure Programming
- Industry's Most Effective Security Key (FlashLock™) Prevents Read Back of Programming Bitstream

Low Power
- Low Impedance Flash Switches
- Segmented Hierarchical Routing Structure
- Small, Efficient, Configurable (Combinatorial or Sequential) Logic Cells

High Performance Routing Hierarchy
- Ultra-Fast Local and Long-Line Network
- High-Speed, Very Long-Line Network
- High Performance, Low-Skew, Splittable Global Network
- 100% Utilization and >95% Routability

I/O
- Schmitt-Trigger Option on Every Input
- 2.5V/3.3V Support with Individually-Selectable Voltage and Slew Rate
- Bidirectional Global I/Os
- Compliance with PCI Specification Revision 2.2
- Boundary-Scan Test IEEE Std. 1149.1 (JTAG) Compliant
- Pin Compatible Packages across ProASIC^{PLUS} Family

Unique Clock Conditioning Circuitry
- PLLs with Flexible Phase, Multiply/Divide and Delay Capabilities
- Internal and/or External Dynamic PLL Configuration
- Two LVPECL Differential Pairs for Clock or Data Inputs

Standard FPGA and ASIC Design Flow
- Flexibility with Choice of Industry-Standard Frontend Tools
- Efficient Design through Front-End Timing and Gate Optimization

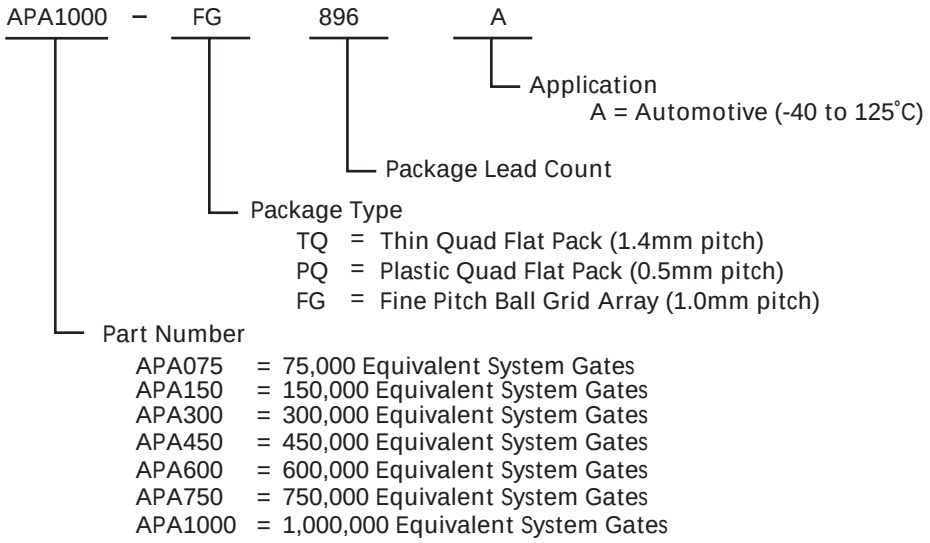
ISP Support
- In-System Programming (ISP) via JTAG Port

SRAMs and FIFOs
- ACTgen Netlist Generation Ensures Optimal Usage of Embedded Memory Blocks
- 24 SRAM and FIFO Configurations with Synchronous and Asynchronous Operation up to 150 MHz (typical)

Table 1 • **Automotive-Grade ProASIC^{PLUS} Product Profile**

Device	APA075	APA150	APA300	APA450	APA600	APA750	APA1000
Maximum System Gates	75,000	150,000	300,000	450,000	600,000	750,000	1,000,000
Maximum Tiles (Registers)	3,072	6,144	8,192	12,288	21,504	32,768	56,320
Embedded RAM Bits (k=1,024 bits)	27k	36k	72k	108k	126k	144k	198k
Embedded RAM Blocks (256x9)	12	16	32	48	56	64	88
LVPECL	2	2	2	2	2	2	2
PLL	2	2	2	2	2	2	2
Global Networks	4	4	4	4	4	4	4
Maximum Clocks	24	32	32	48	56	64	88
Maximum User I/Os	158	186	186	344	370	562	642
JTAG ISP	Yes	Yes	Yes	Yes	Yes	Yes	Yes
PCI	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Package (by pin count)							
TQFP	100	100	–	–	–	–	–
PQFP	208	208	208	208	208	208	208
PBGA	144	144, 256	144, 256	144, 256, 484	256, 484	896	896

Ordering Information



Plastic Device Resources

	User I/Os*					
Device	**TQFP 100-Pin**	**PQFP 208-Pin**	**FBGA 144-Pin**	**FBGA 256-Pin**	**FBGA 484-Pin**	**FBGA 896-Pin**
APA075	66	158	100			
APA150	66	158	100	186		
APA300		158	100	186		
APA450		158	100	186	344	
APA600		158		186	370	
APA750		158				562
APA1000		158				642

Package Definitions

TQFP = Thin Quad Flat Pack, PQFP = Plastic Quad Flat Pack, FBGA = Fine Pitch Ball Grid Array

*Each pair of PECL I/Os were counted as one user I/O.

Speed Grade Matrix

	Std
Automotive-Grade	✔

Contact your local Actel sales representative for device availability.

General Description

ProASIC^PLUS devices offer a reprogrammable design integration solution at the automotive temperature range (-40°C to +125°C) through the use of nonvolatile Flash technology. ProASIC^PLUS devices have a fine-grain architecture, similar to ASICs, and enable engineers to design high-density systems using existing ASIC or FPGA design flows and tools. Automotive-grade ProASIC^PLUS devices offer up to 1 million system gates, support up to 198kbits of two-port SRAM and 642 user I/Os and provide 50 MHz PCI performance.

The nonvolatile and reprogrammable Flash technology enables ProASIC^PLUS devices to be live at power-up, and no external boot PROM is required to support device programming. While on-board security mechanisms prevent any access to the programmed information, reprogramming can be performed in-system to support future design iterations and field upgrades. The ProASIC^PLUS device architecture mitigates the complexity of ASIC migration at higher user volume, making the automotive-grade ProASIC^PLUS a cost-effective solution for in-cabin telematics and automobile interconnect applications.

The ProASIC^PLUS family is built on an advanced Flash-based 0.22µm LVCMOS process with four layers of metal. Standard CMOS design techniques are used to implement logic and control functions, including the PLLs and LVPECL inputs, resulting in predictable performance fully compatible with gate arrays.

The ProASIC^PLUS architecture provides granularity comparable to gate arrays. The device core consists of a Sea-of-Tiles™. Each tile can be configured as a flip-flop, latch, or three-input/one-output logic function by programming the appropriate Flash switches. The combination of fine granularity, flexible routing resources, and abundant Flash switches allows 100% utilization and over 95% routability for highly congested designs. Tiles and larger functions are interconnected through a four-level routing hierarchy.

Automotive-grade ProASIC^PLUS devices feature embedded two-port SRAM blocks with built-in FIFO/RAM control logic and user-defined depth and width. Users can select programming for synchronous or asynchronous operation, as well as parity generation or checking.

The automotive-grade ProASIC^PLUS devices offer a unique clock conditioning circuit (CCC), with two clock conditioning blocks in each device. Each block provides a phase-locked loop (PLL) core, delay lines, phase shifts (0°, 90°, 180°, 270°), and clock multipliers/dividers, as well as the circuitry required to provide bidirectional access to the PLL. The PLL block contains four programmable frequency dividers, which allow the incoming clock signal to be divided by a wide range of factors from 1 to 64. The clock conditioning circuit can perform a positive/negative clock delay operation in increments of 0.25 ns by up to 8 ns. The PLL can be configured internally or externally during operation without redesigning or reprogramming the part. In addition to the PLL, there are two LVPECL differential input pairs to accommodate high speed clock and data inputs.

The automotive-grade ProASIC^PLUS devices are available in a variety of high-performance plastic packages to simplify the system board design.

To support for comprehensive, lower cost board-level testing, Actel's ProASIC^PLUS devices are fully compatible with IEEE Standard 1149.1 for test access port and boundary-scan test architecture.

Operating Conditions

Table 1 • **Absolute Maximum Ratings***

Parameter	Condition	Minimum	Maximum	Units
Supply Voltage Core (V_{DD})		–0.3	3.0	V
Supply Voltage I/O Ring (V_{DDP})		–0.3	4.0	V
DC Input Voltage		–0.3	V_{DDP} + 0.3	V
PCI DC Input Voltage		–1.0	V_{DDP} + 1.0	V
PCI DC Input Clamp Current (absolute)	V_{IN} < –1V or V_{IN} = V_{DDP} + 1V	10		mA
LVPECL Input Voltage		–0.3	V_{DDP} + 0.5	V
GND		0	0	V

Note: **Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.*

Performance Retention

Actel guarantees the performance numbers presented in the Actel Designer timing analysis software and in this datasheet, as long as the specified device performance retention period is not exceeded. For devices operated and stored at 110°C or less, the performance retention period is 20 years after programming. For devices operated and stored at temperatures greater than 110°C, refer to Table 2 on page 5 to determine the performance retention period. Actel does not guarantee performance if the performance retention period is exceeded. Evaluate the percentage of time spent at the highest temperature, then determine the next highest temperature to which the device will be exposed. In Table 2 on page 5, find the temperature profile that most closely matches the application.

For example, the ambient temperature of a system cycles between 100°C (25% of the time) and 50°C (75% of the time). No forced ventilation cooling system is in use. An APA600-PQ208A FPGA operates in the system, dissipating 1W. The package thermal resistance (junction-to-ambient) in still air is 20°C/W, indicating that the junction temperature of the FPGA will be 120°C (25% of the time) and 70°C (75% of the time). The entry in Table 2 on page 5, which most closely matches the application, is 25% at 125°C with 75% at 110°C. Performance retention in this example is at least 16.0 years.

Note that exceeding the stated retention period may result in a performance degradation in the FPGA below the worst-case performance indicated in the Actel Timer. To ensure that performance does not degrade below the worst-case values in the Actel Timer, the FPGA must be reprogrammed within the performance retention period. In addition, note that performance retention is independent of whether or not the FPGA is operating. The retention period of a device in storage at a given temperature will be the same as the retention period of a device operating at that junction temperature.

Table 2 • **Performance Retention**

Time at T_J 110°C or below	Time at T_J 125°C or below	Minimum Program Retention (Years)
100%	0%	20.0
99%	1%	19.8
98%	2%	19.6
95%	5%	19.0
90%	10%	18.2
85%	15%	17.4
80%	20%	16.7
75%	25%	16.0
70%	30%	15.4
60%	40%	14.3
50%	50%	13.3
25%	75%	11.4
0%	100%	10.0

Table 3 • **Nominal Supply Voltages**

Mode	V_{DD}	V_{DDP}
2.5V Output	2.5V	2.5V
3.3V Output*	2.5V	3.3V

Note: **Automotive-grade ProASIC^PLUS devices do not support mixed-mode I/Os.*

Table 4 • **Recommended Maximum Operating Conditions for Programming and PLL Supplies***

Parameter	Condition	Automotive		Units
		Minimum	Maximum	
V_{PP}	During Programming	15.8	16.5	V
	Normal Operation	0	16.5	V
V_{PN}	During Programming	–13.8	–13.2	V
	Normal Operation	–13.8	0	V
I_{PP}	During Programming		25	mA
I_{PN}	During Programming		10	mA
AVDD		V_{DD}	V_{DD}	V
AGND		GND	GND	V

Note: **Devices should not be operated outside the Recommended Operating Conditions.*

Table 5 • **Recommended Operating Conditions***

Parameter	Symbol	Limits
		Automotive
DC Supply Voltage (2.5V I/Os)	V_{DD} & V_{DDP}	2.5V ± 5%
DC Supply Voltage (3.3V I/Os)	V_{DDP} V_{DD}	3.3V ± 5% 2.5V ± 5%
Operating Junction Temperature Range	T_J	-40°C to125°C

Note: **Devices should not be operated outside the Recommended Operating Conditions.*

Table 6 • **DC Electrical Specifications (V_{DD} and V_{DDP} = 2.5V ±5%)**

Symbol	Parameter	Conditions	Automotive[1]			Units
			Min.	Typ.	Max.	
V_{OH}	Output High Voltage High Drive (OB25LPH) Low Drive (OB25LPL)	I_{OH} = –6 mA I_{OH} = –12 mA I_{OH} = –24 mA I_{OH} = –3 mA I_{OH} = –6 mA I_{OH} = –8 mA	2.1 2.0 1.7 2.1 1.9 1.7			V
V_{OL}	Output Low Voltage High Drive (OB25LPH) Low Drive (OB25LPL)	I_{OL} = 8 mA I_{OL} = 15 mA I_{OL} = 24 mA I_{OL} = 4 mA I_{OL} = 8 mA I_{OL} = 15 mA			0.2 0.4 0.7 0.2 0.4 0.7	V
V_{IH}	Input High Voltage		1.7		V_{DDP} + 0.3	V
V_{IL}	Input Low Voltage		–0.3		0.7	V
$R_{WEAKPULLUP}$	Weak Pull-up Resistance (OTB25LPU)	$V_{IN} \geq$ 1.25V	6		56	kΩ
HYST	Input Hysteresis Schmitt		0.3	0.35	0.45	V
I_{IN}	Input Current	with pull up (V_{IN} = GND)	–240		– 20	µA
		without pull up (V_{IN} = GND or V_{DD})	–50		50	µA
I_{DDQ}	Quiescent Supply Current (standby)	V_{IN} = GND[2] or V_{DD}		5.0	20	mA
I_{OZ}	Tristate Output Leakage Current	V_{OH} = GND or V_{DD}	–50		50	µA
I_{OSH}	Output Short Circuit Current High High Drive (OB25LPH) Low Drive (OB25LPL)	 V_{IN} = V_{SS} V_{IN} = V_{SS}	 –120 –100			mA
I_{OSL}	Output Short Circuit Current Low High Drive (OB25LPH) Low Drive (OB25LPL)	 V_{IN} = V_{DDP} V_{IN} = V_{DDP}			 100 30	mA
$C_{I/O}$	I/O Pad Capacitance				10	pF
C_{CLK}	Clock Input Pad Capacitance				10	pF

Notes:

1. All process conditions. Junction Temperature: –40 to +125°C.
2. No pull-up resistor.

Table 7 • **DC Electrical Specifications (V_{DDP} = 3.3V ±5% and V_{DD} 2.5V ±5%)**

Symbol	Parameter	Conditions	Automotive[1]			Units
			Min.	Typ.	Max.	
V_{OH}	Output High Voltage 3.3V I/O, High Drive (OB33P) 3.3V I/O, Low Drive (OB33L)	I_{OH} = –14 mA I_{OH} = –24 mA I_{OH} = –6 mA I_{OH} = –12 mA	0.9*V_{DDP} 2.4 0.9*V_{DDP} 2.4			V
V_{OL}	Output Low Voltage 3.3V I/O, High Drive (OB33P) 3.3V I/O, Low Drive (OB33L)	I_{OL} = 15 mA I_{OL} = 20 mA I_{OL} = 28 mA I_{OL} = 7 mA I_{OL} = 10 mA I_{OL} = 15 mA			0.1V_{DDP} 0.4 0.7 0.1V_{DDP} 0.4 0.7	V
V_{IH}	Input High Voltage 3.3V LVTTL/LVCMOS		2		V_{DDP} + 0.3	V
V_{IL}	Input Low Voltage 3.3V LVTTL/LVCMOS		–0.3		0.8	V
$R_{WEAKPULLUP}$	Weak Pull-up Resistance (IOB33U)	$V_{IN} \geq$ 1.5V	7		43	kΩ
$R_{WEAKPULLUP}$	Weak Pull-up Resistance (IOB25U)	$V_{IN} \geq$ 1.5V	7		43	kΩ
I_{IN}	Input Current	with pull up (V_{IN} = GND)	–300		–40	µA
		without pull up (V_{IN} = GND or V_{DD})	–50		50	µA
I_{DDQ}	Quiescent Supply Current (standby)	V_{IN} = GND[2] or V_{DD}		5.0	20	mA
I_{OZ}	Tristate Output Leakage Current	V_{OH} = GND or V_{DD}	–10		10	µA
I_{OSH}	Output Short Circuit Current High 3.3V High Drive (OB33P) 3.3V Low Drive (OB33L)	 V_{IN} = GND V_{IN} = GND	 –200 –100			mA
I_{OSL}	Output Short Circuit Current Low 3.3V High Drive 3.3V Low Drive	 V_{IN} = V_{DD} V_{IN} = V_{DD}			 200 100	mA
$C_{I/O}$	I/O Pad Capacitance				10	pF
C_{CLK}	Clock Input Pad Capacitance				10	pF

Notes:

1. All process conditions. Junction Temperature: –40 to +125°C.
2. No pull-up resistor.

Table 8 • **DC Specifications (3.3V PCI Revision 2.2 Operation)[1]**

Symbol	Parameter	Condition	Automotive[2]		Units
			Min.	Max.	
V_{DD}	Supply Voltage for Core		2.375	2.625	V
V_{DDP}	Supply Voltage for I/O Ring		3.135	3.465	V
V_{IH}	Input High Voltage		$0.5V_{DDP}$	V_{DDP} + 0.5	V
V_{IL}	Input Low Voltage		–0.5	$0.3V_{DDP}$	V
I_{IPU}	Input Pull-up Voltage[3]		$0.7V_{DDP}$		V
I_{IL}	Input Leakage Current[4]	$0 < V_{IN} < V_{CCI}$	–50	50	µA
V_{OH}	Output High Voltage	I_{OUT} = –500 µA	$0.9V_{DDP}$		V
V_{OL}	Output Low Voltage	I_{OUT} = 1500 µA		$0.1V_{DDP}$	V
C_{IN}	Input Pin Capacitance (except CLK)			10	pF
C_{CLK}	CLK Pin Capacitance		5	12	pF

Notes:

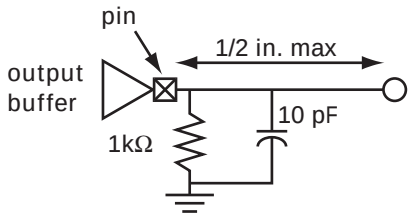
1. For PCI operation, use OTB33PH, OB33PH, IOB33PH, IB33, or IB33S macro library cells only.
2. All process conditions. Junction Temperature: –40 to +125°C.
3. This specification is guaranteed by design. It is the minimum voltage to which pull-up resistors are calculated to pull a floated network. Designers with applications sensitive to static power utilization should ensure that the input buffer is conducting minimum current at this input voltage.
4. Input leakage currents include hi-Z output leakage for all bidirectional buffers with tristate outputs.

Table 9 • **AC Specifications (3.3V PCI Revision 2.2 Operation)**

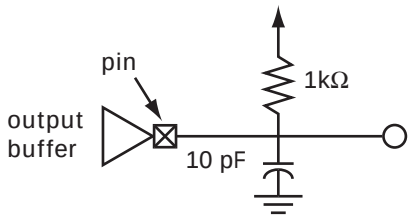
Symbol	Parameter	Condition	Automotive		Units
			Min.	Max.	
$I_{OH(AC)}$	Switching Current High	$0 < V_{OUT} \le 0.3V_{CCI}$*	$-12V_{CCI}$		mA
		$0.3V_{CCI} \le V_{OUT} < 0.9V_{CCI}$*	$(-17.1 + (V_{DDP} - V_{OUT}))$		mA
		$0.7V_{CCI} < V_{OUT} < V_{CCI}$*		See equation C – page 124 of the PCI Specification document rev. 2.2	
	(Test Point)	$V_{OUT} = 0.7V_{CC}$*		$-32V_{CCI}$	mA
$I_{OL(AC)}$	Switching Current Low	$V_{CCI} > V_{OUT} \ge 0.6V_{CCI}$*	$16V_{DDP}$		mA
		$0.6V_{CCI} > V_{OUT} > 0.1V_{CCI}$ [1]	$(26.7V_{OUT})$		mA
		$0.18V_{CCI} > V_{OUT} > 0$*		See equation D – page 124 of the PCI Specification document rev. 2.2	
	(Test Point)	$V_{OUT} = 0.18V_{CC}$		$38V_{CCI}$	mA
I_{CL}	Low Clamp Current	$-3 < V_{IN} \le -1$	$-25 + (V_{IN} + 1)/0.015$		mA
I_{CH}	High Clamp Current	$V_{CCI} + 4 > V_{IN} \ge V_{CCI} + 1$	$25 + (V_{IN} - V_{DDP} - 1)/0.015$		mA
$slew_R$	Output Rise Slew Rate	$0.2V_{CCI}$ to $0.6V_{CCI}$ load*	1	4	V/ns
$slew_F$	Output Fall Slew Rate	$0.6V_{CCI}$ to $0.2V_{CCI}$ load*	1	4	V/ns

Note: ** Refer to the PCI Specification document rev. 2.2.*

Pad Loading Applicable to the Rising Edge PCI



Pad Loading Applicable to the Falling Edge PCI



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