

Inchange Semiconductor

Product Specification

Silicon NPN Power Transistors

2SD1445 2SD1445A

DESCRIPTION

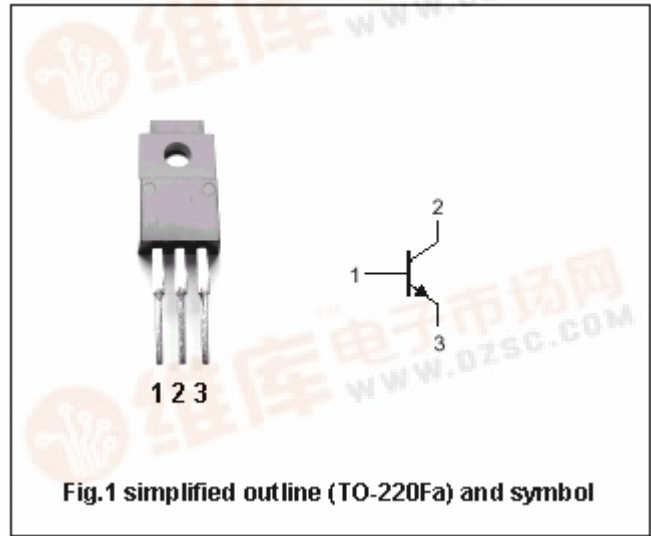
- With TO-220Fa package
- Complement to type 2SB948/948A
- High speed switching
- Low collector saturation voltage

APPLICATIONS

- For power amplification, power switching and low-voltage switching applications

PINNING

PIN	DESCRIPTION
1	Base
2	Collector
3	Emitter



Absolute maximum ratings(Ta=25)

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT	
V _{CBO}	Collector-base voltage	Open emitter	2SD1445	40	V
			2SD1445A	50	
V _{CEO}	Collector-emitter voltage	Open base	2SD1445	20	V
			2SD1445A	40	
V _{EBO}	Emitter-base voltage	Open collector	5	V	
I _C	Collector current		10	A	
I _{CM}	Collector current-peak		20	A	
P _C	Collector power dissipation	T _a =25	2	W	
		T _C =25	40		
T _j	Junction temperature		150		
T _{stg}	Storage temperature		-55~150		

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CHARACTERISTICS

T_j=25 unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V _{(BR)CEO}	Collector-emitter breakdown voltage	2SD1445	20			V
		2SD1445A	40			
V _{CEsat}	Collector-emitter saturation voltage	I _C =10mA ; I _B =0			0.6	V
V _{BEsat}	Base-emitter saturation voltage	I _C =10A ; I _B =0.33A			1.5	V
I _{CBO}	Collector cut-off current	2SD1445			50	μA
		2SD1445A				
I _{EBO}	Emitter cut-off current	V _{EB} =5V ; I _C =0			50	μA
h _{FE-1}	DC current gain	I _C =0.1A ; V _{CE} =2V	45			
h _{FE-2}	DC current gain	I _C =3A ; V _{CE} =2V	90		260	
f _T	Transition frequency	I _C =0.5A ; V _{CE} =10V, f=10MHz		120		MHz
C _{OB}	Collector output capacitance	I _E =0 ; f=1MHz ; V _{CB} =10V		200		pF

Switching times

t _{on}	Trun-on time			0.3		μs
t _{stg}	Storage time	I _C =3A I _{B1} =0.1A, I _{B2} =-0.1A V _{CC} =20V		0.4		μs
t _f	Fall time			0.1		μs

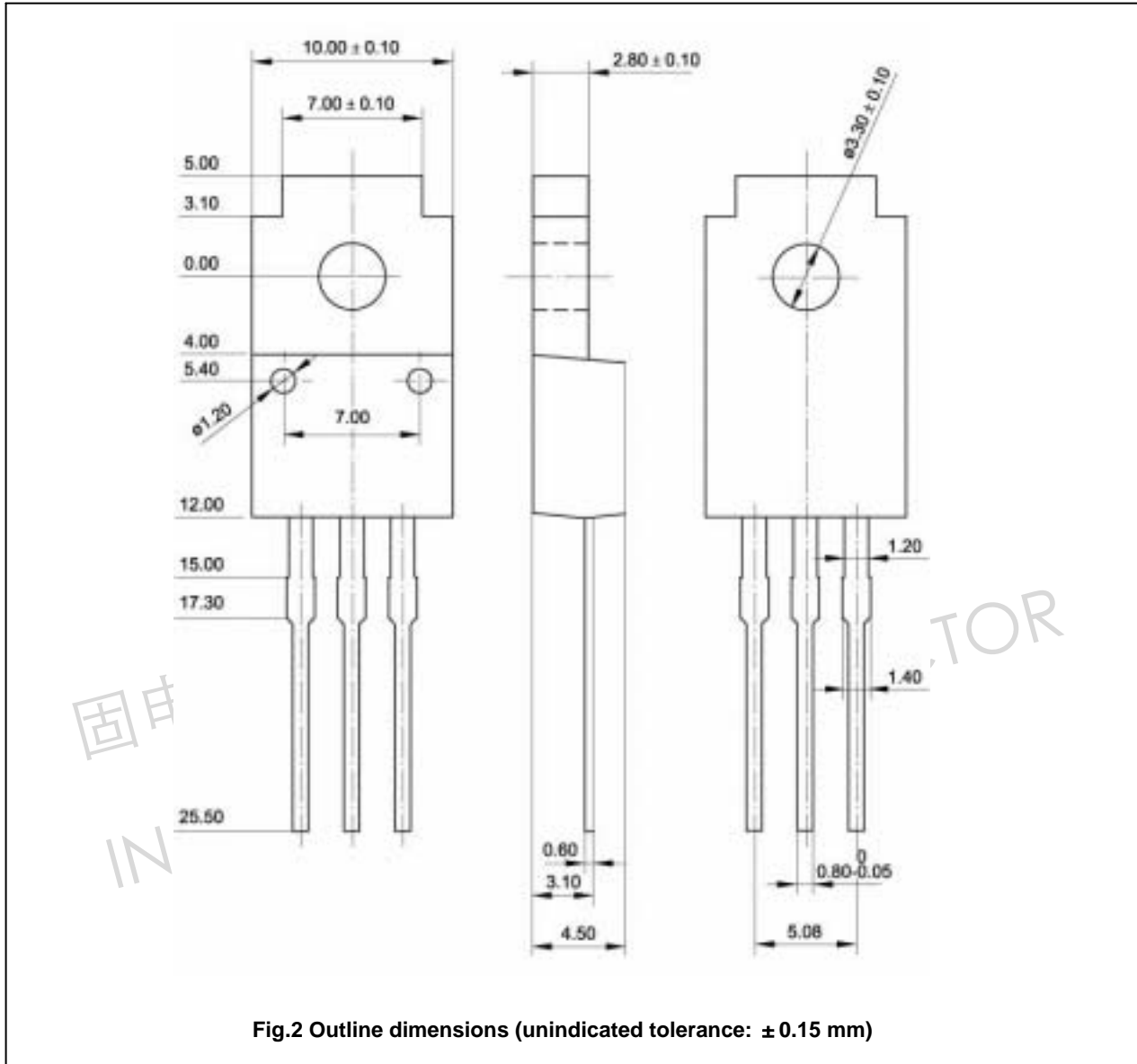
◆ h_{FE-2} Classifications

Q	P
90-180	130-260

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PACKAGE OUTLINE



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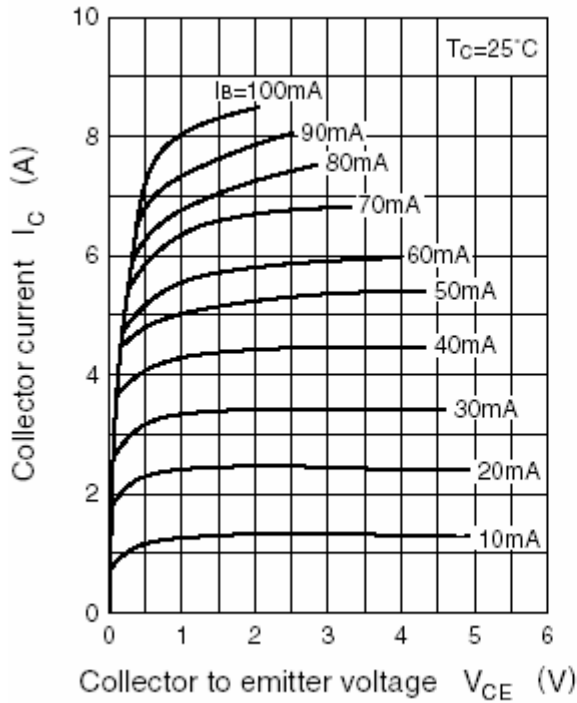


Fig.3 Static Characteristic

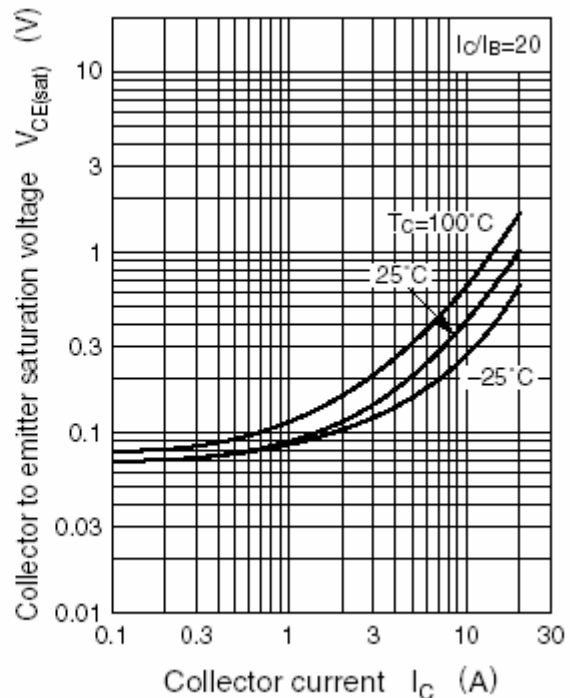


Fig.4 Collector-Emitter Saturation Voltage

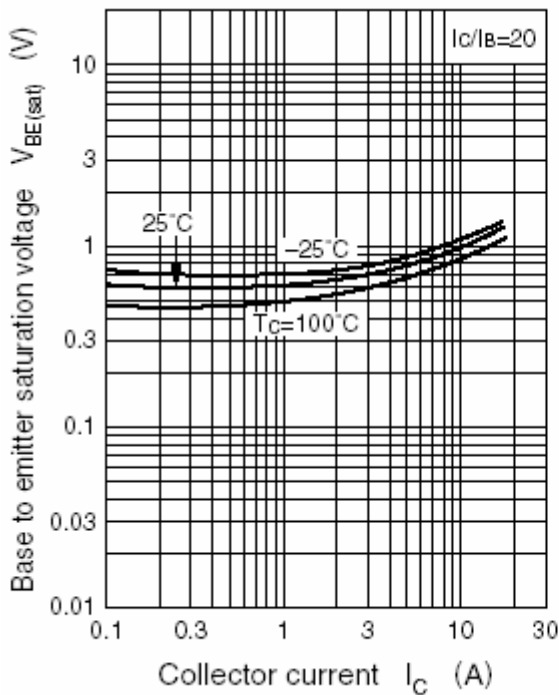


Fig.5 Base-Emitter Saturation Voltage

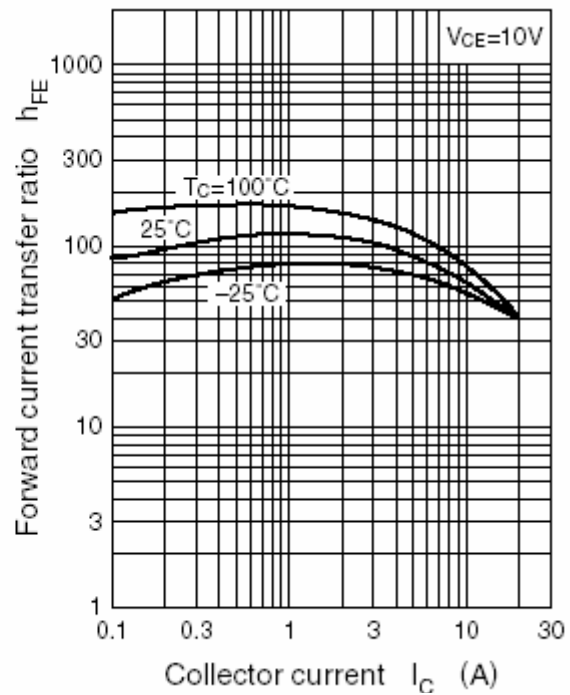


Fig.6 DC current Gain

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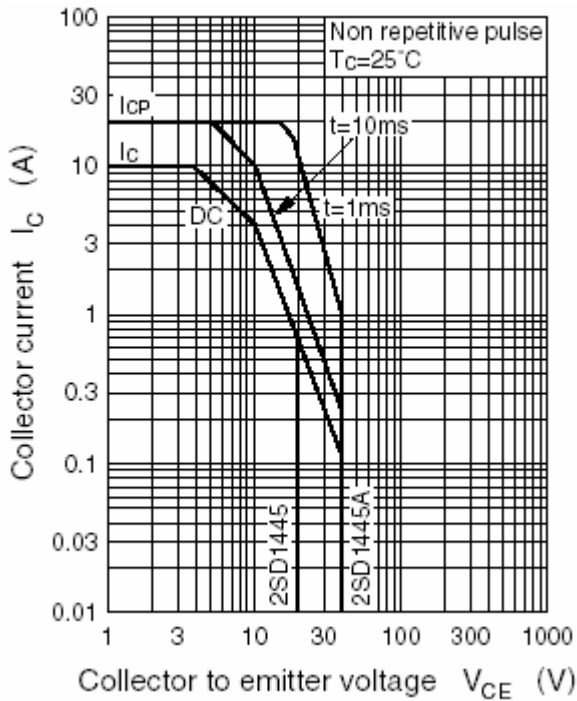


Fig.7 Safe Operating Area

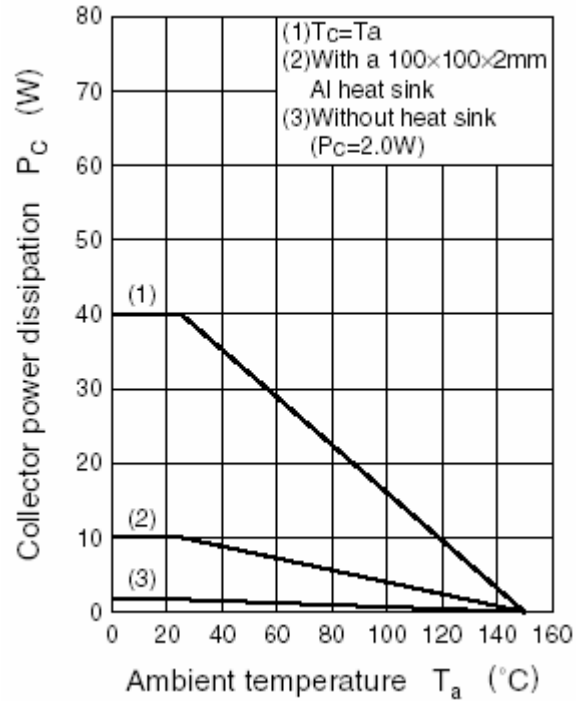


Fig.8 Power Derating

固电半导体
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