



## LTC4442/LTC4442-1

### High Speed Synchronous N-Channel MOSFET Drivers

#### FEATURES

- Wide  $V_{CC}$  Range: 6V to 9.5V
- 38V Maximum Input Supply Voltage
- Adaptive Shoot-Through Protection
- 2.4A Peak Pull-Up Current
- 5A Peak Pull-Down Current
- 8ns TG Fall Time Driving 3000pF Load
- 12ns TG Rise Time Driving 3000pF Load
- Separate Supply to Match PWM Controller
- Drives Dual N-Channel MOSFETs
- Undervoltage Lockout
- Thermally Enhanced MSOP Package

#### APPLICATIONS

- Distributed Power Architectures
- High Density Power Modules

#### DESCRIPTION

The LTC<sup>®</sup>4442 is a high frequency gate driver designed to drive two N-channel MOSFETs in a synchronous buck DC/DC converter topology. The powerful driver capability reduces switching losses in MOSFETs with high gate capacitance.

The LTC4442 features a separate supply for the input logic to match the signal swing of the controller IC. If the input signal is not being driven, the LTC4442 activates a shutdown mode that turns off both external MOSFETs. The input logic signal is internally level-shifted to the bootstrapped supply, which may function at up to 42V above ground.

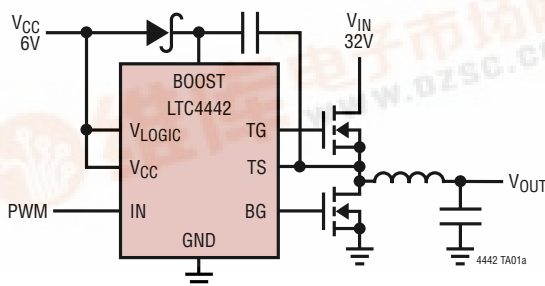
The LTC4442 contains undervoltage lockout circuits on both the driver and logic supplies that turn off the external MOSFETs when an undervoltage condition is present. The LTC4442 and LTC4442-1 have different undervoltage lockout thresholds to accommodate a wide variety of applications. An adaptive shoot-through protection feature is also built-in to prevent power loss resulting from MOSFET cross-conduction current.

The LTC4442/LTC4442-1 are available in the thermally enhanced 8-lead MSOP package.

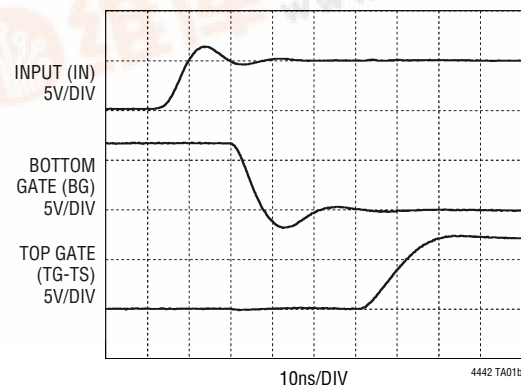
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#### TYPICAL APPLICATION

Synchronous Buck Converter Driver



LTC4442 Driving 3000pF Capacitive Loads



# LTC4442/LTC4442-1

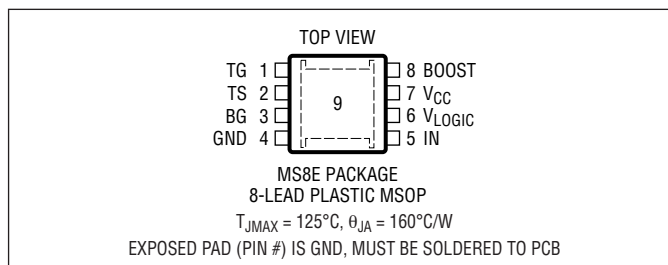
## ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage

$V_{CC}$	–0.3V to 10V
$V_{LOGIC}$	–0.3V to 10V
BOOST – TS	–0.3V to 10V
IN Voltage	–0.3V to 10V
BOOST Voltage	–0.3V to 42V
TS Voltage	–5V to 38V
TS + $V_{CC}$	42V
Driver Output TG (with Respect to TS)	–0.3V to 10V
Driver Output BG	–0.3V to 10V
Operating Temperature Range (Note 2)	–40°C to 85°C
Junction Temperature (Note 3)	125°C
Storage Temperature Range	–65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

## PIN CONFIGURATION



## ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4442EMS8E#PBF	LTC4442EMS8E#TRPBF	LTCTJ	8-Lead Plastic MSOP	–40°C to 85°C
LTC4442IMS8E#PBF	LTC4442IMS8E#TRPBF	LTCTJ	8-Lead Plastic MSOP	–40°C to 85°C
LTC4442EMS8E-1#PBF	LTC4442EMS8E-1#TRPBF	LTCXR	8-Lead Plastic MSOP	–40°C to 85°C
LTC4442IMS8E-1#PBF	LTC4442IMS8E-1#TRPBF	LTCXR	8-Lead Plastic MSOP	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. \*The temperature grade is identified by a label on the shipping container. Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreeel/>

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^{\circ}\text{C}$ .  $V_{CC} = V_{BOOST} = 7\text{V}$ ,  $V_{TS} = \text{GND} = 0\text{V}$ ,  $V_{LOGIC} = 5\text{V}$ , unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
<b>Logic Supply (<math>V_{LOGIC}</math>)</b>						
$V_{LOGIC}$	Operating Range		3		9.5	V
$I_{VLOGIC}$	DC Supply Current	IN = Floating		730	850	μA
UVLO	Undervoltage Lockout Threshold	$V_{LOGIC}$ Rising $V_{LOGIC}$ Falling Hysteresis	● 2.5 ● 2.4	2.75 2.65 100	3.0 2.9	V mV
<b>Gate Driver Supply (<math>V_{CC}</math>)</b>						
$V_{CC}$	Operating Range		6		9.5	V
$I_{VCC}$	DC Supply Current	IN = Floating		300	380	μA

**ELECTRICAL CHARACTERISTICS**

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V_{CC} = V_{BOOST} = 7\text{V}$ ,  $V_{TS} = \text{GND} = 0\text{V}$ ,  $V_{LOGIC} = 5\text{V}$ , unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
UVLO	Undervoltage Lockout Threshold	$V_{CC}$ Rising (LTC4442)	● 2.75	3.20	3.65	V
		$V_{CC}$ Falling (LTC4442)	● 2.60	3.04	3.50	V
		Hysteresis (LTC4442)		160		mV
		$V_{CC}$ Rising (LTC4442-1)	● 5.6	6.2	6.7	V
		$V_{CC}$ Falling (LTC4442-1)	● 4.7	5.3	5.8	V
		Hysteresis (LTC4442-1)		850		mV

**Bootstrapped Supply (BOOST – TS)**

$I_{BOOST}$	DC Supply Current	IN = Floating		325	400	$\mu\text{A}$
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**Input Signal (IN)**

$V_{IH(TG)}$	TG Turn-On Input Threshold	$V_{LOGIC} \geq 5\text{V}$ , IN Rising	● 3.0	3.5	4.0	V
		$V_{LOGIC} = 3.3\text{V}$ , IN Rising	● 1.9	2.2	2.6	V
$V_{IL(TG)}$	TG Turn-Off Input Threshold	$V_{LOGIC} \geq 5\text{V}$ , IN Falling		3.25		V
		$V_{LOGIC} = 3.3\text{V}$ , IN Falling		2.09		V
$V_{IH(BG)}$	BG Turn-On Input Threshold	$V_{LOGIC} \geq 5\text{V}$ , IN Falling	● 0.8	1.25	1.6	V
		$V_{LOGIC} = 3.3\text{V}$ , IN Falling	● 0.8	1.10	1.4	V
$V_{IL(BG)}$	BG Turn-Off Input Threshold	$V_{LOGIC} \geq 5\text{V}$ , IN Rising		1.50		V
		$V_{LOGIC} = 3.3\text{V}$ , IN Rising		1.21		V
$I_{IN(SD)}$	Maximum Current Into or Out of IN in Shutdown Mode	$V_{LOGIC} \geq 5\text{V}$ , IN Floating	200	300		$\mu\text{A}$
		$V_{LOGIC} = 3.3\text{V}$ , IN Floating	100	150		$\mu\text{A}$

**High Side Gate Driver Output (TG)**

$V_{OH(TG)}$	TG High Output Voltage	$I_{TG} = -10\text{mA}$ , $V_{OH(TG)} = V_{BOOST} - V_{TG}$		0.7		V
$V_{OL(TG)}$	TG Low Output Voltage	$I_{TG} = 100\text{mA}$ , $V_{OL(TG)} = V_{TG} - V_{TS}$		100		mV
$I_{PU(TG)}$	TG Peak Pull-Up Current		● 1.5	2.4		A
$I_{PD(TG)}$	TG Peak Pull-Down Current		● 1.5	2.4		A

**Low Side Gate Driver Output (BG)**

$V_{OH(BG)}$	BG High Output Voltage	$I_{BG} = -10\text{mA}$ , $V_{OH(BG)} = V_{CC} - V_{BG}$		0.7		V
$V_{OL(BG)}$	BG Low Output Voltage	$I_{BG} = 100\text{mA}$		100		mV
$I_{PU(BG)}$	BG Peak Pull-Up Current		● 1.4	2.4		A
$I_{PD(BG)}$	BG Peak Pull-Down Current		● 3.5	5.0		A

**Switching Time**

$t_{PLH(TG)}$	BG Low to TG High Propagation Delay			20		ns
$t_{PHL(TG)}$	IN Low to TG Low Propagation Delay			12		ns
$t_{PLH(BG)}$	TG Low to BG High Propagation Delay			20		ns
$t_{PHL(BG)}$	IN High to BG Low Propagation Delay			12		ns
$t_r(TG)$	TG Output Rise Time	10% – 90%, $C_L = 3\text{nF}$		12		ns
$t_f(TG)$	TG Output Fall Time	10% – 90%, $C_L = 3\text{nF}$		8		ns
$t_r(BG)$	BG Output Rise Time	10% – 90%, $C_L = 3\text{nF}$		12		ns
$t_f(BG)$	BG Output Fall Time	10% – 90%, $C_L = 3\text{nF}$		5		ns

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** The LTC4442/LTC4442-1 are guaranteed to meet specifications from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ . The LTC4442E/LTC4442E-1 are guaranteed to meet specifications from  $0^\circ\text{C}$  to  $85^\circ\text{C}$  with specifications over the  $-40^\circ\text{C}$  to  $85^\circ\text{C}$  operating temperature range assured by design, characterization and correlation with statistical process controls.

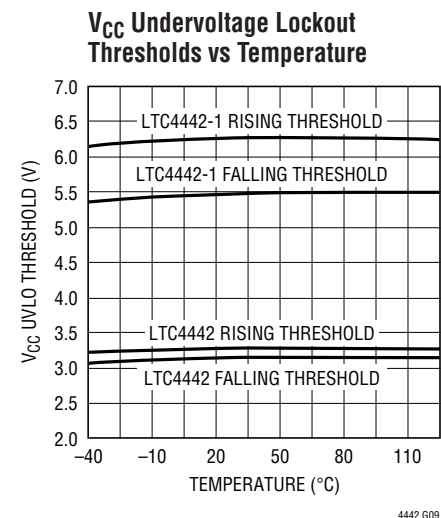
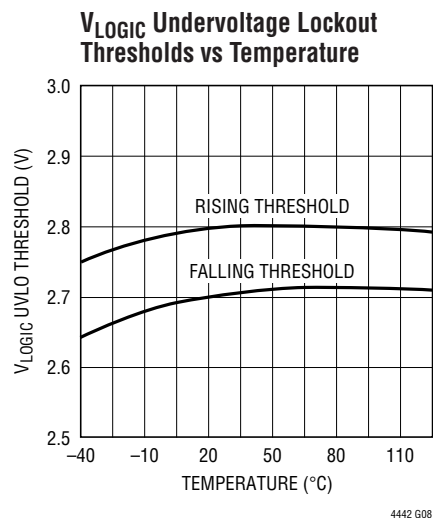
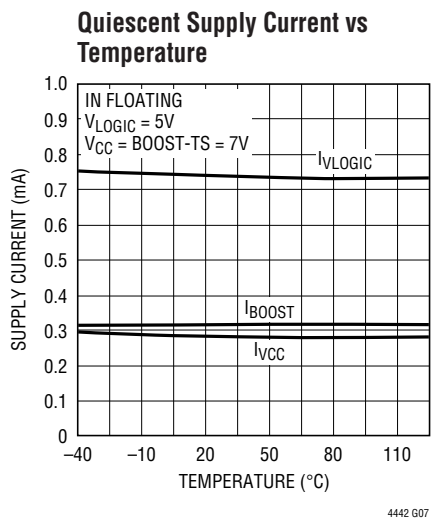
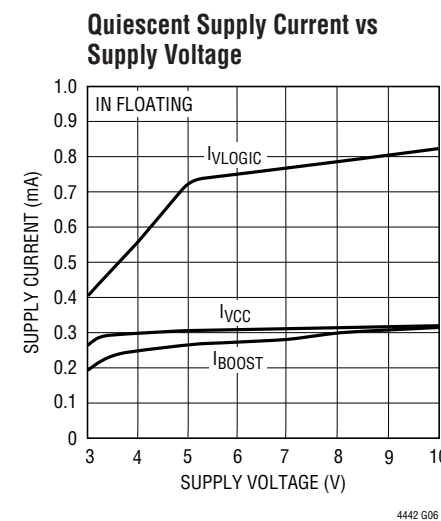
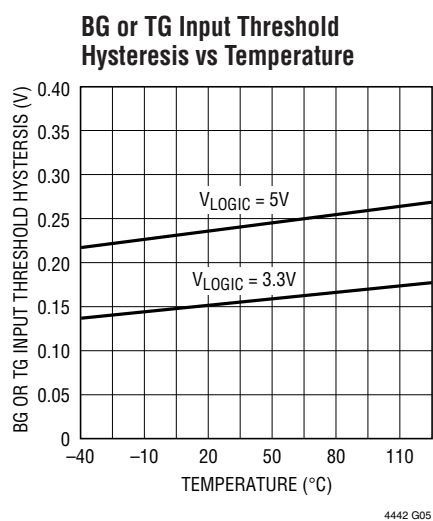
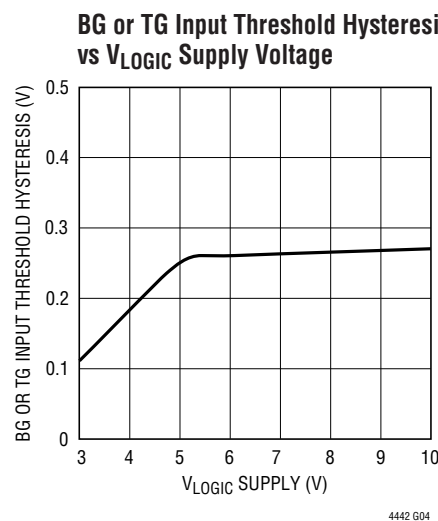
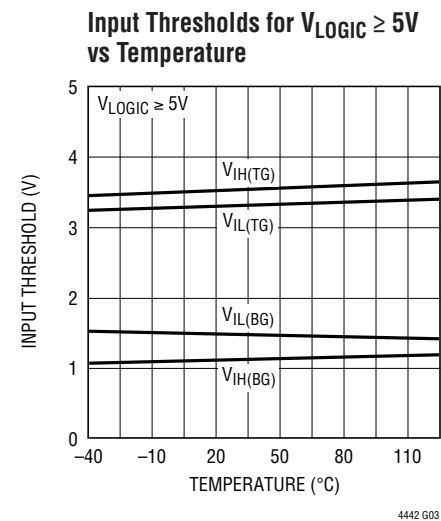
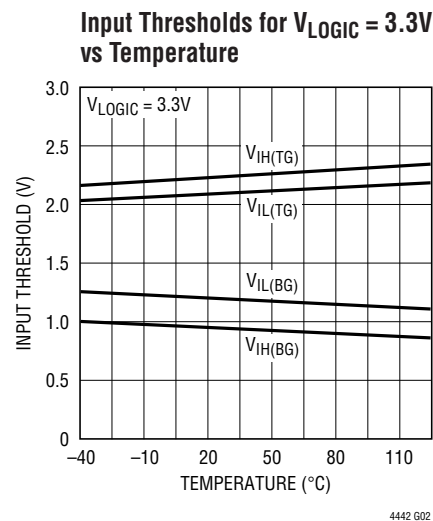
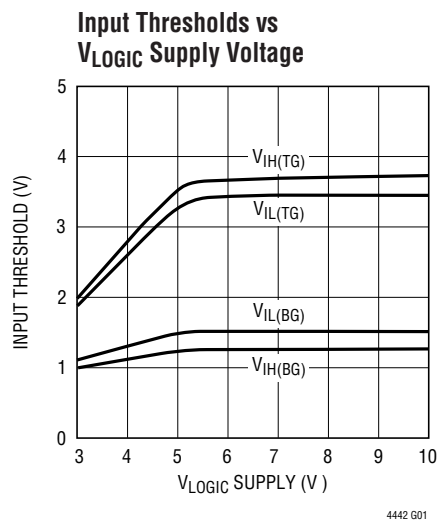
$T_J$  is calculated from the ambient temperature  $T_A$  and power dissipation  $P_D$  according to the following formula:

$$T_J = T_A + (P_D \cdot \theta_{JA}^\circ\text{C/W})$$

**Note 3:** This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed  $125^\circ\text{C}$  when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

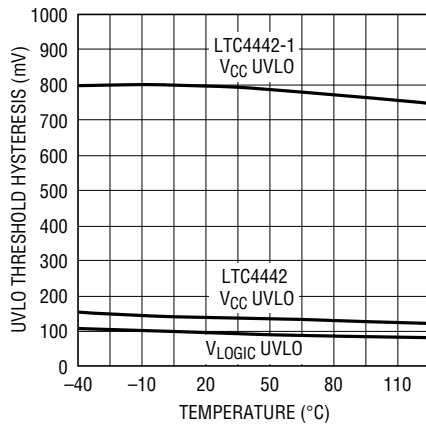
# LTC4442/LTC4442-1

## TYPICAL PERFORMANCE CHARACTERISTICS



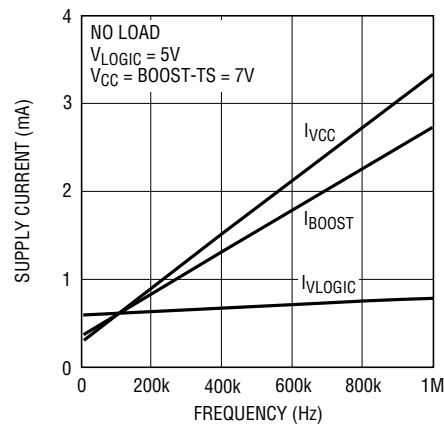
## TYPICAL PERFORMANCE CHARACTERISTICS

Undervoltage Lockout Threshold Hysteresis vs Temperature



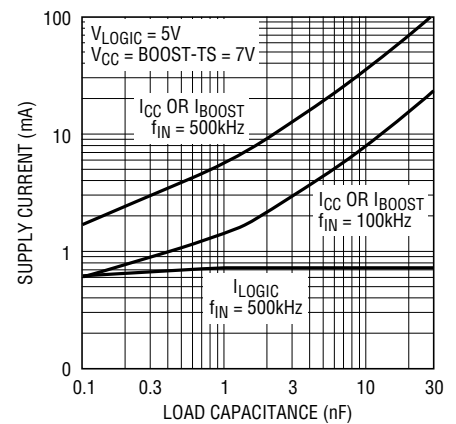
4442 G10

Switching Supply Current vs Input Frequency

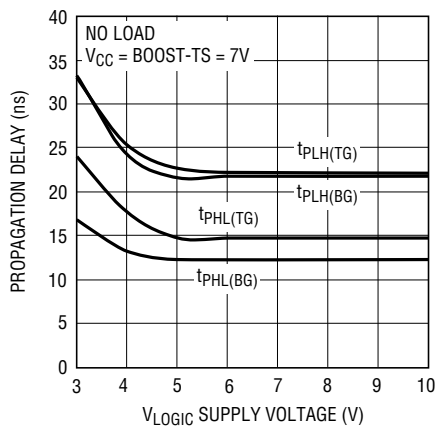


4442 G11

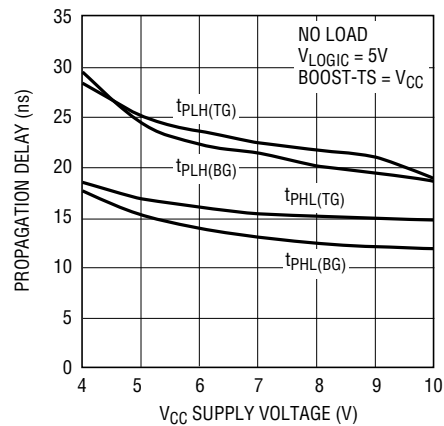
Switching Supply Current vs Load Capacitance



4442 G12

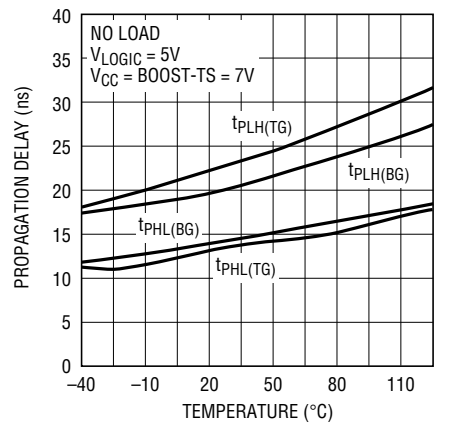
Propagation Delay vs  $V_{LOGIC}$  Supply Voltage

4442 G13

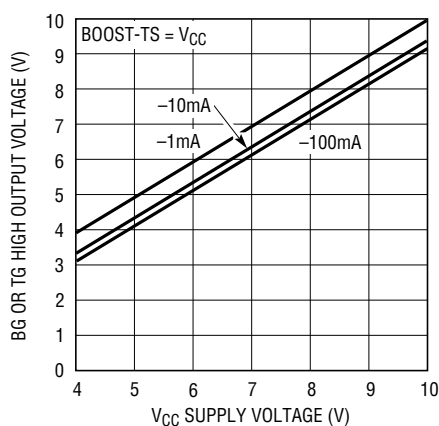
Propagation Delay vs  $V_{CC}$  Supply Voltage

4442 G14

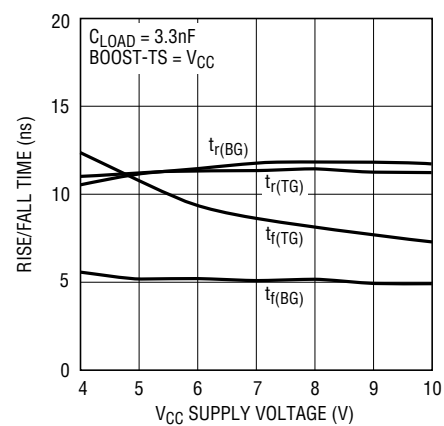
Propagation Delay vs Temperature



4442 G15

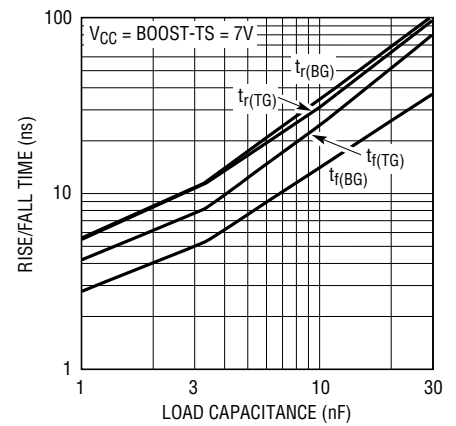
Output High Voltage vs  $V_{CC}$  Supply Voltage

4442 G16

Rise and Fall Time vs  $V_{CC}$  Supply Voltage

4442 G17

Rise and Fall Time vs Load Capacitance



4442 G18

## PIN FUNCTIONS

**TG (Pin 1):** High Side Gate Driver Output (Top Gate). This pin swings between TS and BOOST.

**TS (Pin 2):** High Side MOSFET Source Connection (Top Source).

**BG (Pin 3):** Low Side Gate Driver Output (Bottom Gate). This pin swings between  $V_{CC}$  and GND.

**GND (Pin 4):** Chip Ground.

**IN (Pin 5):** Input Signal. Input referenced to an internal supply powered by  $V_{LOGIC}$  (Pin 6) and referenced to GND (Pin 4). If this pin is floating, an internal resistive divider triggers a shutdown mode in which both BG (Pin 3) and TG (Pin 1) are pulled low. Trace capacitance on this pin should be minimized to keep the shutdown time low.

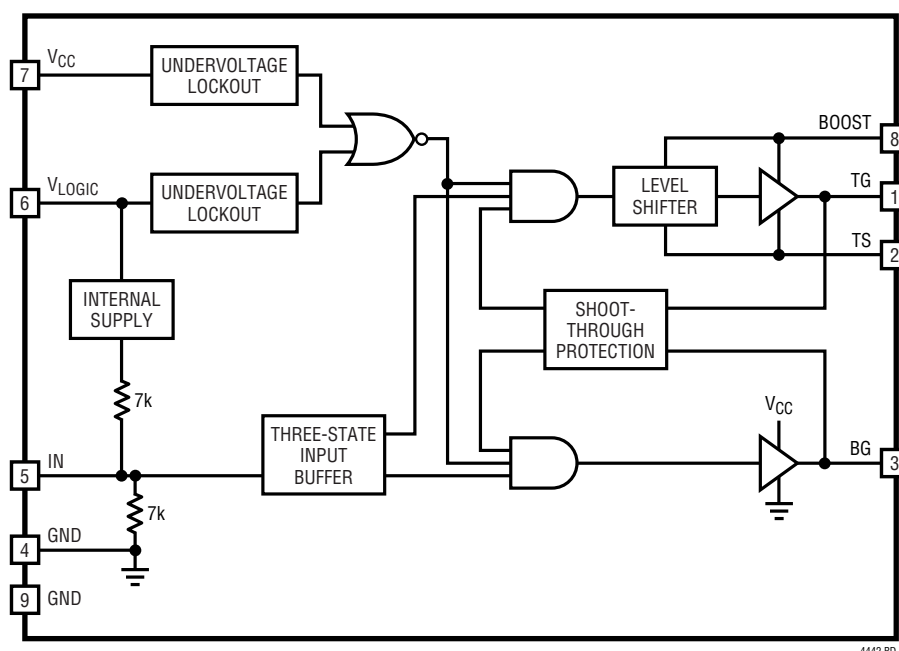
**$V_{LOGIC}$  (Pin 6):** Logic Supply. This pin powers the input buffer and logic. Connect this pin to the power supply of the controller that is driving IN (Pin 5) to match input thresholds or to  $V_{CC}$  (Pin 7) to simplify PCB routing.

**$V_{CC}$  (Pin 7):** Output Driver Supply. This pin powers the low side gate driver output directly and the high side gate driver output through an external diode connected between this pin and BOOST (Pin 8). A low ESR ceramic bypass capacitor should be tied between this pin and GND (Pin 4).

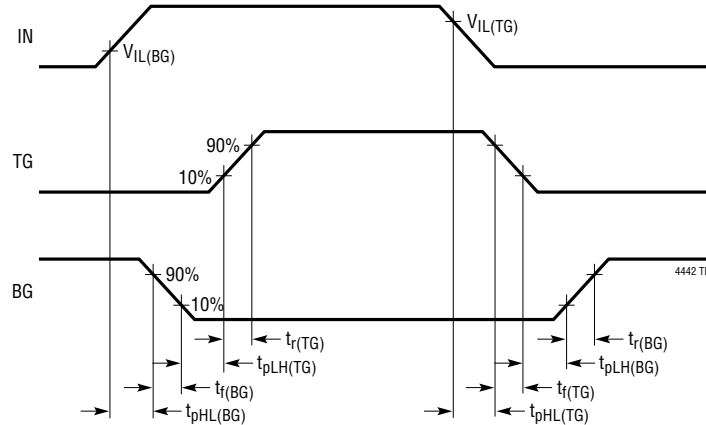
**BOOST (Pin 8):** High Side Bootstrapped Supply. An external capacitor should be tied between this pin and TS (Pin 2). Normally, a bootstrap diode is connected between  $V_{CC}$  (Pin 7) and this pin. Voltage swing at this pin is from  $V_{CC} - V_D$  to  $V_{IN} + V_{CC} - V_D$ , where  $V_D$  is the forward voltage drop of the bootstrap diode.

**Exposed Pad (Pin 9):** Ground. Must be electrically connected to GND (Pin 4) and soldered to PCB ground for optimal thermal performance.

## BLOCK DIAGRAM



## TIMING DIAGRAM



## OPERATION

### Overview

The LTC4442 receives a ground-referenced, low voltage digital input signal to drive two N-channel power MOSFETs in a synchronous buck power supply configuration. The gate of the low side MOSFET is driven either to  $V_{CC}$  or GND, depending on the state of the input. Similarly, the gate of the high side MOSFET is driven to either BOOST or TS by a supply bootstrapped off of the switch node (TS).

### Input Stage

The LTC4442 employs a unique three-state input stage with transition thresholds that are proportional to the  $V_{LOGIC}$  supply. The  $V_{LOGIC}$  supply can be tied to the controller IC's power supply so that the input thresholds will match those of the controller's output signal. Alternatively,  $V_{LOGIC}$  can be tied to  $V_{CC}$  to simplify routing. An internal voltage regulator in the LTC4442 limits the input threshold values for  $V_{LOGIC}$  supply voltages greater than 5V.

The relationship between the transition thresholds and the three input states of the LTC4442 is illustrated in Figure 1. When the voltage on IN is greater than the threshold  $V_{IH(TG)}$ , TG is pulled up to BOOST, turning the high side MOSFET on. This MOSFET will stay on until IN falls below  $V_{IL(TG)}$ . Similarly, when IN is less than  $V_{IH(BG)}$ , BG is pulled up to  $V_{CC}$ , turning the low side (synchronous) MOSFET on. BG will stay high until IN increases above the threshold  $V_{IL(BG)}$ .

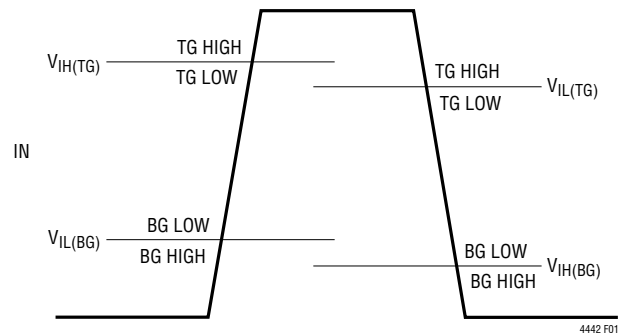


Figure 1. Three-State Input Operation

The thresholds are positioned to allow for a region in which both BG and TG are low. An internal resistive divider will pull IN into this region if the signal driving the IN pin goes into a high impedance state.

One application of this three-state input is to keep both of the power MOSFETs off while an undervoltage condition exists on the controller IC power supply. This can be accomplished by driving the IN pin with a logic buffer that has an enable pin. With the enable pin of the buffer tied to the power good pin of the controller IC, the logic buffer output will remain in a high impedance state until the controller confirms that its supply is not in an undervoltage state. The three-state input of the LTC4442 will therefore pull IN into the region where TG and BG are low until the controller has enough voltage to operate predictably.



## OPERATION

The hysteresis between the corresponding  $V_{IH}$  and  $V_{IL}$  voltage levels eliminates false triggering due to noise during switch transitions; however, care should be taken to keep noise from coupling into the IN pin, particularly in high frequency, high voltage applications.

### Undervoltage Lockout

The LTC4442 contains undervoltage lockout detectors that monitor both the  $V_{CC}$  and  $V_{LOGIC}$  supplies. When  $V_{CC}$  falls below 3.04V or  $V_{LOGIC}$  falls below 2.65V, the output pins BG and TG are pulled to GND and TS, respectively. This turns off both of the external MOSFETs. When  $V_{CC}$  and  $V_{LOGIC}$  have adequate supply voltage for the LTC4442 to operate reliably, normal operation will resume.

### Adaptive Shoot-Through Protection

Internal adaptive shoot-through protection circuitry monitors the voltages on the external MOSFETs to ensure that they do not conduct simultaneously. The LTC4442 does not allow the bottom MOSFET to turn on until the gate-source voltage on the top MOSFET is sufficiently low, and vice-versa. This feature improves efficiency by eliminating cross-conduction current from flowing from the  $V_{IN}$  supply through the MOSFETs to ground during a switch transition.

### Output Stage

A simplified version of the LTC4442's output stage is shown in Figure 2. The pull-up device on both the BG and TG outputs is an NPN bipolar junction transistor (Q1 and Q2). The BG and TG outputs are pulled up to within an NPN  $V_{BE}$  (~0.7V) of their positive rails ( $V_{CC}$  and BOOST, respectively). Both BG and TG have N-channel MOSFET pull-down devices (N1 and N2) which pull BG and TG down to their negative rails, GND and TS. An additional NPN bipolar junction transistor (Q3) is present on BG to increase its pull-down drive current capacity. The large voltage swing of the BG and TG output pins is important in driving external power MOSFETs, whose  $R_{DS(ON)}$  is inversely proportional to its gate overdrive voltage ( $V_{GS} - V_{TH}$ ).

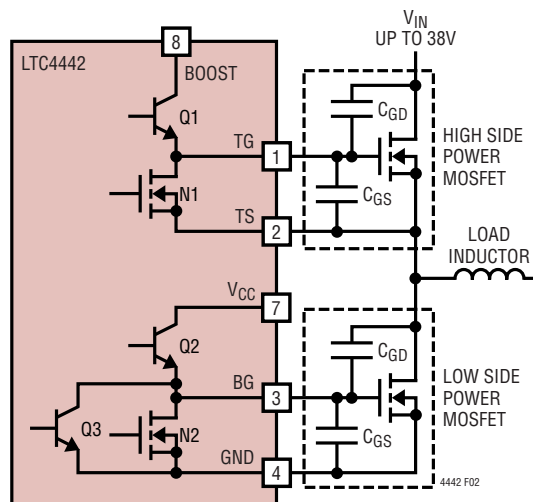


Figure 2. Capacitance Seen by BG and TG During Switching

### Rise/Fall Time

Since the power MOSFET generally accounts for the majority of power loss in a converter, it is important to quickly turn it on and off, thereby minimizing the transition time and power loss. The LTC4442's peak pull-up current of 2.4A for both BG and TG (Q1 and Q2) produces a rapid turn-on transition for the MOSFETs. This high current is capable of driving a 3nF load with a 12ns rise time.

It is also important to turn the power MOSFETs off quickly to minimize power loss due to transition time; however, an additional benefit of a strong pull-down on the driver outputs is the prevention of cross-conduction current. For example, when BG turns the low-side power MOSFET off and TG turns the high-side power MOSFET on, the voltage on the TS pin will rise to  $V_{IN}$  very rapidly. This high frequency positive voltage transient will couple through the  $C_{GD}$  capacitance of the low side power MOSFET to the BG pin. If the BG pin is not held down sufficiently, the voltage on the BG pin will rise above the threshold voltage of the low side power MOSFET, momentarily turning it back on. As a result, both the high side and low side MOSFETs will be conducting, which will cause significant cross-conduction current to flow through the MOSFETs from  $V_{IN}$  to ground, thereby introducing substantial power loss. A similar effect occurs on TG due to the  $C_{GS}$  and  $C_{GD}$  capacitances of the high side MOSFET.



## OPERATION

The LTC4442's powerful parallel combination of the N-channel MOSFET (N2) and NPN (Q3) on the BG pull-down generates a phenomenal 5ns fall time on BG while driving a 3nF load. Similarly, the 1Ω pull-down MOSFET (N1) on

TG results in a rapid 8ns fall time with a 3nF load. These powerful pull-down devices minimize the power loss associated with MOSFET turn-off time and cross-conduction current.

## APPLICATIONS INFORMATION

### Power Dissipation

To ensure proper operation and long-term reliability, the LTC4442 must not operate beyond its maximum temperature rating. Package junction temperature can be calculated by:

$$T_J = T_A + (P_D)(\theta_{JA})$$

where:

$T_J$  = Junction temperature

$T_A$  = Ambient temperature

$P_D$  = Power dissipation

$\theta_{JA}$  = Junction-to-ambient thermal resistance

Power dissipation consists of standby, switching and capacitive load power losses:

$$P_D = P_{DC} + P_{AC} + P_{QG}$$

where:

$P_{DC}$  = Quiescent power loss

$P_{AC}$  = Internal switching loss at input frequency  $f_{IN}$

$P_{QG}$  = Loss due turning on and off the external MOSFET with gate charge  $Q_G$  at frequency  $f_{IN}$

The LTC4442 consumes very little quiescent current. The DC power loss at  $V_{LOGIC} = 5V$  and  $V_{CC} = V_{BOOST} - TS = 7V$  is only  $(730\mu A)(5V) + (625\mu A)(7V) = 8mW$ .

At a particular switching frequency, the internal power loss increases due to both AC currents required to charge and discharge internal nodal capacitances and cross-conduction currents in the internal logic gates. The sum of the quiescent current and internal switching current with no load are shown in the Typical Performance Characteristics plot of Switching Supply Current vs Input Frequency.

The gate charge losses are primarily due to the large AC currents required to charge and discharge the capacitance of the external MOSFETs during switching. For identical pure capacitive loads  $C_{LOAD}$  on TG and BG at switching frequency  $f_{IN}$ , the load losses would be:

$$P_{CLOAD} = (C_{LOAD})(f_{IN})[(V_{BOOST} - TS)^2 + (V_{CC})^2]$$

In a typical synchronous buck configuration,  $V_{BOOST} - TS$  is equal to  $V_{CC} - V_D$ , where  $V_D$  is the forward voltage drop across the diode between  $V_{CC}$  and BOOST. If this drop is small relative to  $V_{CC}$ , the load losses can be approximated as:

$$P_{CLOAD} \approx 2(C_{LOAD})(f_{IN})(V_{CC})^2$$

Unlike a pure capacitive load, a power MOSFET's gate capacitance seen by the driver output varies with its  $V_{GS}$  voltage level during switching. A MOSFET's capacitive load power dissipation can be calculated using its gate charge,  $Q_G$ . The  $Q_G$  value corresponding to the MOSFET's  $V_{GS}$  value ( $V_{CC}$  in this case) can be readily obtained from the manufacturer's  $Q_G$  vs  $V_{GS}$  curves. For identical MOSFETs on TG and BG:

$$P_{QG} \approx 2(V_{CC})(Q_G)(f_{IN})$$

To avoid damaging junction temperatures due to power dissipation, the LTC4442 includes a temperature monitor that will pull BG and TG low if the junction temperature exceeds 160°C. Normal operation will resume when the junction temperature cools to less than 135°C.

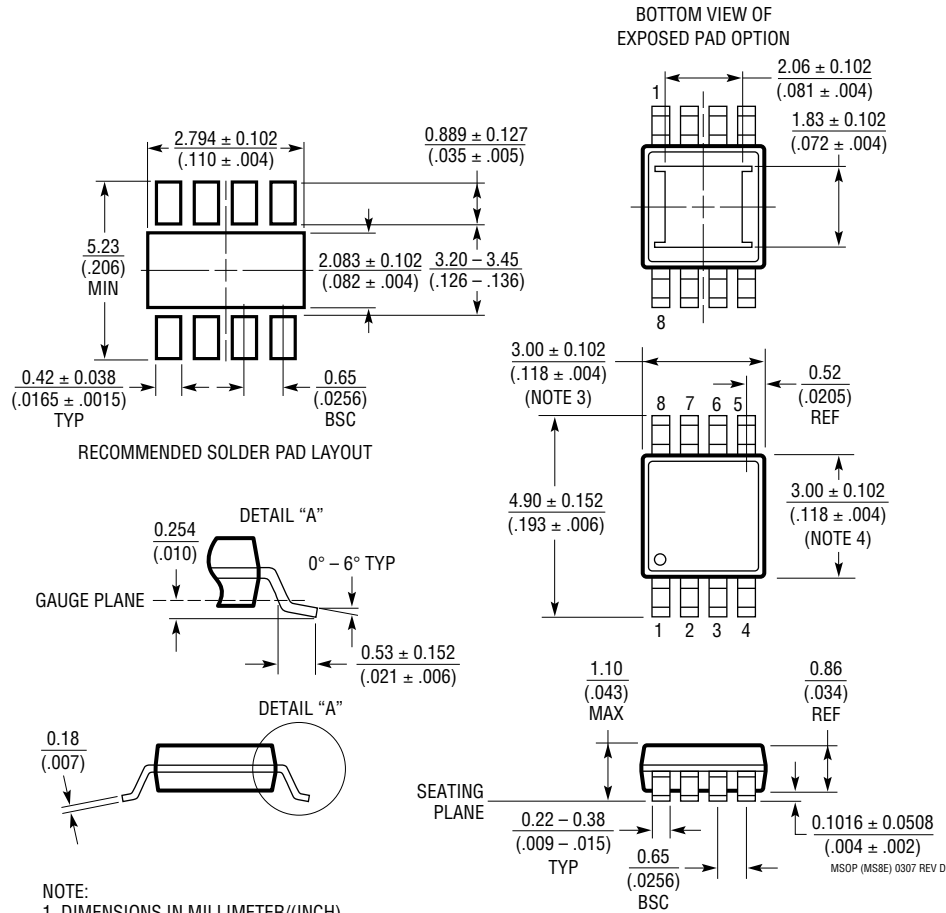
### Bypassing and Grounding

The LTC4442 requires proper bypassing on the  $V_{LOGIC}$ ,  $V_{CC}$  and  $V_{BOOST} - TS$  supplies due to its high speed switching (nanoseconds) and large AC currents (Amperes). Careless component placement and PCB trace routing may cause excessive ringing and undershoot/overshoot.



## PACKAGE DESCRIPTION

### MS8E Package 8-Lead Plastic MSOP, Exposed Die Pad (Reference LTC DWG # 05-08-1662 Rev D)



**NOTE:**

1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.  
MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED  $0.152\text{mm}$  ( $.006$ ") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.  
INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED  $0.152\text{mm}$  ( $.006$ ") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE  $0.102\text{mm}$  ( $.004$ ") MAX

# LTC4442/LTC4442-1

## RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1154	High Side Micropower MOSFET Driver	Internal Charge Pump, 4.5V to 18V Supply Range
LTC1155	Dual Micropower High/Low Side Driver	Internal Charge Pump, 4.5V to 18V Supply Range
LT <sup>®</sup> 1161	Quad Protected High Side MOSFET Driver	8V to 48V Supply Range, $t_{ON} = 200\mu s$ , $t_{OFF} = 28\mu s$
LTC1163	Triple 1.8V to 6V High Side MOSFET Driver	1.8V to 6V Supply Range, $t_{ON} = 95\mu s$ , $t_{OFF} = 45\mu s$
LTC1693	High Speed Single/Dual N-Channel MOSFET Driver	CMOS Compatible Input, $V_{CC}$ Range: 4.5V to 13.2V
LTC3900	Synchronous Rectifier Driver for Forward Converter	Pulse Transformer Synchronization Input
LTC3901	Secondary Side Synchronous Driver for Push-Pull and Full-Bridge Converter	Gate Drive Transformer Synchronous Input
LTC4440	High Speed, High Voltage, High Side Gate Driver	Wide Operating $V_{IN}$ Range: Up to 80V DC, 100V Transient
LTC4441	6A MOSFET Driver	Adjustable Gate Drive from 5V to 8V, $5V \leq V_{IN} \leq 28V$
LTC7510	Digital DC/DC Controller with PMBus Interface	Digital Controller, PMBus Serial Interface, 150kHz to 2MHz Switching Frequency