



**ALPHA & OMEGA**  
SEMICONDUCTOR



**AOD4185**

**P-Channel Enhancement Mode Field Effect Transistor**

**General Description**

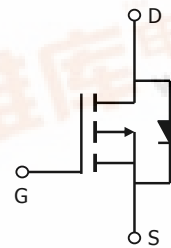
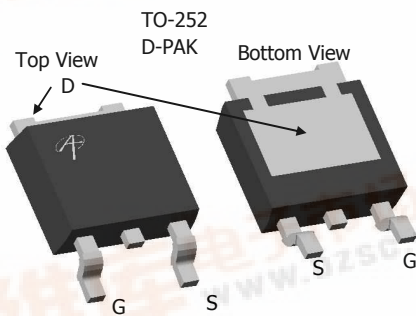
The AOD4185 uses advanced trench technology to provide excellent  $R_{DS(ON)}$  and low gate charge. With the excellent thermal resistance of the DPAK package, this device is well suited for high current applications.

- RoHS Compliant
- Halogen Free\*

**Features**

- $V_{DS}$  (V) = -40V
- $I_D$  = -40A ( $V_{GS}$  = -10V)
- $R_{DS(ON)}$  < 15m $\Omega$  ( $V_{GS}$  = -10V)
- $R_{DS(ON)}$  < 20m $\Omega$  ( $V_{GS}$  = -4.5V)

**100% UIS Tested!**  
**100% Rg Tested!**



**Absolute Maximum Ratings  $T_C=25^\circ\text{C}$  unless otherwise noted**

Parameter	Symbol	Maximum	Units	
Drain-Source Voltage	$V_{DS}$	-40	V	
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V	
Continuous Drain Current <sup>B,H</sup>	$I_D$	$T_C=25^\circ\text{C}$	A	
		$T_C=100^\circ\text{C}$		-31
		Pulsed Drain Current <sup>C</sup>		$I_{DM}$
Avalanche Current <sup>C</sup>	$I_{AR}$	-42		
Repetitive avalanche energy $L=0.1\text{mH}$ <sup>C</sup>	$E_{AR}$	88	mJ	
Power Dissipation <sup>B</sup>	$P_D$	$T_C=25^\circ\text{C}$	W	
		$T_C=100^\circ\text{C}$		31
Power Dissipation <sup>A</sup>	$P_{DSM}$	$T_A=25^\circ\text{C}$	2.5	
		$T_A=70^\circ\text{C}$	1.6	
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 175	$^\circ\text{C}$	

**Thermal Characteristics**

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient <sup>A,G</sup>	$R_{\theta JA}$	15	20	$^\circ\text{C/W}$
Maximum Junction-to-Ambient <sup>A,G</sup>		Steady-State	41	
Maximum Junction-to-Case <sup>D,F</sup>	$R_{\theta JC}$	2	2.4	$^\circ\text{C/W}$



Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> =-250μA, V <sub>GS</sub> =0V	-40			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =-40V, V <sub>GS</sub> =0V T <sub>J</sub> =55°C			-1 -5	μA
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> = ±20V			±100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> I <sub>D</sub> =-250μA	-1.7	-1.9	-3	V
I <sub>D(ON)</sub>	On state drain current	V <sub>GS</sub> =-10V, V <sub>DS</sub> =-5V	-115			A
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =-10V, I <sub>D</sub> =-20A T <sub>J</sub> =125°C		12.5 19	15 23	mΩ
		V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-15A		16	20	
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =-5V, I <sub>D</sub> =-20A		50		S
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =-1A, V <sub>GS</sub> =0V		-0.72	-1	V
I <sub>S</sub>	Maximum Body-Diode Continuous Current				-20	A
<b>DYNAMIC PARAMETERS</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =-20V, f=1MHz		2550		pF
C <sub>oss</sub>	Output Capacitance			280		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			190		pF
R <sub>g</sub>	Gate resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1MHz	2.5	4	6	Ω
<b>SWITCHING PARAMETERS</b>						
Q <sub>g</sub> (-10V)	Total Gate Charge	V <sub>GS</sub> =-10V, V <sub>DS</sub> =-20V, I <sub>D</sub> =-20A		42	55	nC
Q <sub>g</sub> (-4.5V)	Total Gate Charge			18.6		
Q <sub>gs</sub>	Gate Source Charge			7		nC
Q <sub>gd</sub>	Gate Drain Charge			8.6		nC
t <sub>D(on)</sub>	Turn-On DelayTime	V <sub>GS</sub> =-10V, V <sub>DS</sub> =-20V, R <sub>L</sub> =1Ω, R <sub>GEN</sub> =3Ω		9.4		ns
t <sub>r</sub>	Turn-On Rise Time			20		ns
t <sub>D(off)</sub>	Turn-Off DelayTime			55		ns
t <sub>f</sub>	Turn-Off Fall Time			30		ns
t <sub>rr</sub>	Body Diode Reverse Recovery Time		I <sub>F</sub> =-20A, dI/dt=100A/μs		38	49
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> =-20A, dI/dt=100A/μs		47		nC

A: The value of R<sub>θJA</sub> is measured with the device in a still air environment with T<sub>A</sub>=25°C. The power dissipation P<sub>DSM</sub> and current rating I<sub>DSM</sub> are based on T<sub>J(MAX)</sub>=150°C, using steady state junction-to-ambient thermal resistance.

B: The power dissipation P<sub>D</sub> is based on T<sub>J(MAX)</sub>=175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C: Repetitive rating, pulse width limited by junction temperature T<sub>J(MAX)</sub>=175°C.

D: The R<sub>θJA</sub> is the sum of the thermal impedance from junction to case R<sub>θJC</sub> and case to ambient.

E: The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.

F: These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T<sub>J(MAX)</sub>=175°C. The SOA curve provides a single pulse rating.

G: These tests are performed with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25°C.

H: The maximum current rating is limited by bond-wires.

\*This device is guaranteed green after data code 8X11 (Sep 1<sup>ST</sup> 2008).

Rev1: Oct 2008

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

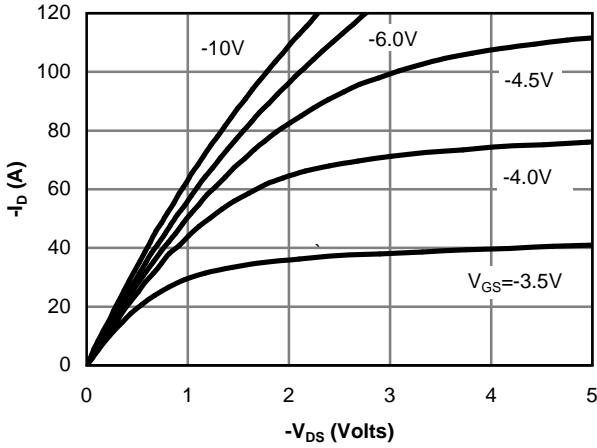


Figure 1: On-Region Characteristics

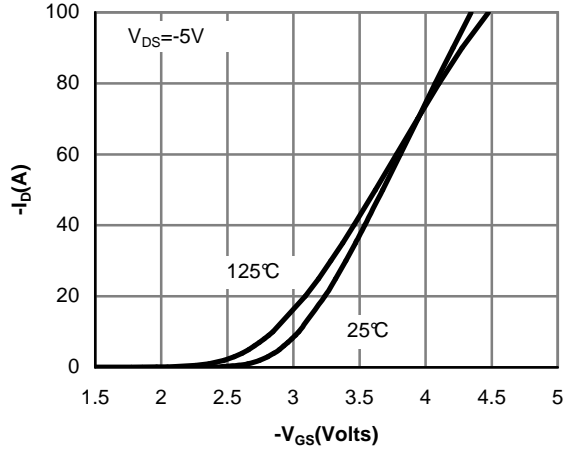


Figure 2: Transfer Characteristics

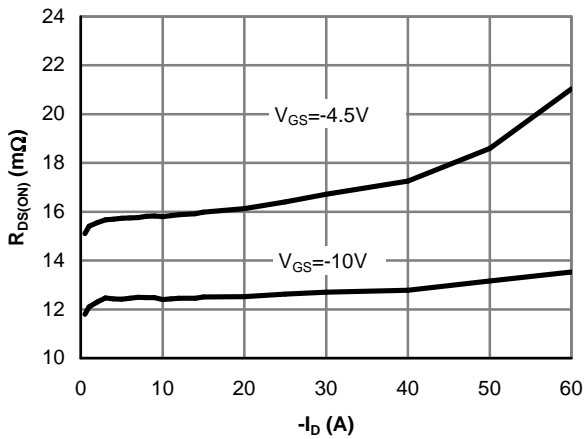


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

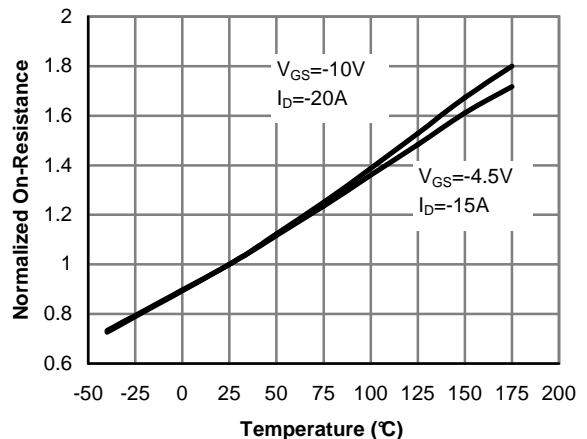


Figure 4: On-Resistance vs. Junction Temperature

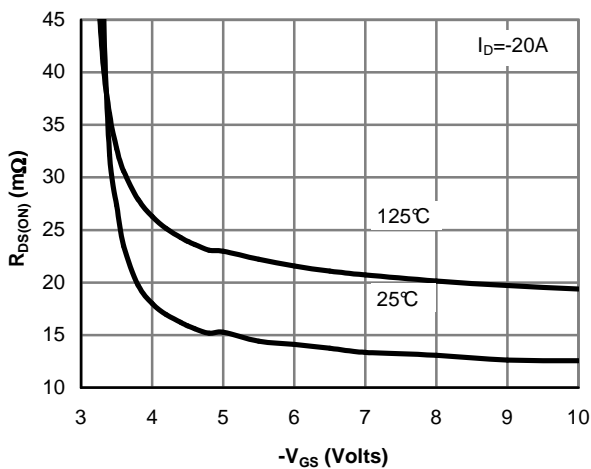


Figure 5: On-Resistance vs. Gate-Source Voltage

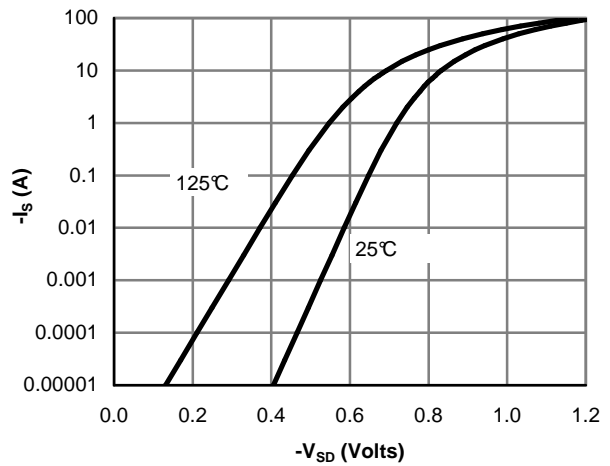


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

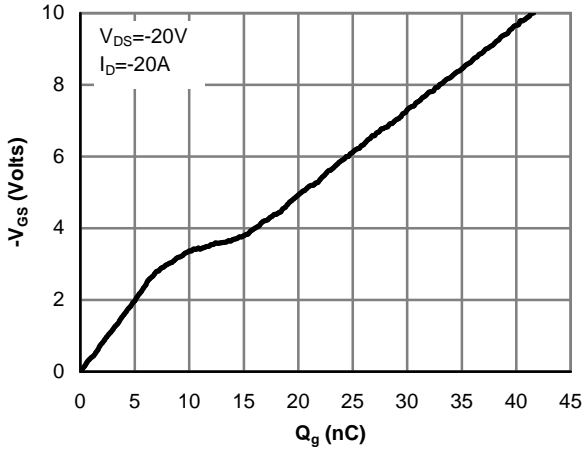


Figure 7: Gate-Charge Characteristics

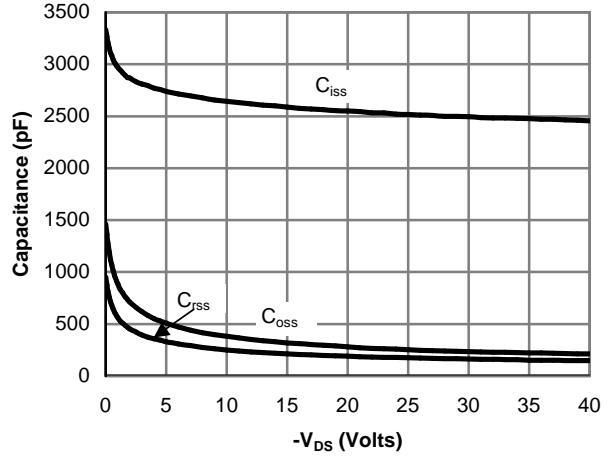


Figure 8: Capacitance Characteristics

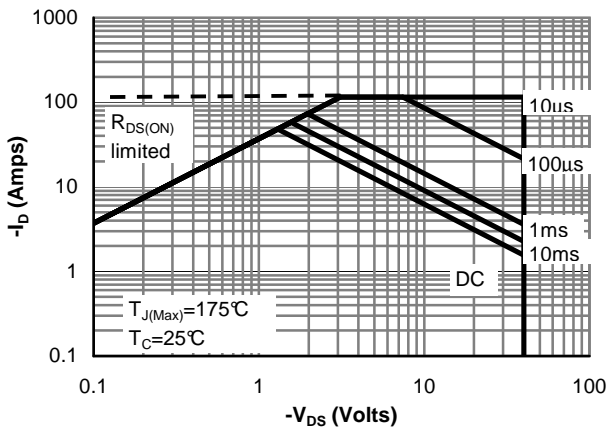


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

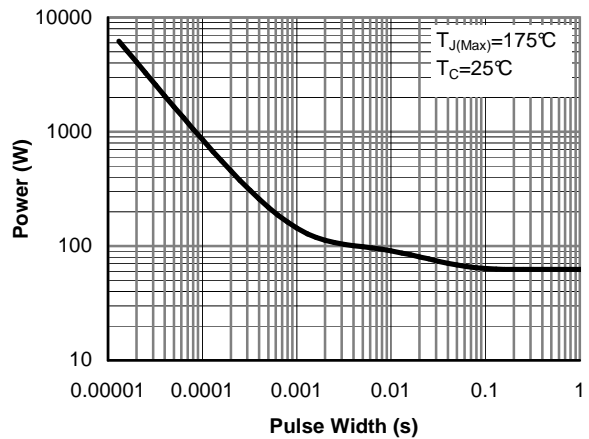


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

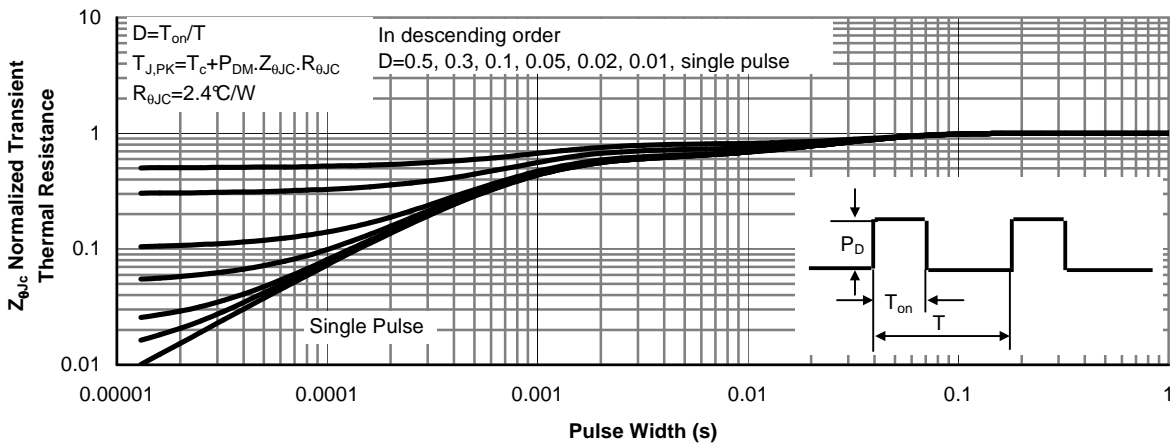


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

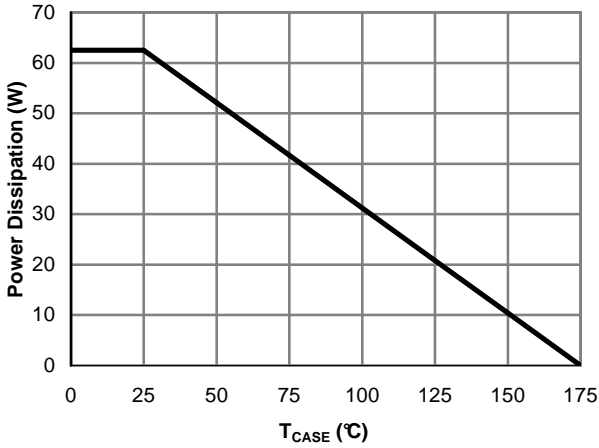


Figure 12: Power De-rating (Note B)

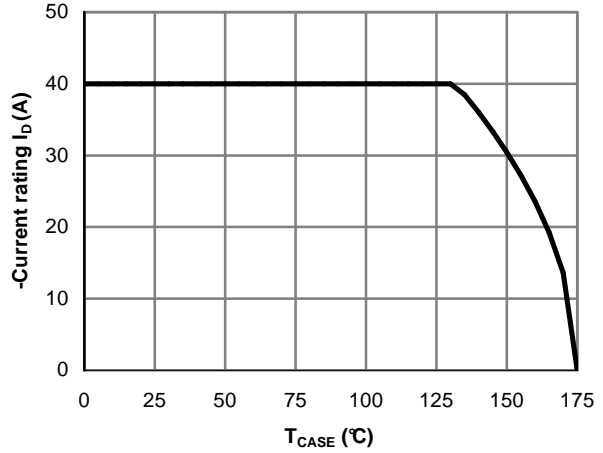


Figure 13: Current De-rating (Note B)

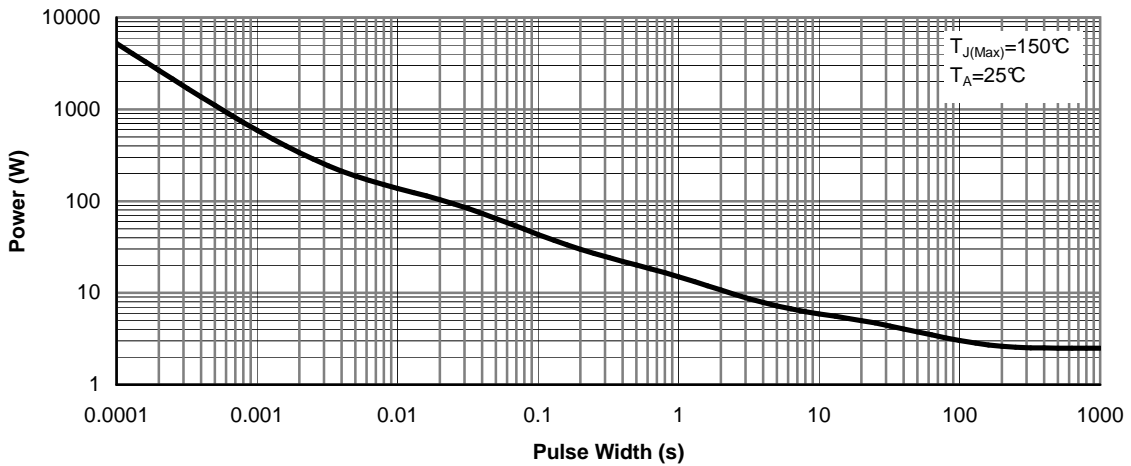


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note G)

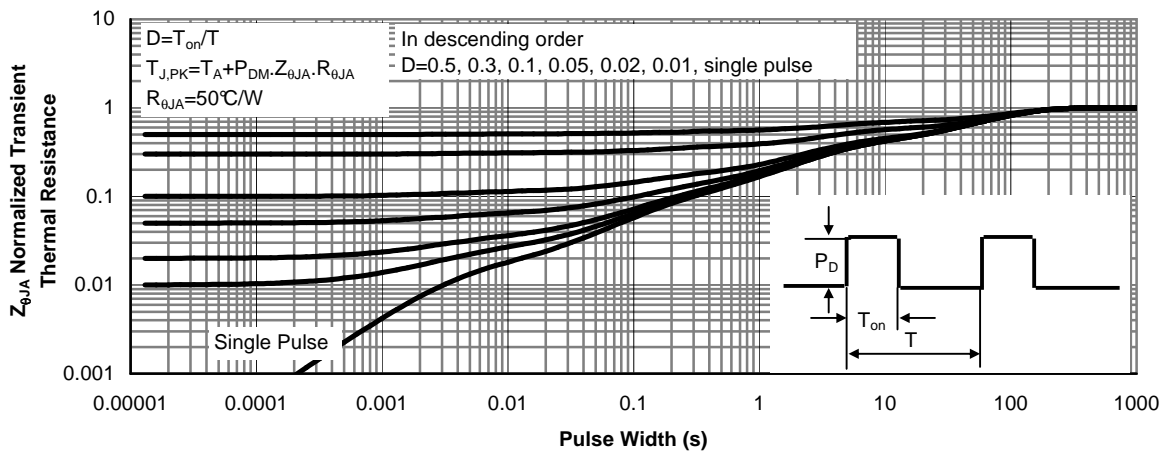
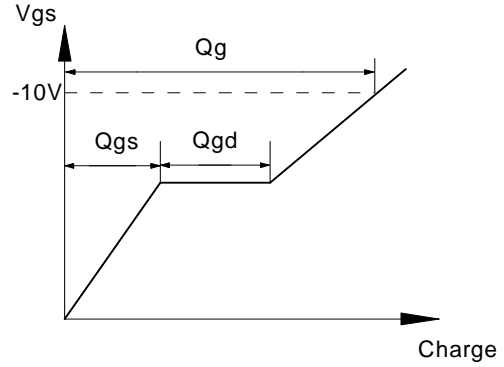
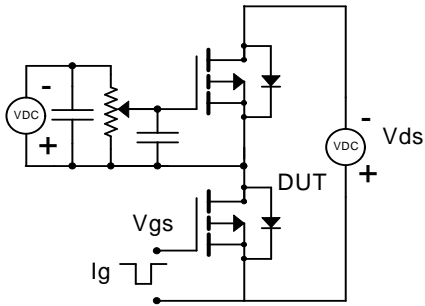
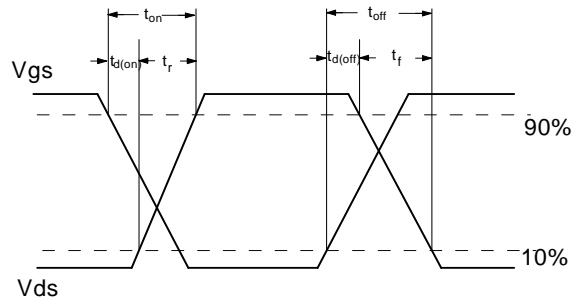
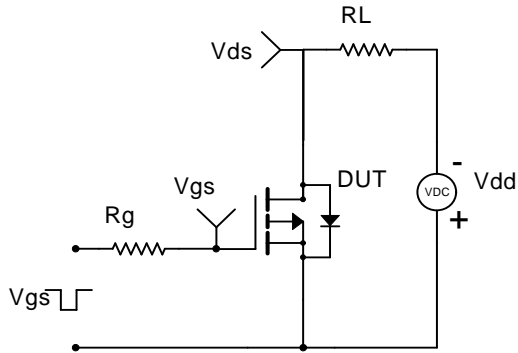


Figure 15: Normalized Maximum Transient Thermal Impedance (Note G)

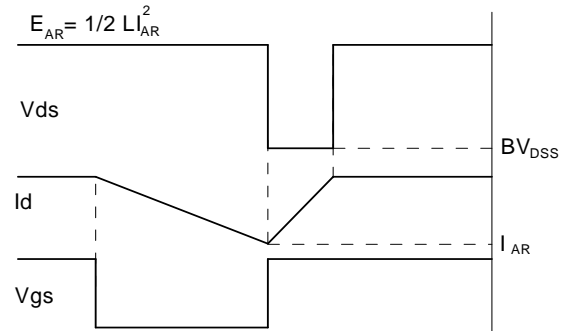
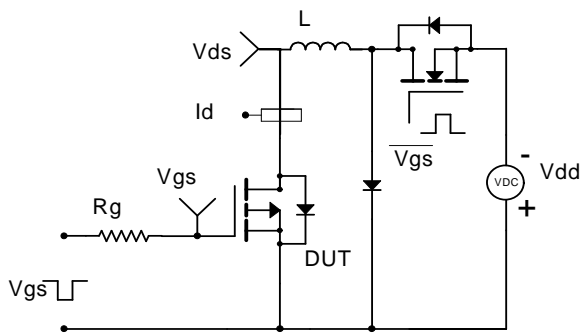
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

