



ALPHA & OMEGA
SEMICONDUCTOR



AOD496A N-Channel Enhancement Mode Field Effect Transistor

General Description

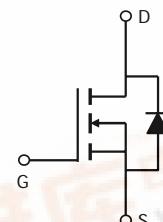
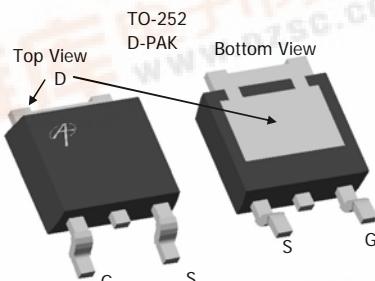
The AOD496A uses advanced trench technology to provide excellent $R_{DS(ON)}$ with low gate charge. This device is suitable for high side switch in SMPS and general purpose applications.

- RoHS Compliant
- Halogen Free

Features

V_{DS} (V) = 30V
 I_D = 57A (V_{GS} = 10V)
 $R_{DS(ON)}$ < 9mΩ (V_{GS} = 10V)
 $R_{DS(ON)}$ < 14mΩ (V_{GS} = 4.5V)

100% UIS Tested!
100% R_g Tested!



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current	I_D	57	A
		40	
Pulsed Drain Current ^C	I_{DM}	100	
Continuous Drain Current	I_{DSM}	11	A
		9	
Avalanche Current ^C	I_{AR}	20	A
Repetitive avalanche energy $L=0.1\text{mH}^C$	E_{AR}	20	mJ
Power Dissipation ^B	P_D	50	W
		25	
Power Dissipation ^A	P_{DSM}	2.3	W
		1.5	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 175	°C

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	18	22	°C/W
Maximum Junction-to-Ambient ^{A,D}		44	55	°C/W
Maximum Junction-to-Case	$R_{\theta JC}$	2.4	3	°C/W

Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D=250\mu\text{A}, V_{GS}=0\text{V}$	30			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=30\text{V}, V_{GS}=0\text{V}$ $T_J=55^\circ\text{C}$		1	5	μA
I_{GSS}	Gate-Body leakage current	$V_{DS}=0\text{V}, V_{GS}=\pm 20\text{V}$			± 100	nA
$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	1.2	1.7	2.2	V
$I_{D(\text{ON})}$	On state drain current	$V_{GS}=10\text{V}, V_{DS}=5\text{V}$	100			A
$R_{DS(\text{ON})}$	Static Drain-Source On-Resistance	$V_{GS}=10\text{V}, I_D=20\text{A}$ $T_J=125^\circ\text{C}$		7.4	9	$\text{m}\Omega$
		$V_{GS}=4.5\text{V}, I_D=20\text{A}$		11	13	$\text{m}\Omega$
g_{FS}	Forward Transconductance	$V_{DS}=5\text{V}, I_D=20\text{A}$		43		S
V_{SD}	Diode Forward Voltage	$I_S=1\text{A}, V_{GS}=0\text{V}$		0.7	1	V
I_S	Maximum Body-Diode Continuous Current			50		A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	$V_{GS}=0\text{V}, V_{DS}=15\text{V}, f=1\text{MHz}$	600	750	980	pF
C_{oss}	Output Capacitance		200	245	365	pF
C_{rss}	Reverse Transfer Capacitance		40	70	100	pF
R_g	Gate resistance	$V_{GS}=0\text{V}, V_{DS}=0\text{V}, f=1\text{MHz}$	0.4	0.8	1.4	Ω
SWITCHING PARAMETERS						
$Q_g(10\text{V})$	Total Gate Charge	$V_{GS}=10\text{V}, V_{DS}=15\text{V}, I_D=20\text{A}$	9	11.5	14	nC
$Q_g(4.5\text{V})$	Total Gate Charge		4	5	6	nC
Q_{gs}	Gate Source Charge		1.6	2	2.4	nC
Q_{gd}	Gate Drain Charge		1.5	2.5	3.5	nC
$t_{D(\text{on})}$	Turn-On Delay Time	$V_{GS}=10\text{V}, V_{DS}=15\text{V}, R_L=0.75\Omega, R_{\text{GEN}}=3\Omega$		5		ns
t_r	Turn-On Rise Time			3		ns
$t_{D(\text{off})}$	Turn-Off Delay Time			18		ns
t_f	Turn-Off Fall Time			3		ns
t_{rr}	Body Diode Reverse Recovery Time	$I_F=20\text{A}, dI/dt=500\text{A}/\mu\text{s}$	9	11	13	ns
Q_{rr}	Body Diode Reverse Recovery Charge	$I_F=20\text{A}, dI/dt=500\text{A}/\mu\text{s}$	18	23	28	nC

A. The value of R_{JJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The Power dissipation P_{DSM} is based on R_{JJA} and the maximum allowed junction temperature of 150°C . The value in any given application depends on the user's specific board design, and the maximum temperature of 175°C may be used if the PCB allows it.

B. The power dissipation P_D is based on $T_{J(\text{MAX})}=175^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature $T_{J(\text{MAX})}=175^\circ\text{C}$. Ratings are based on low frequency and duty cycles to keep initial $T_J=25^\circ\text{C}$.

D. The R_{JJA} is the sum of the thermal impedance from junction to case R_{JC} and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(\text{MAX})}=175^\circ\text{C}$. The SOA curve provides a single pulse rating.

G. The maximum current rating is limited by bond-wires.

H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

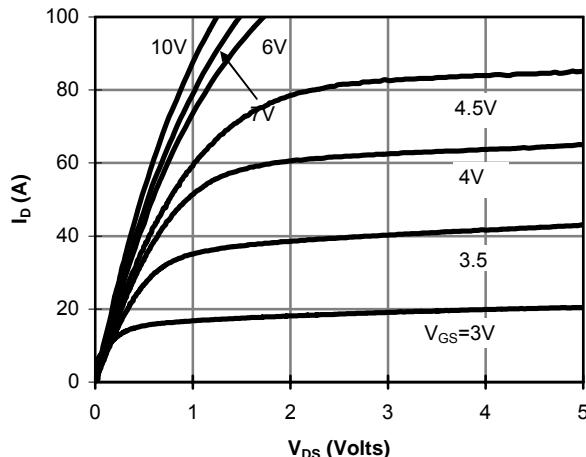


Fig 1: On-Region Characteristics (Note E)

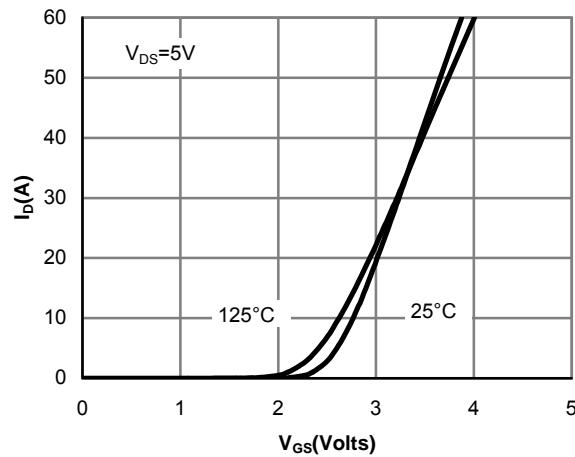


Figure 2: Transfer Characteristics (Note E)

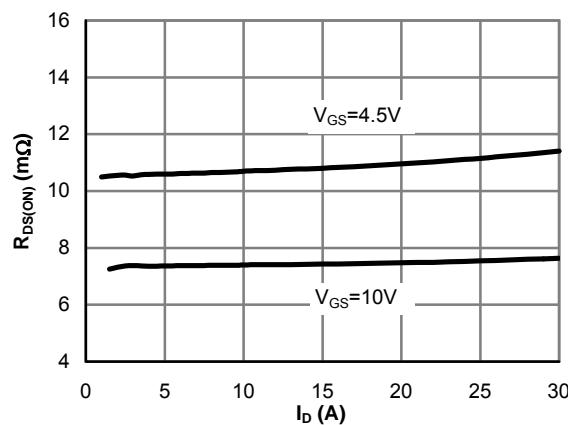


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

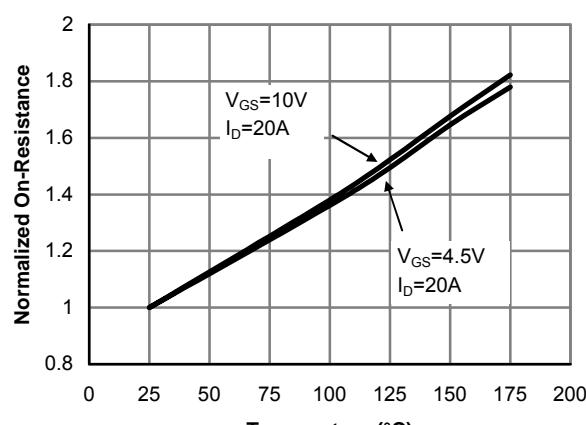


Figure 4: On-Resistance vs. Junction Temperature (Note E)

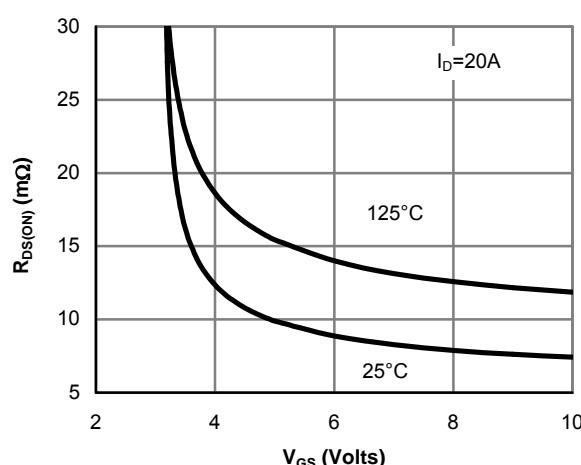


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

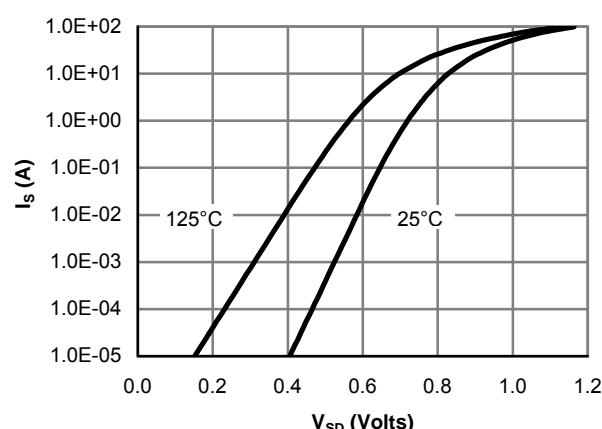


Figure 6: Body-Diode Characteristics (Note E)

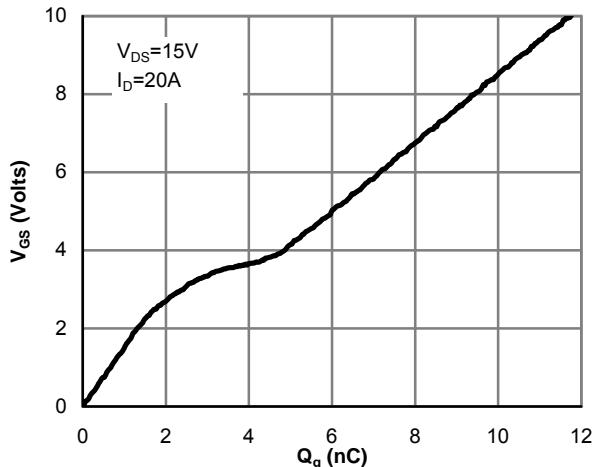
TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS


Figure 7: Gate-Charge Characteristics

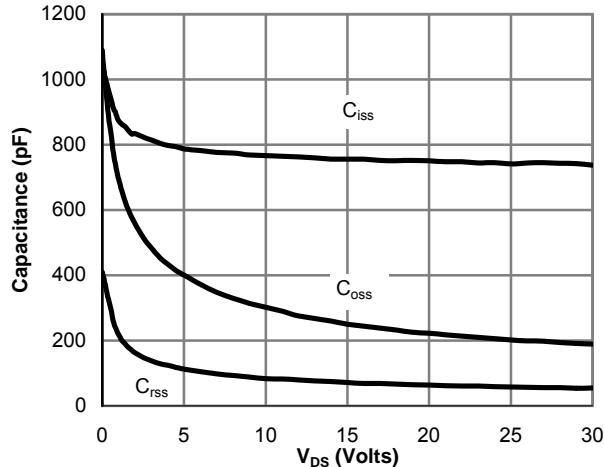


Figure 8: Capacitance Characteristics

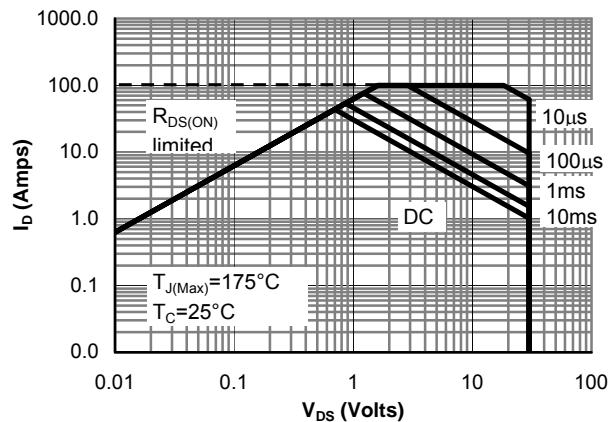


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

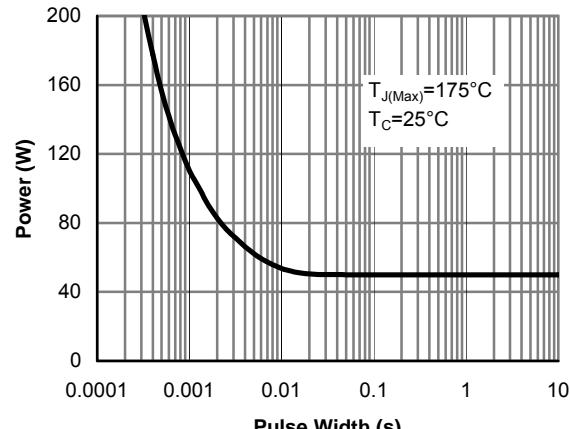


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

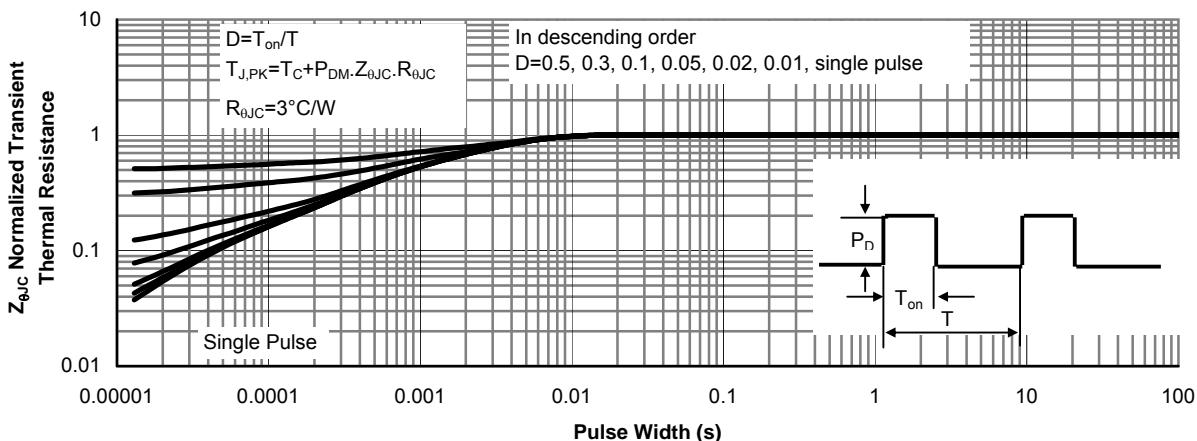
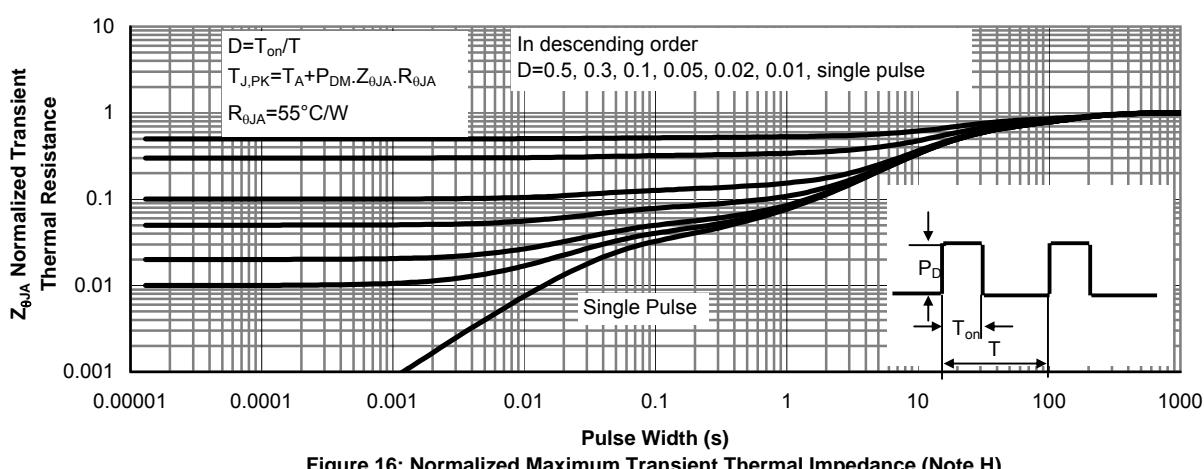
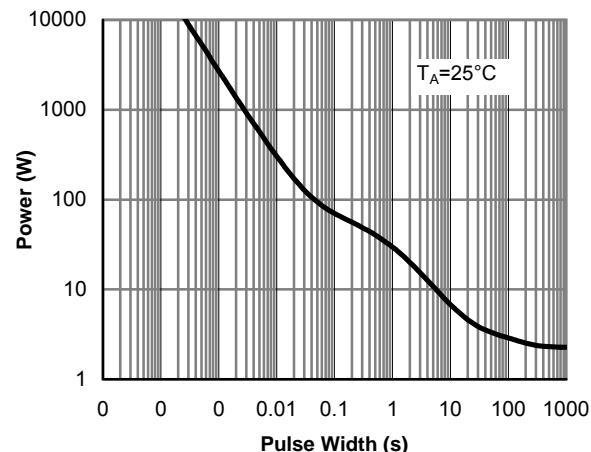
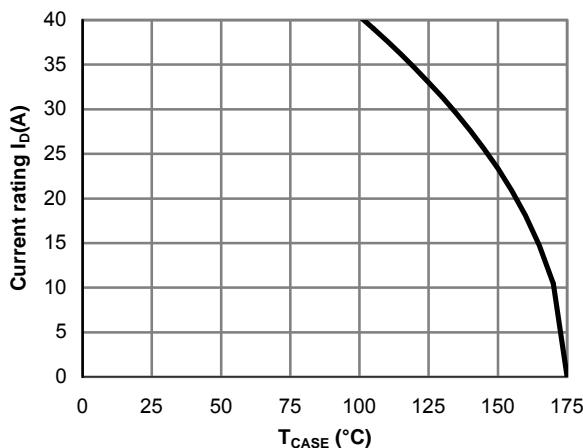
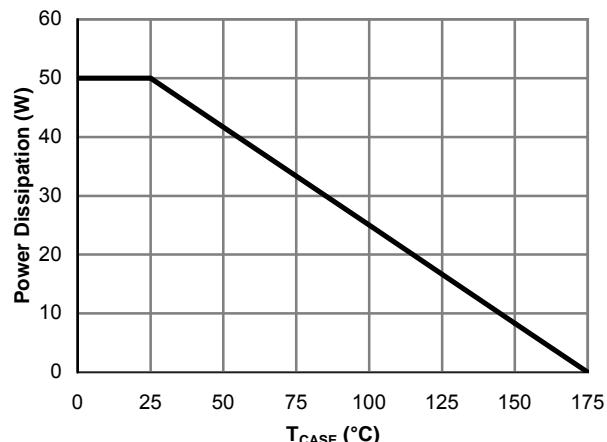
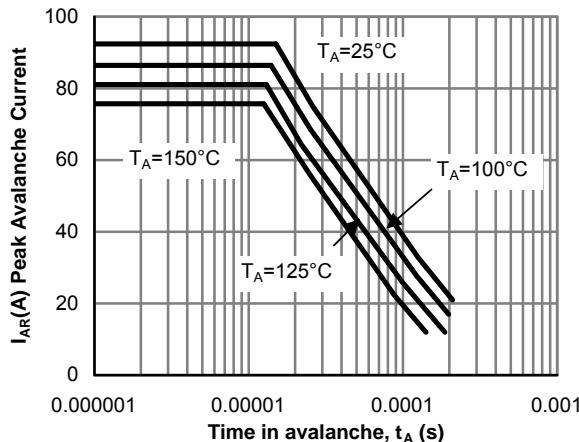
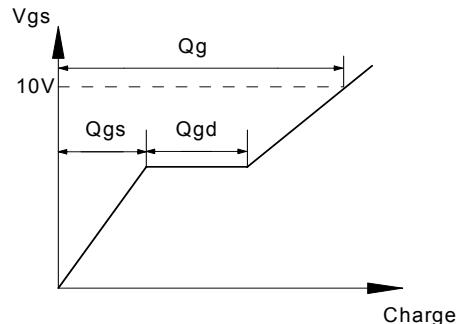
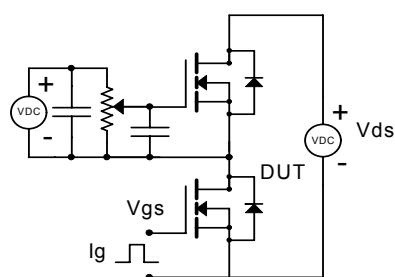


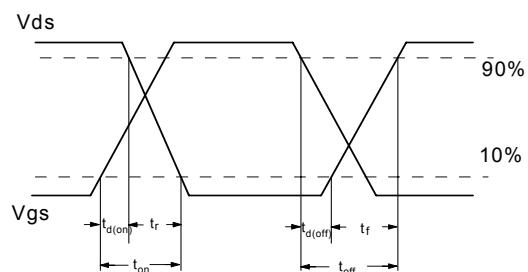
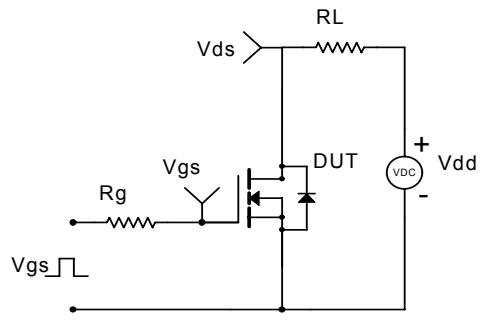
Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

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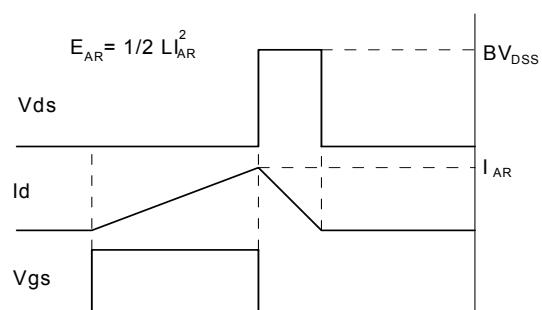
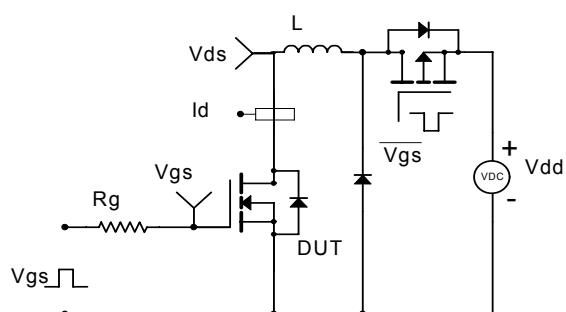
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

