



ALPHA & OMEGA
SEMICONDUCTOR



AON6405L

P-Channel Enhancement Mode Field Effect Transistor

General Description

The AON6405L combines advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$. This device is ideal for load switch and battery protection applications.

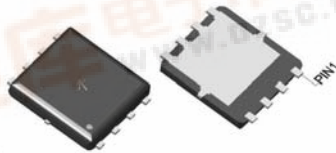
- RoHS Compliant
- Halogen Free

Features

V_{DS} (V) = -30V
 I_D = -30A (V_{GS} = -10V)
 $R_{DS(ON)}$ < 7m Ω (V_{GS} = -10V)
 $R_{DS(ON)}$ < 8m Ω (V_{GS} = -4.5V)

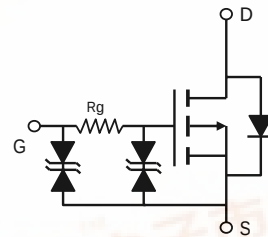
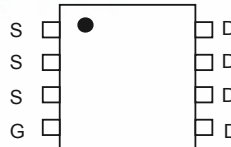
ESD Protected!
100% UIS Tested!

Fits SOIC8 footprint !



DFN5X6

Top View



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ^G	I_D	-30	A
$T_C=25^\circ\text{C}$		-23	
$T_C=100^\circ\text{C}$			
Pulsed Drain Current ^C	I_{DM}	-160	
Continuous Drain Current	I_{DSM}	-15	A
$T_A=25^\circ\text{C}$		-12	
$T_A=70^\circ\text{C}$			
Avalanche Current ^C	I_{AR}	-54	A
Repetitive avalanche energy $L=0.1\text{mH}$ ^C	E_{AR}	146	mJ
Power Dissipation ^B	P_D	83	W
$T_C=25^\circ\text{C}$		33	
$T_C=100^\circ\text{C}$			
Power Dissipation ^A	P_{DSM}	2.5	W
$T_A=25^\circ\text{C}$		1.6	
$T_A=70^\circ\text{C}$			
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	14.2	17	$^\circ\text{C/W}$
$t \leq 10\text{s}$				
Maximum Junction-to-Ambient ^{AD}	$R_{\theta JA}$	42	50	$^\circ\text{C/W}$
Steady-State				
Maximum Junction-to-Case	$R_{\theta JC}$	1.2	1.5	$^\circ\text{C/W}$
Steady-State				

Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D=-250\mu\text{A}$, $V_{GS}=0\text{V}$	-30			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=-30\text{V}$, $V_{GS}=0\text{V}$ $T_J=55^\circ\text{C}$			-1 -5	μA
I_{GSS}	Gate-Body leakage current	$V_{DS}=0\text{V}$, $V_{GS}=\pm 16\text{V}$			± 10	μA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$, $I_D=-250\mu\text{A}$	-0.8	-1.2	-1.6	V
$I_{D(ON)}$	On state drain current	$V_{GS}=-10\text{V}$, $V_{DS}=-5\text{V}$	-160			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=-10\text{V}$, $I_D=-20\text{A}$		5.5	7	$\text{m}\Omega$
		$T_J=125^\circ\text{C}$		7	8.5	
		$V_{GS}=-4.5\text{V}$, $I_D=-20\text{A}$		6.1	8	$\text{m}\Omega$
g_{FS}	Forward Transconductance	$V_{DS}=-5\text{V}$, $I_D=-20\text{A}$		70		S
V_{SD}	Diode Forward Voltage	$I_S=-1\text{A}$, $V_{GS}=0\text{V}$		-0.65	-1	V
I_S	Maximum Body-Diode Continuous Current				-50	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	$V_{GS}=0\text{V}$, $V_{DS}=-15\text{V}$, $f=1\text{MHz}$		4580	5500	pF
C_{oss}	Output Capacitance			755		pF
C_{rss}	Reverse Transfer Capacitance			564		pF
R_g	Gate resistance	$V_{GS}=0\text{V}$, $V_{DS}=0\text{V}$, $f=1\text{MHz}$		160	210	Ω
SWITCHING PARAMETERS						
$Q_g(-10\text{V})$	Total Gate Charge	$V_{GS}=-10\text{V}$, $V_{DS}=-15\text{V}$, $I_D=-20\text{A}$		87	105	nC
$Q_g(-4.5\text{V})$	Total Gate Charge			41		nC
Q_{gs}	Gate Source Charge			12.8		nC
Q_{gd}	Gate Drain Charge			17		nC
$t_{D(on)}$	Turn-On DelayTime	$V_{GS}=-10\text{V}$, $V_{DS}=-15\text{V}$, $R_L=0.75\Omega$, $R_{GEN}=3\Omega$		180		ns
t_r	Turn-On Rise Time			260		ns
$t_{D(off)}$	Turn-Off DelayTime			1.2		μs
t_f	Turn-Off Fall Time			9.7		μs
t_{rr}	Body Diode Reverse Recovery Time	$I_F=-20\text{A}$, $dI/dt=300\text{A}/\mu\text{s}$		32	40	ns
Q_{rr}	Body Diode Reverse Recovery Charge	$I_F=-20\text{A}$, $dI/dt=300\text{A}/\mu\text{s}$		77		nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ and the maximum allowed junction temperature of 150°C . The value in any given application depends on the user's specific board design.

B: The power dissipation P_D is based on $T_{J(MAX)}=150^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C: Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}=150^\circ\text{C}$. Ratings are based on low frequency and duty cycles to keep initial $T_J=25^\circ\text{C}$.

D: The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.

E: The static characteristics in Figures 1 to 6 are obtained using $<300\mu\text{s}$ pulses, duty cycle 0.5% max.

F: These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}=150^\circ\text{C}$. The SOA curve provides a single pulse rating.

G: The maximum current rating is limited by bond-wires.

H: These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

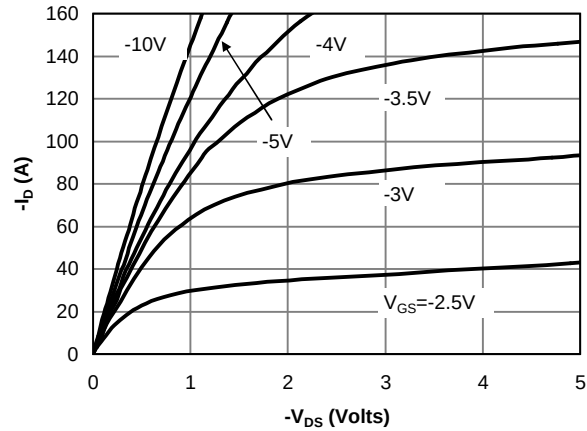


Figure 1: On-Region Characteristics(Note E)

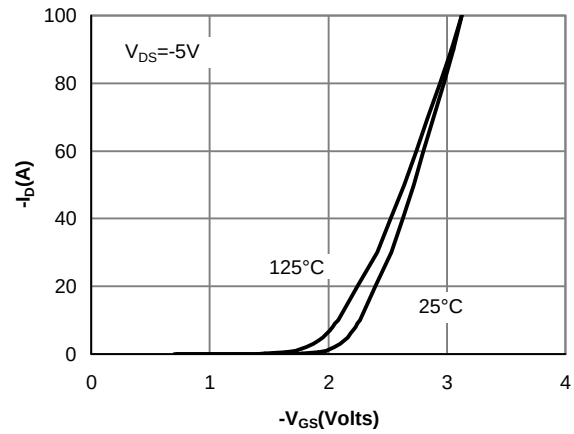


Figure 2: Transfer Characteristics(Note E)

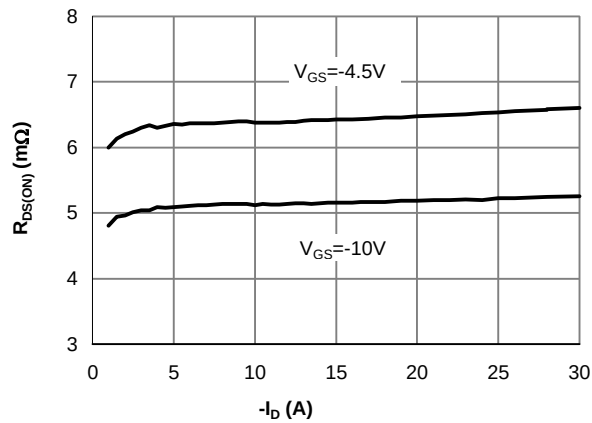


Figure 3: On-Resistance vs. Drain Current and Gate Voltage(Note E)

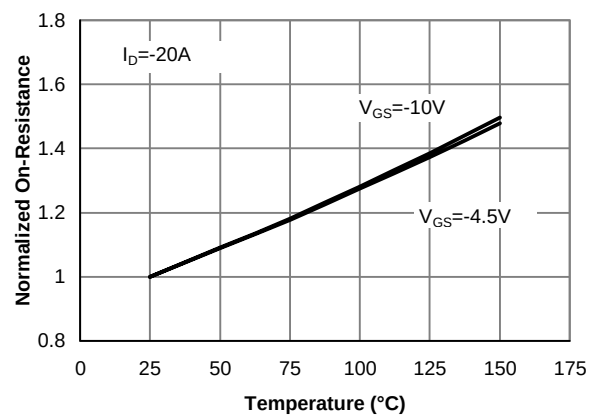


Figure 4: On-Resistance vs. Junction Temperature (Note E)

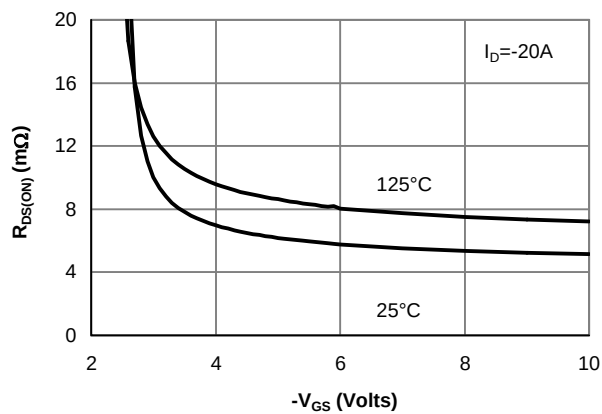


Figure 5: On-Resistance vs. Gate-Source Voltage(Note E)

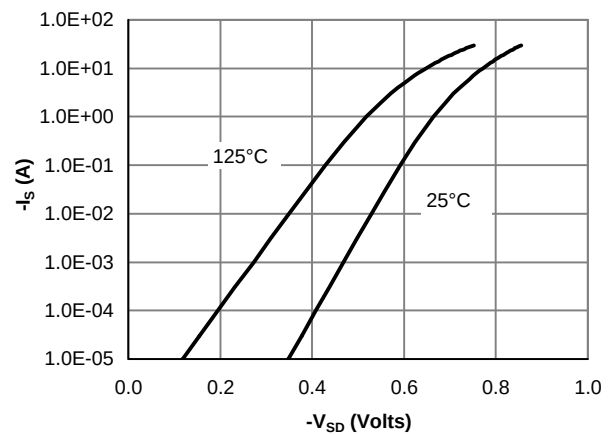
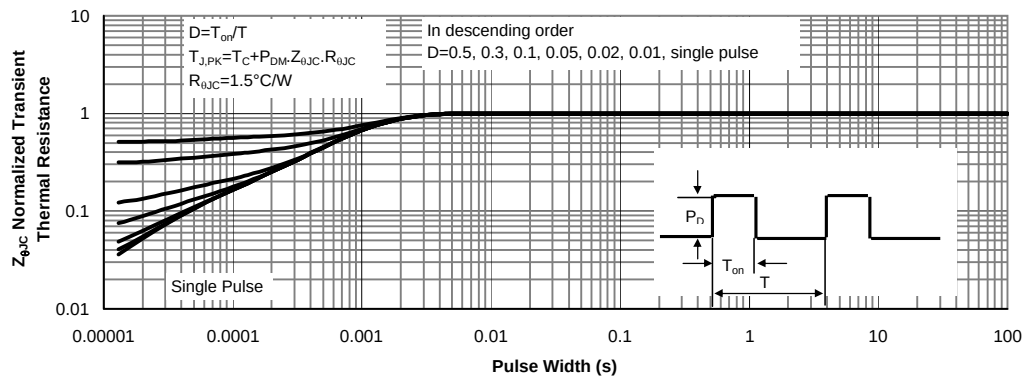
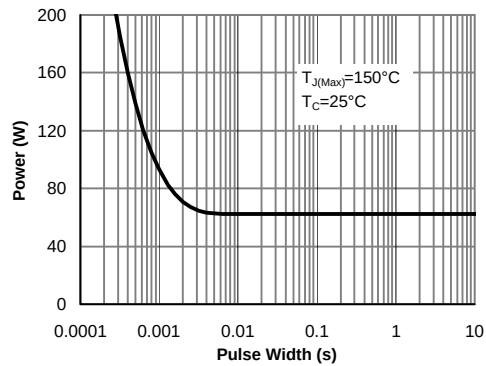
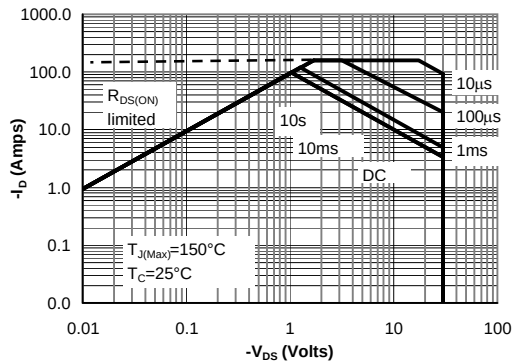
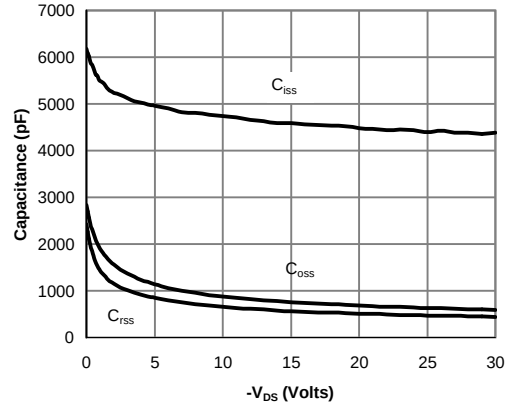
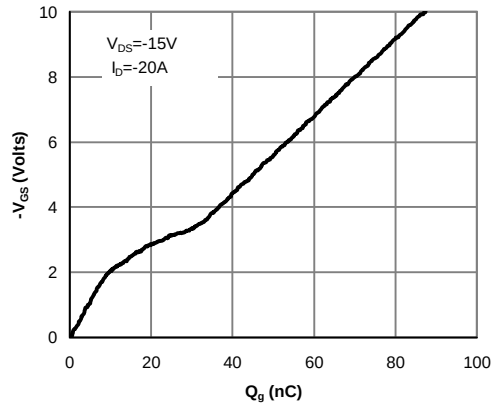
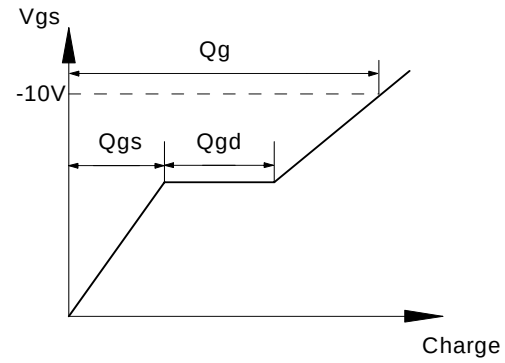
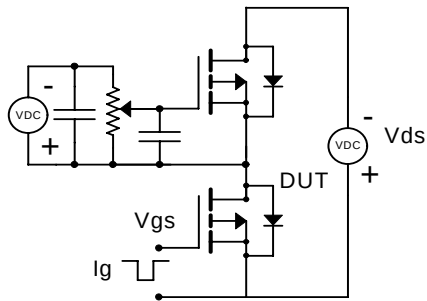


Figure 6: Body-Diode Characteristics(Note E)

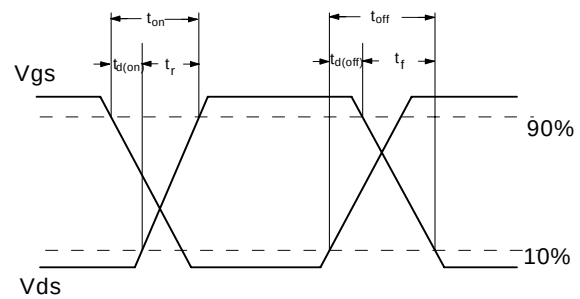
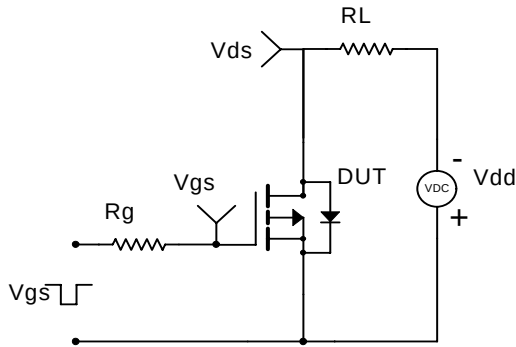
TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS



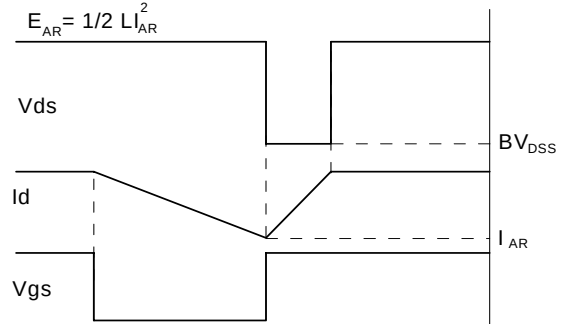
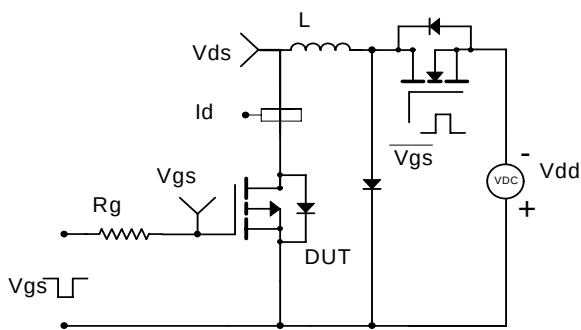
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

