LTC1755/LTC1756

Smart Card Interface

FEATURES

- **Fully ISO 7816-3 and EMV Compliant (Including Auxiliary I/O Pins)**
- **Buck-Boost Charge Pump Generates 3V or 5V**
- **2.7V to 6.0V Input Voltage Range (LTC1755)**
- **Very Low Operating Current: 60μA**
- **>10kV ESD on All Smart Card Pins**
- Dynamic Pull-Ups Deliver Fast Signal Rise Times
- Soft-Start Limits Inrush Current at Turn On
- 3V ↔ 5V Signal Level Translators
- Shutdown Current: <1μA
- Short-Circuit and Overtemperature Protected
- Alarm Output Indicates Fault Condition
- Multiple Devices May Be Paralleled for Multicard Applications (LTC1755)
- Available in 16- and 24-Pin SSOP Packages

APPLICATIONS

- Handheld Payment Terminals
- Pay Telephones
- ATMs
- Key Chain Readers
- Smart Card Readers

DESCRIPTION

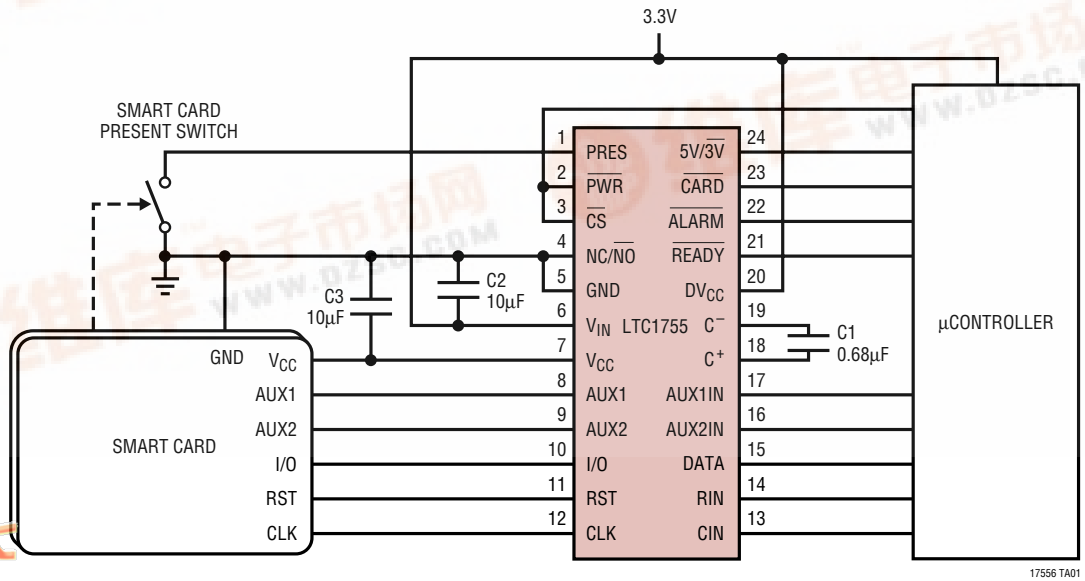
The LTC®1755/LTC1756 universal Smart Card interfaces are fully compliant with ISO 7816-3 and EMV specifications. The parts provide the smallest and simplest interface circuits between a host microcontroller and general purpose Smart Cards.

An internal charge pump DC/DC converter delivers regulated 3V or 5V to the Smart Card, while on-chip level shifters allow connection to a low voltage controller. All Smart Card contacts are rated for 10kV ESD, eliminating the need for external ESD protection devices.

Input voltage may range from 2.7V to 6.0V, allowing direct connection to a battery. Internal soft-start mitigates start-up problems that may result when the input power is provided by another regulator. Multiple devices may be paralleled and connected to a single controller for multicard applications.

Battery life is maximized by 60μA operating current and 1μA shutdown current. The narrow SSOP packages minimize PCB area for compact portable systems.

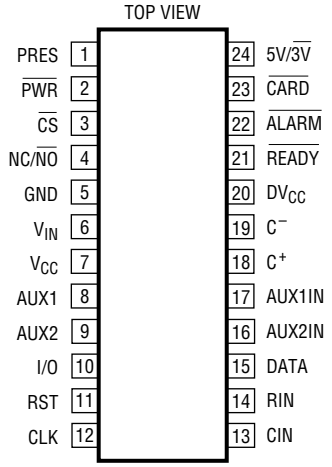
TYPICAL APPLICATION



ABSOLUTE MAXIMUM RATINGS (Note 1)

V_{IN} to GND (LTC1755) ..... –0.3V to 6.5V
V_{IN} to GND (LTC1756) ..... –0.3V to 6.0V
DV_{CC} to GND (LTC1755) ..... –0.3V to 5.5V
V_{CC} to GND ..... –0.3V to 5.5V
Digital Inputs to GND
(LTC1755) ..... –0.3V to DV_{CC} + 0.3V
Digital Inputs to GND
(LTC1756) ..... –0.3V to V_{IN} + 0.3V
CLK, RST, I/O, AUX1,
AUX2 to GND ..... –0.3V to V_{CC} + 0.3V
V_{CC} Short-Circuit Duration ..... Indefinite
Operating Temperature Range (Note 2) .. –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

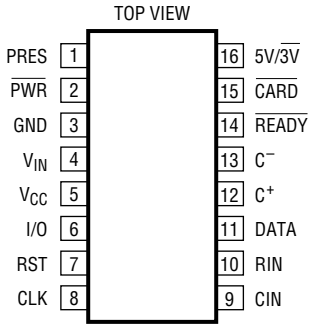
PACKAGE/ORDER INFORMATION



GN PACKAGE
24-LEAD NARROW PLASTIC SSOP
T_{JMAX} = 125°C, θ_{JA} = 150°C/W

ORDER PART NUMBER

LTC1755EGN



GN PACKAGE
16-LEAD NARROW PLASTIC SSOP
T_{JMAX} = 125°C, θ_{JA} = 135°C/W

ORDER PART NUMBER

LTC1756EGN

PART MARKING

1756

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full specified temperature range, otherwise specificatons are at T_A = 25°C.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
LTC1755 (V_{IN} = 2.7V to 6V, DV_{CC} = 2V to 5.5V, unless otherwise noted)						
V_{IN} Operating Voltage		●	2.7		6	V
DV_{CC} Operating Voltage		●	2.0		5.5	V
I_{VIN} Operating Current	ACTIVE State, I_{VCC} = 0	●		50	100	µA
I_{DVCC} Operating Current	ACTIVE State, DV_{CC} = 3V	●		10	20	µA
I_{VIN} Shutdown Current	IDLE State, DV_{CC} = 0V, $V_{IN} \leq 3.6V$	●			1	µA
	IDLE State, DV_{CC} = 0V, $3.6V < V_{IN} \leq 6V$	●			10	µA
	IDLE State, DV_{CC} = 5.5V, $V_{IN} \leq 6V$	●			20	µA
V_{CC} Output Voltage	5V/$\overline{3V}$ = DV_{CC}	●	4.75	5.00	5.25	V
	5V/$\overline{3V}$ = 0V	●	2.80	3.00	3.20	V
I_{VCC} Output Current	5V/$\overline{3V}$ = 0V, $3V \leq V_{IN} \leq 6.0V$	●	55			mA
	5V/$\overline{3V}$ = DV_{CC}, $3V \leq V_{IN} \leq 6.0V$	●	65			mA
	5V/$\overline{3V}$ = 0V, $2.7V \leq V_{IN} \leq 6.0V$	●	55			mA
	5V/$\overline{3V}$ = DV_{CC}, $2.7V \leq V_{IN} \leq 6.0V$	●	40			mA
V_{CC} Turn-On Time	C_{OUT} = 10µF, ↓ $\overline{PWR}$ to ↓ $\overline{READY}$, 50% to 50%	●		2.7	12	ms
V_{CC} Discharge Time to 0.4V	I_{VCC} = 0mA, V_{CC} = 5V, C_{OUT} = 10µF	●		100	250	µs
LTC1756 (V_{IN} = 2.7V to 5.5V, unless otherwise noted)						
V_{IN} Operating Voltage		●	2.7		5.5	V
I_{VIN} Operating Current	ACTIVE State, I_{VCC} = 0	●		75	150	µA
I_{VIN} Shutdown Current	IDLE State, $V_{IN} \leq 3.6V$	●			2.5	µA
	IDLE State, $3.6V < V_{IN} \leq 5.5V$	●			10	µA
V_{CC} Output Voltage	5V/$\overline{3V}$ = V_{IN}	●	4.75	5.00	5.25	V
	5V/$\overline{3V}$ = 0V	●	2.80	3.00	3.20	V
I_{VCC} Output Current	5V/$\overline{3V}$ = 0V, $3V \leq V_{IN} \leq 5.5V$	●	55			mA
	5V/$\overline{3V}$ = V_{IN}, $3V \leq V_{IN} \leq 5.5V$	●	65			mA
	5V/$\overline{3V}$ = 0V, $2.7V \leq V_{IN} \leq 5.5V$	●	55			mA
	5V/$\overline{3V}$ = V_{IN}, $2.7V \leq V_{IN} \leq 5.5V$	●	40			mA
V_{CC} Turn-On Time	C_{OUT} = 10µF, ↓ $\overline{PWR}$ to ↓ $\overline{READY}$, 50% to 50%	●		2.7	12	ms
V_{CC} Discharge Time to 0.4V	I_{VCC} = 0mA, V_{CC} = 5V, C_{OUT} = 10µF	●		100	250	µs

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full specified temperature range, otherwise specificatons are at T_A = 25°C. DV_{CC} = 2V to 5.5V, unless otherwise noted (Note 4).

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Controller Inputs/Outputs DATA, AUX1IN, AUX2IN, DV_{CC} = 3V						
High Input Voltage Threshold (V_{IH})	(Note 4)	●	DV_{CC} – 0.6	0.5 • DV_{CC}		V
Low Input Voltage Threshold (V_{IL})	(Note 4)	●		0.5 • DV_{CC}	0.3	V
High Level Output Voltage (V_{OH})	Source Current = 20µA (Note 4)	●	0.7 • DV_{CC}			V
Low Level Output Voltage (V_{OL})	Sink Current = –500µA (Note 3)	●			0.3	V
Output Rise/Fall Time	Loaded with 30pF, 10% to 90%	●			0.5	µs
Input Current (I_{IH}/I_{IL})	$\overline{CS}$ = DV_{CC}	●	–1		1	µA
RIN, CIN, $\overline{PWR}$, $\overline{CS}$, 5V/$\overline{3V}$, NC/$\overline{NO}$						
High Input Voltage Threshold (V_{IH})	(Note 4)	●	0.7 • DV_{CC}	0.5 • DV_{CC}		V
Low Input Voltage Threshold (V_{IL})	(Note 4)	●		0.5 • DV_{CC}	0.2 • DV_{CC}	V
Input Current (I_{IH}/I_{IL})		●	–1		1	µA
$\overline{READY}$, $\overline{ALARM}$, $\overline{CARD}$						
Pull-Up Current (I_{OH})		●	250			nA
Low Level Output Voltage (V_{OL})	Sink Current = –20µA	●			0.3	V
Smart Card Inputs/Outputs I/O, AUX1, AUX2, V_{CC} = 3V or 5V						
High Input Voltage Threshold (V_{IH})	$I_{IH(MAX)}$ = ±20µA	●	0.6 • V_{CC}	0.5 • V_{CC}		V
Low Input Voltage Threshold (V_{IL})	$I_{IL(MAX)}$ = 1mA	●		0.5 • V_{CC}	0.8	V
High Level Output Voltage (V_{OH})	Source Current = 20µA DATA, AUX1IN, AUX2IN = DV_{CC}	●	0.8 • V_{CC}			V
Low Level Output Voltage (V_{OL})	Sink Current = –1mA DATA, AUX1IN, AUX2IN = 0V (Note 3)	●			0.3	V
Rise/ Fall Time	Loaded with 30pF, 10% to 90%	●			0.5	µs
Short-Circuit Current	Shorted to V_{CC}	●		3.5	7.5	mA
CLK						
High Level Output Voltage (V_{OH})	Source Current = 100µA	●	V_{CC} – 0.5			V
Low Level Output Voltage (V_{OL})	Sink Current = –200µA	●			0.3	V
CLK Rise/Fall Time	CLK Loaded with 30pF	●			16	ns
CLK Frequency	CLK Loaded with 30pF	●	5			MHz
RST						
High Level Output Voltage (V_{OH})	Source Current = 200µA Source Current = 50µA	● ●	0.8 • V_{CC} V_{CC} – 0.5V			V V
Low Level Output Voltage (V_{OL})	Sink Current = –200µA	●			0.3	V
RST Rise/Fall Time	Loaded with 30pF, 10% to 90%	●			0.5	µs
PRES						
High Input Voltage Threshold (V_{IH})	(Note 4)	●	0.7 • DV_{CC}	0.5 • DV_{CC}		V
Low Input Voltage Threshold (V_{IL})	(Note 4)	●		0.5 • DV_{CC}	0.2 • DV_{CC}	V
PRES Pull-Up Current	V_{PRES} = 0V	●	0.5	1		µA
PRES Debounce Time	Proportional to the 0.68µF Charge Pump Capacitor	●	40	80		ms

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

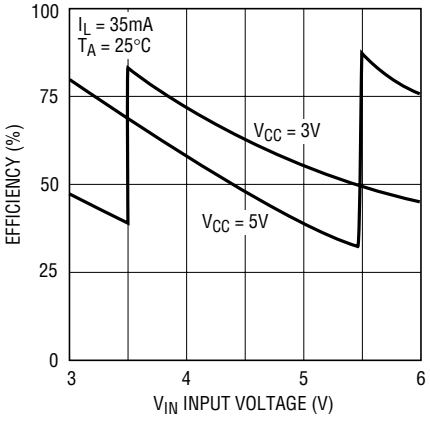
Note 2: The LTC1755/LTC1756 are guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

Note 3: The DATA, AUX1IN, AUX2IN, AUX1, AUX2 and I/O pull-down drivers must sink up to 250µA sourced by the internal current sources.

Note 4: On the LTC1756, DV_{CC} is internally connected to the V_{IN} pin. Specifications that call out DV_{CC} should be referred to V_{IN} instead.

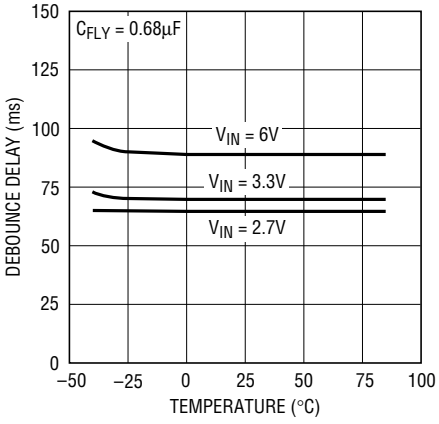
TYPICAL PERFORMANCE CHARACTERISTICS

Power Efficiency vs Input Voltage



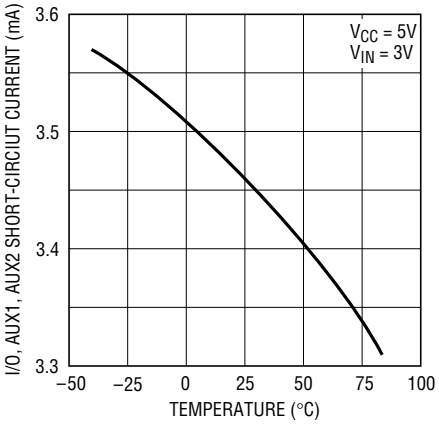
17556 G01

Card Detection Debounce Period vs Temperature



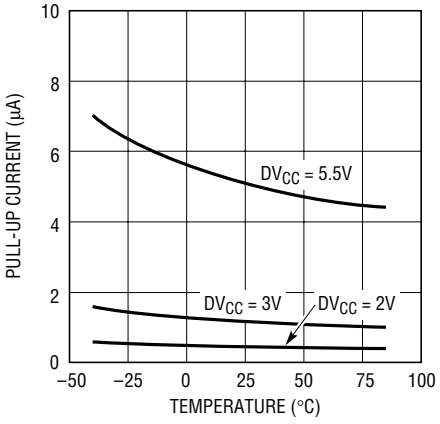
17556 G02

I/O, AUX1, AUX2 Short-Circuit Current vs Temperature



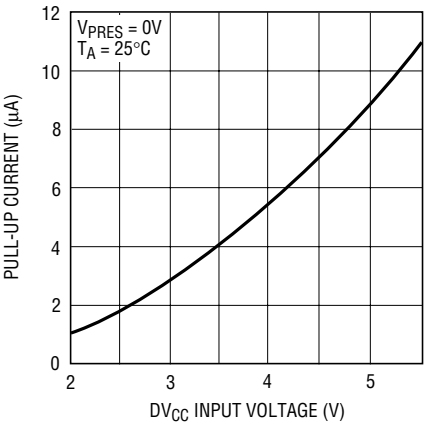
17556 G03

$\overline{CARD}$, $\overline{READY}$, $\overline{ALARM}$ Pull-Up Current vs Temperature



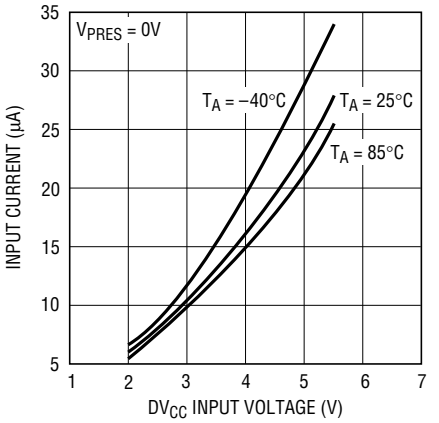
17556 G04

PRES Pin Pull-Up Current vs DV_{CC}



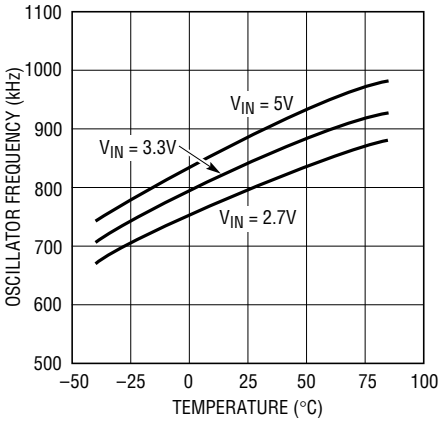
17556 G05

DV_{CC} Input Current vs DV_{CC} Voltage



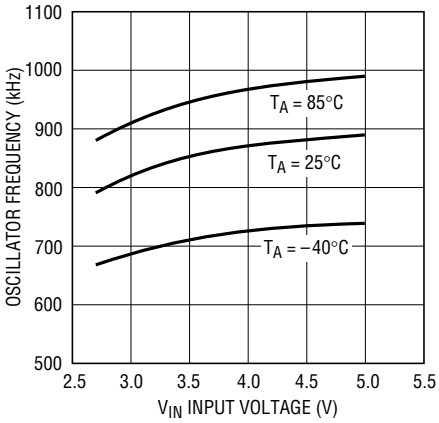
17556 G02

Oscillator Frequency vs Temperature



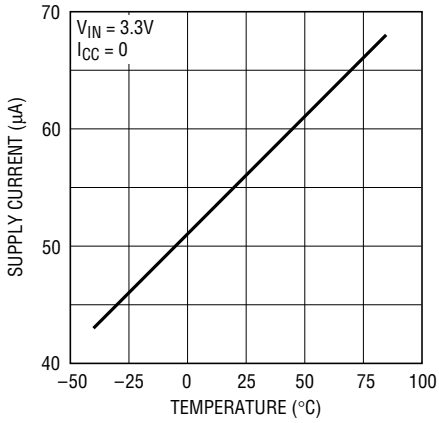
17556 G07

Oscillator Frequency vs Input Voltage



17556 G07

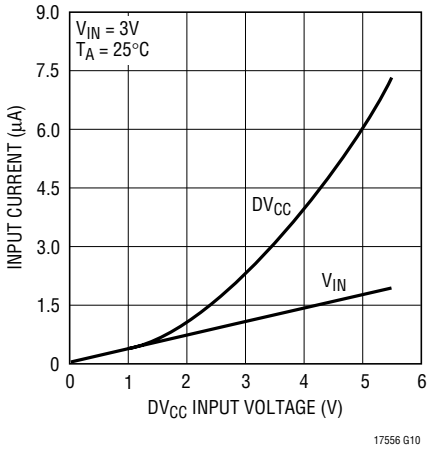
V_{IN} Supply Current vs Temperature



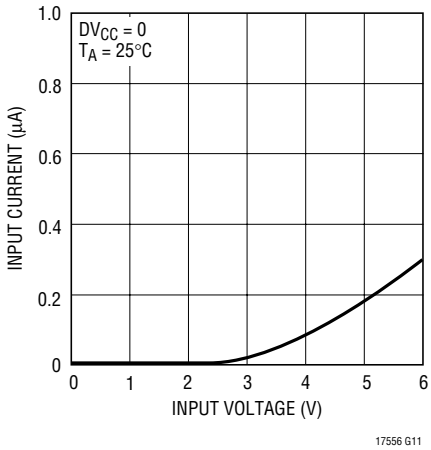
17556 G09

TYPICAL PERFORMANCE CHARACTERISTICS

DV_{CC}, V_{IN} Supply Current In Shutdown



V_{IN} Shutdown Current vs Input Voltage



PIN FUNCTIONS LTC1755/LTC1756

PRES (Pin 1): (Input) Connects to the Smart Card acceptor's PRESENT indicator switch to detect if a card is inserted. This pin has a pull-up current source so that a grounded switch can be detected with no external components. The pull-up current source is nonlinear, delivering higher current when the PRES pin is above 1V but very little current below 1V. This helps resist false card indications due to leakage current. The activation state of the PRES pin can be set by the NC/$\overline{NO}$ pin so that both normally open (NO) and normally closed (NC) switches are easily recognized (see NC/$\overline{NO}$ pin description).

DV_{CC} sets the logic reference level for the PRES pin.

$\overline{PWR}$ (Pin 2): (Input) A low on the $\overline{PWR}$ pin places the LTC1755/LTC1756 in the ACTIVE state enabling the charge pump. The $\overline{READY}$ pin indicates when the card supply voltage (V_{CC}) has reached its final value and communication with the Smart Card is possible. The reset and clock channels are enabled after $\overline{READY}$ goes low. The three I/O channels are also enabled only after $\overline{READY}$ goes low, however they may be disabled separately via the $\overline{CS}$ pin ($\overline{CS}$ is not available on the LTC1756).

The falling edge of $\overline{PWR}$ latches the state of the 5V/$\overline{3V}$ pin. After $\overline{PWR}$ is low, changes on the 5V/$\overline{3V}$ pin are ignored.

$\overline{CS}$ (Pin 3, LTC1755 Only): (Input) The $\overline{CS}$ pin enables the three bidirectional I/O channels of the LTC1755. When the I/O channels are disabled the Smart Card pins (I/O, AUX1, AUX2) are forced to logic one and the controller pins (DATA, AUX2IN, AUX1IN) are high impedance. $\overline{CS}$ can be brought low along with $\overline{PWR}$ when the device is first enabled, however communication with the Smart Card is inhibited until V_{CC} reaches its final value as indicated by a low on the $\overline{READY}$ pin. $\overline{CS}$ does not affect the charge pump, CLK or RST channels. On the LTC1756, $\overline{CS}$ is internally connected to the $\overline{PWR}$ pin.

DV_{CC} sets the logic reference level for the $\overline{CS}$ pin.

NC/$\overline{NO}$ (Pin 4, LTC1755 Only): (Input) This pin controls the activation level of the PRES pin. When it is high (DV_{CC}) the PRES pin is active high. When it is low (GND) the PRES pin is active low. In either case the presence of a Smart Card is indicated by a low on the $\overline{CARD}$ output. When a ground side normally open (NO) switch is used the NC/$\overline{NO}$ pin should be grounded. When a ground side normally closed (NC) switch is used the NC/$\overline{NO}$ pin should be connected to DV_{CC}. The LTC1756 is permanently configured to accept a normally open switch.

PIN FUNCTIONS LTC1755/LTC1756

Note: If a normally closed switch is used, a small current (several microamperes) will flow through the switch whenever a Smart Card is not present. For ultralow power consumption in shutdown, a normally open switch is optimum.

DV_{CC} sets the logic reference level for the NC/$\overline{NO}$ pin.

GND (Pins 5/3): Ground Reference for the IC. This pin should be connected to a low impedance ground plane. Bypass capacitors for V_{IN} and V_{CC} should be in close proximity to the GND pin.

V_{IN} (Pins 6/4): Supply Voltage for the Charge Pump. May be between 2.7V and 6V. A 10µF low ESR ceramic bypass capacitor is required on this pin for optimum performance.

V_{CC} (Pins 7/5): Regulated Smart Card Supply Voltage. This pin should be connected to the Smart Card V_{CC} contact. The 5V/$\overline{3V}$ pin determines the V_{CC} output voltage.

The V_{CC} pin is protected against short circuits by comparing the actual output voltage with an internal reference voltage. If V_{CC} is below its correct level (for as little as 5µs) the LTC1755/LTC1756 switch to the Alarm state (see the State Diagram). The V_{CC} pin requires a 10µF charge storage capacitor to ground. For optimum performance a low ESR ceramic capacitor should be used.

During the Idle and Alarm states the V_{CC} pin is rapidly discharged to ground to comply with the deactivation requirements of the EMV and ISO-7816 specifications.

AUX1 (Pin 8, LTC1755 Only): (Input/Output) Smart Card Side Auxiliary I/O Pin. This pin is used for auxiliary bidirectional data transfer between the microcontroller and the Smart Card. It has the same characteristics as the I/O pin.

AUX2 (Pin 9, LTC1755 Only): (Input/Output) Smart Card Side Auxiliary I/O Pin. This pin is used for auxiliary bidirectional data transfer between the microcontroller and the Smart Card. It has the same characteristics as the I/O pin.

I/O (Pins 10/6): (Input/Output) Smart Card Side Data I/O Pin. This pin is used for bidirectional data transfer between the microcontroller and the Smart Card. It should be connected to the Smart Card I/O contact. The Smart Card I/O pin must be able to sink up to 250µA when driving the I/O pin low due to the pull-up current source. The I/O pin becomes a low impedance to ground during the Idle state. It does not become active until $\overline{READY}$ goes low indicating that V_{CC} is stable.

Once $\overline{READY}$ is low the I/O pin is protected against short circuits to V_{CC} by current limiting to 5mA maximum.

The DATA-I/O channel is bidirectional for half-duplex transmissions. Its idle state is H-H. Once an L is detected on one side of the channel the direction of transmission is established. Specifically, the side which received an L first is now the input, and the opposite side is the output. Transmission from the output side back to the input side is inhibited, thereby preventing a latch condition. Once the input side releases its L, both sides return to H, and the channel is now ready for a new L to be transmitted in either direction. If an L is forced externally on the output side, and it persists until after the L on the input side is released, this illegal input will not be transmitted to the input side because the transmission direction will not have changed. The direction of transmission can only be established from the idle (H-H) state and is determined by the first receipt of an L on either side.

RST (Pins 11/7): (Output) Level-Shifted Reset Output Pin. This pin should be connected to the Smart Card RST contact. The RST pin becomes a low impedance to ground during the Idle state (see the State Diagram). The reset channel does not become active until the $\overline{READY}$ signal goes low indicating that V_{CC} is stable.

Short-circuit protection is provided on the RST pin by comparing RST with R_{IN}. If these signals differ for several microseconds then the LTC1755/LTC1756 switch to the Alarm state. This fault checking is only performed after the V_{CC} pin has reached its final value (as indicated by the $\overline{READY}$ pin).

CLK (Pins 12/8): (Output) Level-Shifted Clock Output Pin. This pin should be connected to the Smart Card CLK contact. The CLK pin becomes a low impedance to ground during the Idle state (see the State Diagram). The clock channel does not become active until the $\overline{READY}$ signal goes low indicating that V_{CC} is stable.

Short-circuit protection is provided on the CLK pin by comparing CLK with C_{IN}. If these signals differ for several

PIN FUNCTIONS LTC1755/LTC1756

microseconds then the LTC1755/LTC1756 switch to the Alarm state. This fault checking is only performed after the V_{CC} pin has reached its final value (as indicated by the $\overline{READY}$ pin).

The clock channel is optimized for signal integrity in order to meet the stringent duty cycle requirements of the EMV specification. Therefore, to reduce power in low power applications, clock stop mode is recommended when data is not being exchanged.

CIN (Pins 13/9): (Input) Clock Input Pin from the Microcontroller. During the Active state this signal appears on the CLK pin after being level-shifted and buffered.

DV_{CC} sets the logic reference level for the C_{IN} pin.

RIN (Pins 14/10): (Input) Reset Input Pin from the Microcontroller. During the Active state this signal appears on the RST pin after being level-shifted and buffered.

DV_{CC} sets the logic reference level for the R_{IN} pin.

DATA (Pins 15/11): (Input/Output) Microcontroller Side Data I/O Pin. This pin is used for bidirectional data transfer between the microcontroller and the Smart Card. The microcontroller data pin must be open drain and must be able to sink up to 250μA when driving the DATA pin low due to the pull-up current source. The DATA pin becomes high impedance during the Idle state or when $\overline{CS}$ is high (see the State Diagram). It does not become active until the $\overline{READY}$ signal goes low indicating that V_{CC} is stable.

AUX2IN (Pin 16, LTC1755 Only): (Input/Output) Microcontroller Side Auxiliary I/O pin. This pin is used for bidirectional auxiliary data transfer between the microcontroller and the Smart Card. It has the same characteristics as the DATA pin.

AUX1IN (Pin 17, LTC1755 Only): (Input/Output) Microcontroller Side Auxiliary I/O Pin. This pin is used for bidirectional auxiliary data transfer between the microcontroller and the Smart Card. It has the same characteristics as the DATA pin.

C^+, C^- (Pins 18/12, 19/13): Charge Pump Flying Capacitor Terminals. Optimum values for the flying capacitor range from 0.68μF to 1μF. Best performance is achieved with a low ESR X7R ceramic capacitor.

DV_{CC} (Pin 20, LTC1755 Only): Supply Voltage for the Microcontroller Side Digital Input and Input/Output Pins (Typically 3V). If the charge pump input pin (V_{IN}) is powered from the same source as the microcontroller, then DV_{CC} should be connected directly to V_{IN}. In this case only one (10μF) input bypass capacitor is needed for the LTC1755. If the DV_{CC} pin is powered separately then it should be bypassed separately with a 0.1μF capacitor. The DV_{CC} pin may be between 2V and 5.5V.

The DV_{CC} pin is monitored for adequate voltage. If DV_{CC} drops below approximately 1.5V the LTC1755 automatically enters the Idle state. On the LTC1756, DV_{CC} is connected internally to V_{IN}.

$\overline{READY}$ (Pins 21/14): (Output) Readiness Indicator of the Smart Card Supply Voltage (V_{CC}). When the LTC1755/LTC1756 are placed in the Active state the soft-start feature slowly ramps the V_{CC} voltage. A low on the $\overline{READY}$ pin indicates that V_{CC} has reached its final value.

The $\overline{READY}$ pin also indicates if the LTC1756 is in Alarm mode. The LTC1756 detects faults such as V_{CC} underrange for at least 5μs, overtemperature shutdown, CLK or RST invalid output levels and card removal during Active state. CLK or RST invalid and overtemperature faults are detected only after V_{CC} has reached its final value. V_{CC} underrange and card removal during Active faults are detected at any time during the Active period (i.e., once $\overline{PWR}$ = 0V).

If the LTC1756 has been activated normally and V_{CC}, the card voltage, has reached its final value then $\overline{READY}$ will go low indicating normal operation. If, following this, a fault occurs and the LTC1756 enters the Alarm state, the $\overline{READY}$ pin will return high.

In the event that a fault precedes the activation of V_{CC}, such as a direct short circuit from V_{CC} to GND, the LTC1756 will attempt to operate until the fault is detected and then automatically shut down and enter the Alarm state. In this case the $\overline{READY}$ pin will never go low after the command to start the smart card is given (i.e., $\overline{PWR}$ = 0V).

If the LTC1755/LTC1756 enter the Alarm state they can only be cleared by returning the $\overline{PWR}$ pin high.

PIN FUNCTIONS LTC1755/LTC1756

The $\overline{\text{READY}}$ pin is configured as an open-drain pull-down with a weak pull-up current source. This permits wired-OR connections of multiple LTC1755/LTC1756s to a single microcontroller.

$\overline{\text{ALARM}}$ (Pin 22, LTC1755 Only): (Output) A low on this pin indicates that a fault has occurred and that the LTC1755 is in the Alarm state (see the State Diagram). Possible faults include V_{CC} underrange for at least 5µs, overtemperature shutdown, CLK or RST invalid output levels, and card removal during the Active state.

CLK or RST invalid and overtemperature faults are detected only after V_{CC} has reached its final value (as indicated by the $\overline{\text{READY}}$ pin). V_{CC} underrange and card removal during Active faults are detected at any time during the Active period (i.e., once $\overline{\text{PWR}}$ = 0V).

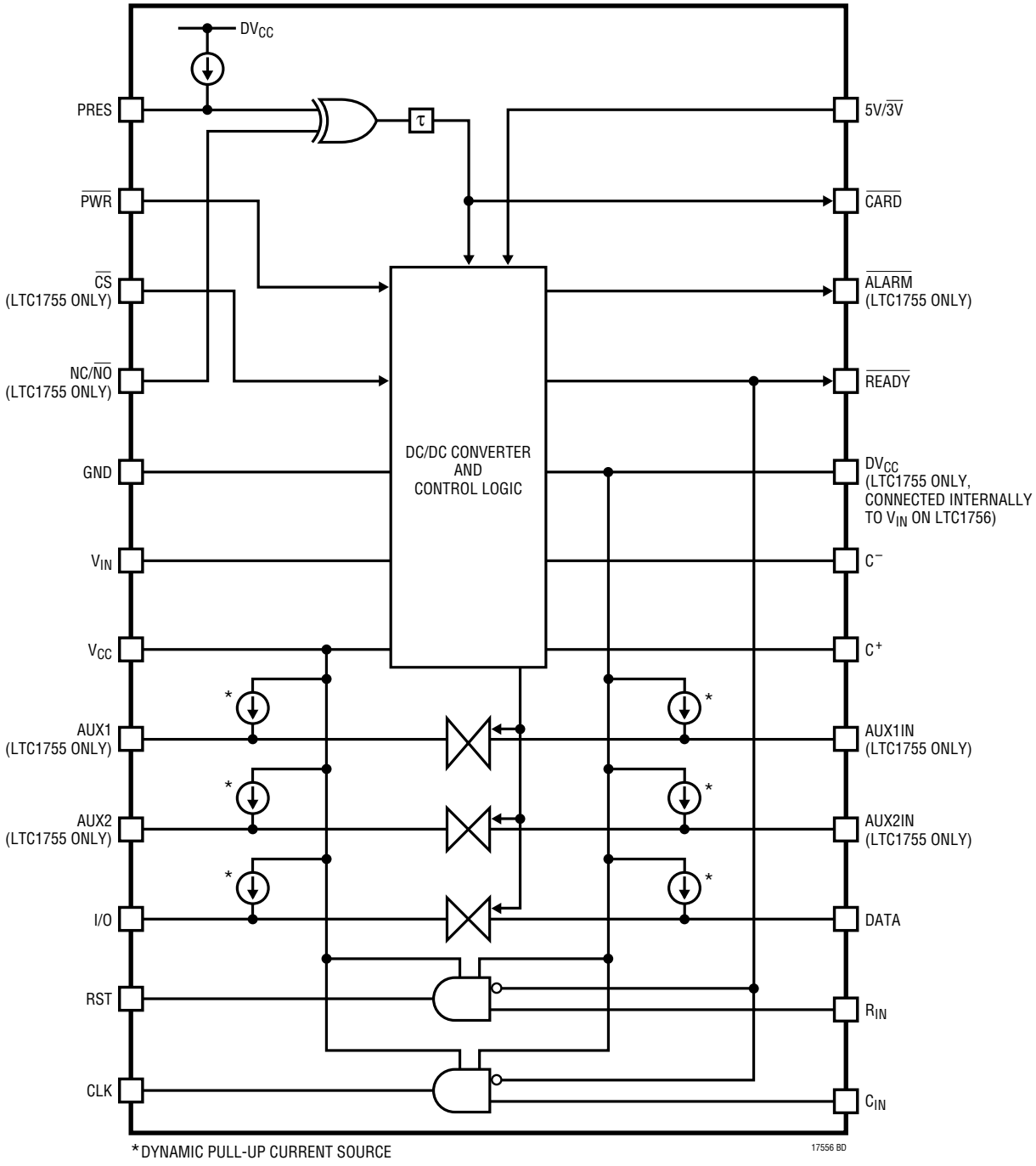
The $\overline{\text{ALARM}}$ pin is configured as an open-drain pull-down with a weak pull-up current source. This permits wired-OR connections of multiple LTC1755s to a single microcontroller.

$\overline{\text{CARD}}$ (Pin 23/15): (Output) Level-Shifted and Debounced PRES Signal from the Smart Card Acceptor Switch. When a valid card indication appears, this pin communicates the presence of the Smart Card to the microcontroller. The $\overline{\text{CARD}}$ pin has an open-drain active pull-down with a weak pull-up current source for logic-OR connections. The debounce circuit ensures that a card has been present for a continuous period of at least 40ms before asserting $\overline{\text{CARD}}$ low. The $\overline{\text{CARD}}$ pin returns high within 50µs of card removal. The PRES pin, in conjunction with the NC/$\overline{\text{NO}}$ pin, determines if a card is present.

5V/$\overline{\text{3V}}$ (Pin 24/16): (Input) Controls the output voltage (V_{CC}) of the DC/DC converter during the Active state. A valid high sets V_{CC} to 5V. A valid low sets V_{CC} to 3V. The 5V/$\overline{\text{3V}}$ pin is latched on the falling edge of the $\overline{\text{PWR}}$ pin. When $\overline{\text{PWR}}$ is low, changes on the 5V/$\overline{\text{3V}}$ pin are ignored. To change the voltage on V_{CC} the LTC1755/LTC1756 must first be returned to the Idle state by bringing the $\overline{\text{PWR}}$ pin high.

DV_{CC} sets the logic reference level for the 5V/$\overline{\text{3V}}$ pin.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

10kV ESD Protection

All Smart Card pins (CLK, RST, I/O, AUX1, AUX2, V_{CC} and GND) can withstand over 10kV of human body model ESD in situ. In order to ensure proper ESD protection, careful board layout is required. The GND pin should be tied directly to a ground plane. The V_{CC} capacitor should be located very close to the V_{CC} pin and tied immediately to the ground plane.

Capacitor Selection

The style and value of capacitors used with the LTC1755/LTC1756 determine several parameters such as output ripple voltage, charge pump strength, Smart Card switch debounce time and V_{CC} discharge rate.

Due to the switching nature of a capacitive charge pump, low equivalent series resistance (ESR) capacitors are recommended for the capacitors at V_{IN} and V_{CC}. Whenever the flying capacitor is switched to the V_{CC} charge storage capacitor, considerable current flows. The product of this high current and the ESR of the output capacitor can generate substantial voltage spikes on the V_{CC} output. These spikes may cause problems with the Smart Card or may interfere with the regulation loop of the LTC1755/LTC1756. Therefore, ceramic or tantalum capacitors are recommended rather than higher ESR aluminum capacitors. Between ceramic and tantalum, ceramic capacitors generally have the lowest ESR. Some manufacturers have developed low ESR tantalum capacitors but they can be expensive and may still have higher ESR than ceramic types. Thus, while they cannot be avoided, ESR spikes will typically be lowest when using ceramic capacitors.

For ceramic capacitors there are several different materials available to choose from. The choice of ceramic material is generally based on factors such as available capacitance, case size, voltage rating, electrical performance and cost. For example, capacitors made of Y5V material have high packing density, which provides high capacitance for a given case size. However, Y5V capacitors tend to lose considerable capacitance over the –40°C to 85°C temperature range. X7R ceramic capacitors are more stable over temperature but don't provide the high packing density. Therefore, large capacitance values are generally not available in X7R ceramic.

The value and style of the flying capacitor are important not only for the charge pump but also because they provide the large debounce time for the Smart Card detection channel. A 0.68µF X7R capacitor is a good choice for the flying capacitor because it provides fairly constant capacitance over temperature and its value is not prohibitively large.

The charge storage capacitor on the V_{CC} pin determines the ripple voltage magnitude and the discharge time of the Smart Card voltage. To minimize ripple, generally, a large value is needed. However, to meet the V_{CC} discharge rate specification, the value should not exceed 20µF. A 10µF capacitor can be used but the ripple magnitude will be higher leading to worse apparent DC load regulation. Typically a 15µF to 18µF Y5V ceramic capacitor is the best choice for the V_{CC} charge storage capacitor. For best performance, this capacitor should be connected as close as possible to the V_{CC} and GND pins. Note that most of the electrostatic discharge (ESD) current on the Smart Card pins is absorbed by this capacitor.

The bypass capacitor at V_{IN} is also important. Large dips on the input supply due to ESR may cause problems with the internal circuitry of the LTC1755/LTC1756. A good choice for the input bypass capacitor is a 10µF Y5V style ceramic

Dynamic Pull-Up Current Sources

The current sources on the bidirectional pins (DATA, AUX2IN, AUX1IN, I/O, AUX2 and AUX1) are dynamically activated to achieve a fast rise time with a relatively small static current (Figure 1). Once a bidirectional pin is relinquished, a small start-up current begins to charge the node. An edge rate detector determines if the pin is

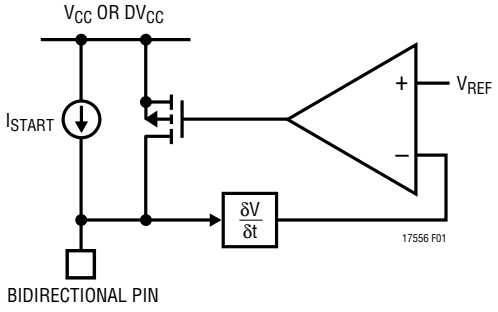


Figure 1. Dynamic Pull-Up Current Sources

APPLICATIONS INFORMATION

released by comparing its slew rate with an internal reference value. If a valid transition is detected, a large pull-up current enhances the edge rate on the node. The higher slew rate corroborates the decision to charge the node thereby effecting a dynamic form of hysteresis. Once the node has reached the power supply voltage the internal comparator requires several hundred nanoseconds to reset. Pulling down on the pin before the reset delay expires will result in a momentary contention and a higher current flow. Therefore, the comparator delay sets the upper limit on the maximum data rate of the bidirectional channels to about 500kHz.

The dynamic pull-up current sources are designed to trigger with as much as 50pF of capacitive load on the bidirectional pins. At approximately 90pF (or greater), the edge rate on the node will be insufficient to trigger the edge rate detector and the node will only ramp up at a rate given by the I_{START} current source and the load capacitance. In these instances the edge rate of the bidirectional pin may not meet the requirements of existing smart card standards. Therefore, it is recommended that the sum of both explicit and parasitic capacitances on the bidirectional pins be kept below 50pF.

If excessive capacitance (either explicit or parasitic) is present on the bidirectional pins, the starting pull-up current must also be increased. This can be accomplished with a pull-up resistor to the respective supply. For the smart card side (I/O, AUX1 and AUX2), the pull-up resistor should be connected to V_{CC}. For the microcontroller side (DATA, AUX1IN and AUX2IN), the pull-up resistor should be connected to DV_{CC} on the LTC1755 (V_{IN} on the LTC1756). To maintain an edge rate of approximately 5V/µs, the following expression for $R_{PULL-UP}$ should be applied:

$$R_{PULL-UP} = \frac{V_{SUPPLY} - 1V}{\left(C_{PAR} - 50pF\right)\left(5 \bullet 10^6\right)}$$

where C_{PAR} is the extra capacitance on the bidirectional pin and V_{SUPPLY} is the minimum local supply for the bidirectional pin. For example, on the smart card side, 3V should be assumed for V_{SUPPLY}.

Note that the addition of a pull-up resistor will give a higher output voltage when the bidirectional pin pulls down. Care should be taken so that the V_{IL} or V_{OL} specifications are not compromised with this technique.

Bidirectional Channels

As described in Pin Functions (Pins 10/6), the bidirectional channels allow transmission in only one direction at a time. Figure 2 shows a simplified block diagram of one of the three bidirectional channels. The three channels operate in an identical fashion.

Figure 3 shows an example of normal transmit and receive operations as well as the two possible collision scenarios. If a channel is activated from one direction and an L is imposed in the other direction before both sides return H a collision results. The result of the collision is that the receiving side (*Slave Side*) will remain low until it is released, but the transmitting side (first side to go low or *Master Side*), will be allowed to return high if released. The colliding L externally imposed on the slave side will not be transmitted back through the channel.

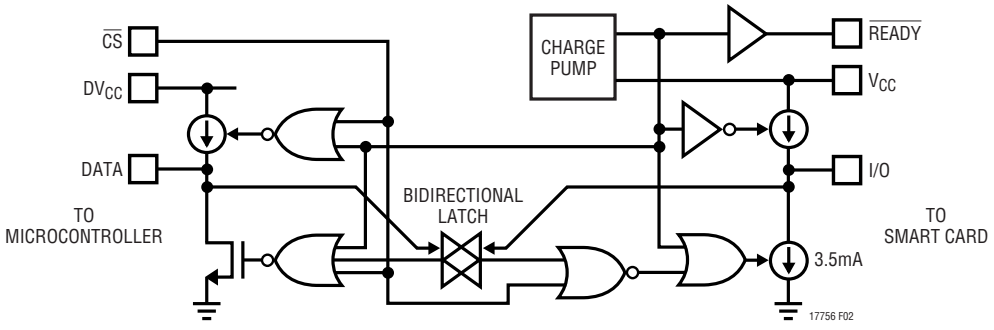


Figure 2. Bidirectional Channel Simplified Block Diagram

APPLICATIONS INFORMATION

I²C™ Compatibility

Some smart cards still require I²C compatibility. In the I²C format it is permissible to impose an L before the signal line has returned H. This is used, for example, as an acknowledge signal. Such a scenario will cause a collision as shown in Figure 3.

Figure 4 shows an analog level translation technique that can be used along with the LTC1755 to support I²C smart cards. In this technique it is important to connect the gate of the external MOSFET to the lower of the two supplies (i.e., the lower of V_{CC} or DV_{CC}). If DV_{CC} is operating from a fixed 5V supply, the gate of MN1 should be connected to V_{CC}. If DV_{CC} is operating from a regulated 3.3V supply, the gate of MN1 should be connected to DV_{CC}. In the latter case, the gate may need to be connected to a digital signal ranging from 0V to DV_{CC} so that it can be disabled when the LTC1755 is in shutdown. Otherwise, the the LTC1755 will try to assert an L on the microcontroller side of the channel when it is in shutdown.

Supporting Synchronous and Asyncronous Cards

In synchronous/asynchronous applications it is necessary to switch the CLK pin of the card socket from a free running asynchronous clock to a controlled syncronous clock. To avoid glitches and pulses shorter than the minimum allowed pulse width, the circuit shown in Figure 5 should be used as a clock selection circuit. Note that for this circuit to be effective the SYNC input should be held constant while switching the ASYNC\$\overline{\text{SYNC}}$ control signal.

Low Power Operation

The LTC1755/LTC1756 are inherently low power devices. When there is no Smart Card present the supply current is less than 10µA. If DV_{CC} is 0V the current drops below 1µA. When a Smart Card is present the LTC1755/LTC1756 operate with a quiescent current of only 60µA, thus the majority of power is consumed by charge pump losses and the card itself. If the card can be made to consume less power during idle times a significant power savings will be achieved. Whenever possible Clock Stop Mode should be used (or alternatively a very low "idling" clock speed). Furthermore, in the Active state, the bidirectional pins should all be relinquished whenever possible since there is some static current flow when a bidirectional pin is pulled down.

I²C is a trademark of Philips Electronics N.V.

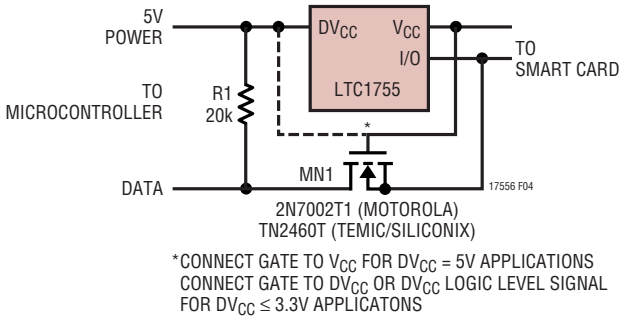


Figure 4. I²C Level Translation Technique

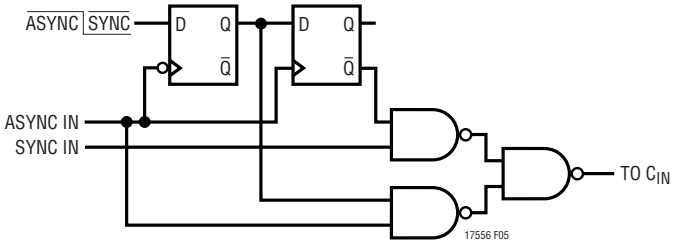


Figure 5. Glitchless Clock Selection Circuit

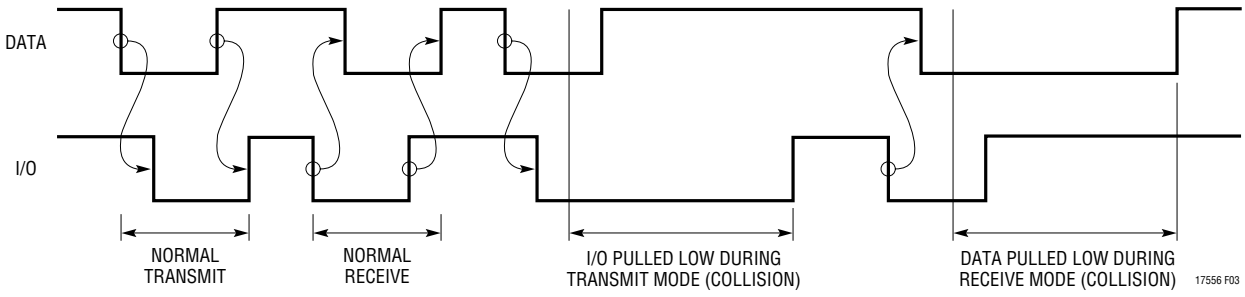


Figure 3. Possible Bidirectional Channel Scenarios

APPLICATIONS INFORMATION

Overtemperature Fault Protection

An overtemperature circuit disables the chip and activates the $\overline{\text{ALARM}}$ pin if the IC's junction temperature exceeds 150°C.

Self-Start Mode

By connecting the $\overline{\text{CARD}}$ pin to the $\overline{\text{PWR}}$ pin, the LTC1755/LTC1756 can be made to start up automatically when a Smart Card is detected (Figure 6). In this mode, the $\overline{\text{READY}}$ pin becomes an interrupt signal indicating to the microcontroller that a Smart Card is present and that V_{CC}, the charge pump voltage, is at its final value. The Smart Card remains powered as long as it is detected by the PRES pin. When the Smart Card is removed the LTC1755/LTC1756 will automatically be deactivated by the fault detection circuitry.

Deactivation Sequence

For maximum flexibility the Smart Card can be deactivated either manually or automatically. In manual mode the deactivation is controlled by explicitly manipulating the LTC1755/LTC1756 input and control pins (DATA, AUX1IN, AUX2IN, RIN and CIN followed by $\overline{\text{PWR}}$ and $\overline{\text{CS}}$). In automatic mode the $\overline{\text{PWR}}$ pin is used to perform the built-in deactivation sequence. Once $\overline{\text{PWR}}$ is brought high the built-in deactivation sequence occurs as shown in Figure 7.

In the event of a fault, the LTC1755/LTC1756 automatically implement the built-in deactivation sequence.

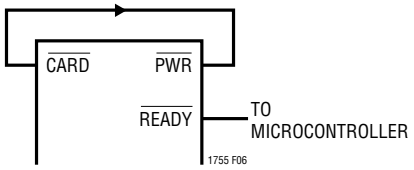


Figure 6. Self-Start Mode

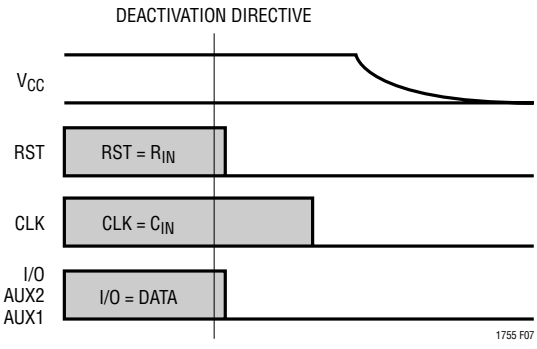


Figure 7. Deactivation Sequence

PC Board Layout

For best performance, the V_{IN} and V_{CC} capacitors should be placed as close to the LTC1755/LTC1756 as possible. This will help reduce ringing due to inductance on the V_{IN} and V_{CC} pins that could cause problems with the LTC1755/LTC1756 control circuitry or Smart Card. Figure 8 illustrates a possible layout technique using only a single layer of the PC board.

State Definitions

IDLE/DEACTIVATION

V_{CC}, RST, CLK, I/O AUX2, AUX1 = L

$\overline{\text{READY}}$, $\overline{\text{ALARM}}$, DATA, AUX2IN, AUX1IN = Z

$\overline{\text{CARD}}$ = PRES ⊕ NC/$\overline{\text{NO}}$

Once the LTC1755/LTC1756 enter the Idle/Deactivation state the deactivation sequence begins. The deactivation sequence will continue until V_{CC} is discharged to approximately 1V. An activation command ($\overline{\text{PWR}}$ = 0V) will only be acknowledged once this occurs.

ALARM/DEACTIVATION

Same as Idle/Deactivation except:

$\overline{\text{ALARM}}$ = L

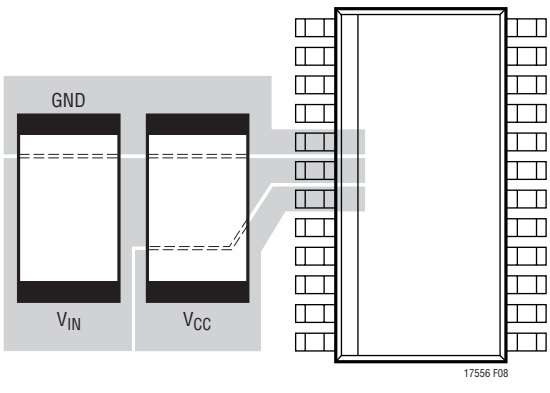


Figure 8. Optimum Bypass Capacitor Placement

APPLICATIONS INFORMATION

The only possible next state is Idle/Deactivation which is achieved by disabling the LTC1755/LTC1756 via the $\overline{PWR}$ pin (i.e., $\overline{PWR} = DV_{CC}$).

The alarm indication can be cleared by rapidly cycling the $\overline{PWR}$ pin. However, a new activation cycle will not begin until V_{CC} is or has dropped below approximately 1V.

ACTIVE

V_{CC} = 3V or 5V (as determined by the 5V/$\overline{3V}$ pin)

RST = R_{IN}, CLK = C_{IN}

I/O, AUX2, AUX1, DATA, AUX2IN, AUX1IN = Ready for data (after $\overline{READY}$ becomes low)

$\overline{CARD}$ = PRES ⊕ NC/$\overline{NO}$

$\overline{ALARM}$ = H

FAULT TIMEOUT

Same as Active except:

The duration of a fault is being measured. If the fault duration exceeds 5µs then the Alarm/Deactivation state follows. If the fault duration is less than 5µs, then the device is returned to the Active state.

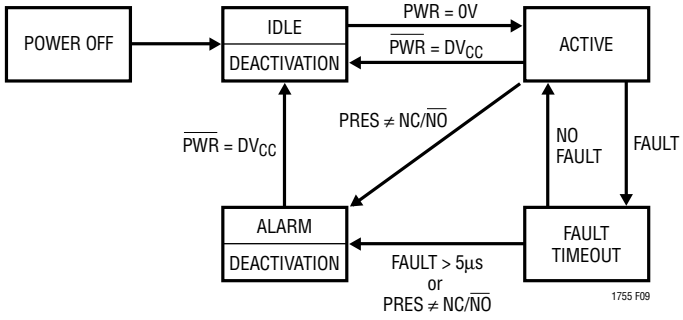
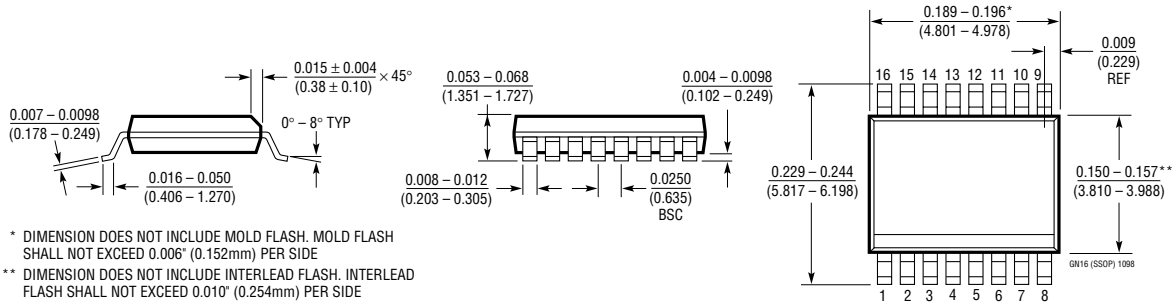


Figure 9. LTC1755/LTC1756 State Diagram

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

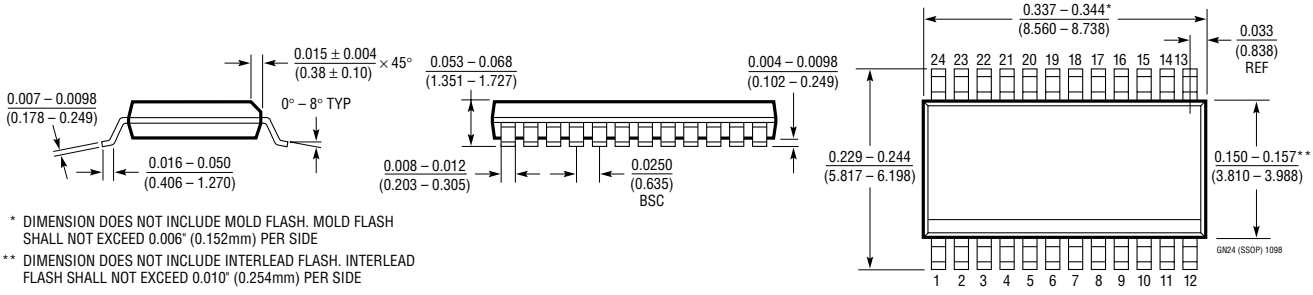
GN Package
16-Lead Plastic SSOP (Narrow 0.150)
(LTC DWG # 05-08-1641)



* DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

** DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

GN Package
24-Lead Plastic SSOP (Narrow 0.150)
(LTC DWG # 05-08-1641)

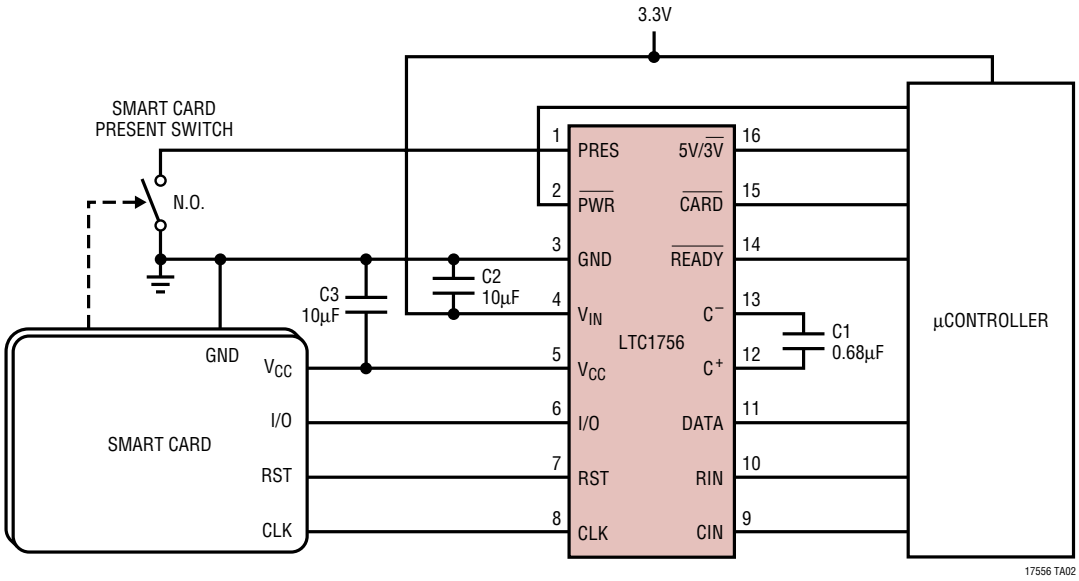


* DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

** DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

TYPICAL APPLICATION

Asynchronous Smart Card Interface



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1514/LTC1515	Micropower Step-Up/Step-Down Inductorless DC/DC Converters	Regulated Output Up to 50mA, V_{IN} from 2V to 10V, SO-8 Package
LTC1516	Micropower Regulated 5V Charge Pump	5V/50mA Output from 2V to 5V Input, S0-8 Package
LTC1555/LTC1556	SIM Power Supply and Level Translator	Step-Up/Step-Down Charge Pump + Generates 3V or 5V
LTC1754-5	5V Charge Pump with Shutdown in SOT-23	V_{IN} from 2.7V to 5.5V, 50mA Output with $V_{IN} \geq 3V$
LTC1986	3V/5V SIM Power Supply in SOT-23	V_{IN} from 2.6V to 4.4V, 3V/5V Output at 10mA