



# AOT474/AOTF474

## N-Channel Enhancement Mode Field Effect Transistor

### General Description

The AOT(F)474/L uses a robust technology that is designed to provide efficient and reliable power conversion even in the most demanding applications, including motor control. With low  $R_{DS(ON)}$  and excellent thermal capability this device is appropriate for high current switching and can endure adverse operating conditions.

AOT(F)474/AOT(F)474L are electrically Identical

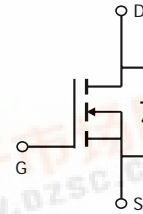
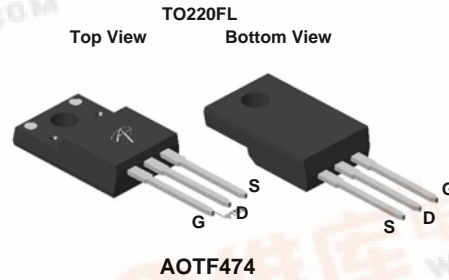
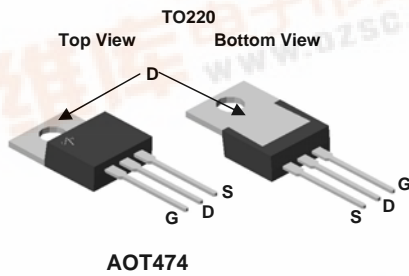
AOT(F)474 -RoHS Compliant

AOT(F)474L -Halogen Free

### Product Summary

$V_{DS}$	75V
$I_{D\_TO220}$ (at $V_{GS}=10V$ )	127A
$I_{D\_TO220FL}$ (at $V_{GS}=10V$ )	47A
$R_{DS(ON)}$ (at $V_{GS}=10V$ )	< 11.3mΩ

100% UIS Tested



### Absolute Maximum Ratings $T_A=25^{\circ}C$ unless otherwise noted

Parameter	Symbol	AOT474	AOTF474	Units	
Drain-Source Voltage	$V_{DS}$	75		V	
Gate-Source Voltage	$V_{GS}$	±25		V	
Continuous Drain Current	$I_D$	$T_C=25^{\circ}C$	127	47	A
		$T_C=100^{\circ}C$	89	33	
Pulsed Drain Current <sup>C</sup>	$I_{DM}$	200			
Continuous Drain Current	$I_{DSM}$	$T_A=25^{\circ}C$	9	9	A
		$T_A=70^{\circ}C$	7	7	
Avalanche Current <sup>C</sup>	$I_{AR}$	106		A	
Repetitive avalanche energy $L=0.1mH$ <sup>C</sup>	$E_{AR}$	562		mJ	
Power Dissipation <sup>B</sup>	$P_D$	$T_C=25^{\circ}C$	417	57.5	W
		$T_C=100^{\circ}C$	208	29	
Power Dissipation <sup>A</sup>	$P_{DSM}$	$T_A=25^{\circ}C$	1.9	1.9	W
		$T_A=70^{\circ}C$	1.2	1.2	
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 175		$^{\circ}C$	

### Thermal Characteristics

Parameter	Symbol	AOT474	AOTF474	Units
Maximum Junction-to-Ambient <sup>A</sup>	$R_{\theta JA}$	13.9	13.9	$^{\circ}C/W$
Maximum Junction-to-Ambient <sup>A,D</sup>		Steady-State	65	65
Maximum Junction-to-Case	$R_{\theta JC}$	0.36	2.6	$^{\circ}C/W$



**Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> =250μA, V <sub>GS</sub> =0V	75			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =75V, V <sub>GS</sub> =0V T <sub>J</sub> =55°C			1 5	μA
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> = ±25V			100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> I <sub>D</sub> =250μA	2.6	3.4	4	V
I <sub>D(ON)</sub>	On state drain current	V <sub>GS</sub> =10V, V <sub>DS</sub> =5V	200			A
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =30A T <sub>J</sub> =125°C		9.4 18	11.3 21.5	mΩ
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =30A		67		S
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =1A, V <sub>GS</sub> =0V		0.73	1	V
I <sub>S</sub>	Maximum Body-Diode Continuous Current				128	A
<b>DYNAMIC PARAMETERS</b>						
C <sub>ISS</sub>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =30V, f=1MHz	2240	2805	3370	pF
C <sub>OSS</sub>	Output Capacitance		355	507	660	pF
C <sub>RSS</sub>	Reverse Transfer Capacitance		22	36	50	pF
R <sub>g</sub>	Gate resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1MHz	1.4	2.8	4.2	Ω
<b>SWITCHING PARAMETERS</b>						
Q <sub>g(10V)</sub>	Total Gate Charge	V <sub>GS</sub> =10V, V <sub>DS</sub> =30V, I <sub>D</sub> =30A	39	49.6	60	nC
Q <sub>gs</sub>	Gate Source Charge		11	13.8	17	nC
Q <sub>gd</sub>	Gate Drain Charge		8	14	20	nC
t <sub>D(on)</sub>	Turn-On DelayTime	V <sub>GS</sub> =10V, V <sub>DS</sub> =30V, R <sub>L</sub> =1Ω, R <sub>GEN</sub> =3Ω		15		ns
t <sub>r</sub>	Turn-On Rise Time			34		ns
t <sub>D(off)</sub>	Turn-Off DelayTime			42		ns
t <sub>f</sub>	Turn-Off Fall Time			4.5		ns
t <sub>rr</sub>	Body Diode Reverse Recovery Time	I <sub>F</sub> =30A, dI/dt=500A/μs	35	50	65	ns
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> =30A, dI/dt=500A/μs	330	472	614	nC

A. The value of R<sub>θJA</sub> is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub> =25°C. The Power dissipation P<sub>DSM</sub> is based on R<sub>θJA</sub> and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175°C may be used if the PCB allows it.

B. The power dissipation P<sub>D</sub> is based on T<sub>J(MAX)</sub>=175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature T<sub>J(MAX)</sub>=175°C. Ratings are based on low frequency and duty cycles to keep initial T<sub>J</sub> =25°C.

D. The R<sub>θJA</sub> is the sum of the thermal impedance from junction to case R<sub>θJC</sub> and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

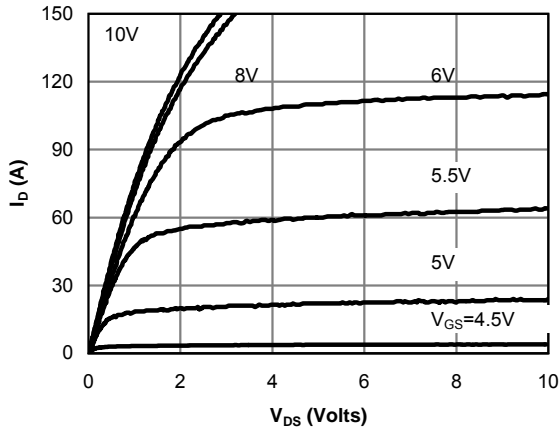
F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T<sub>J(MAX)</sub>=175°C. The SOA curve provides a single pulse rating.

G. These tests are performed with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25°C.

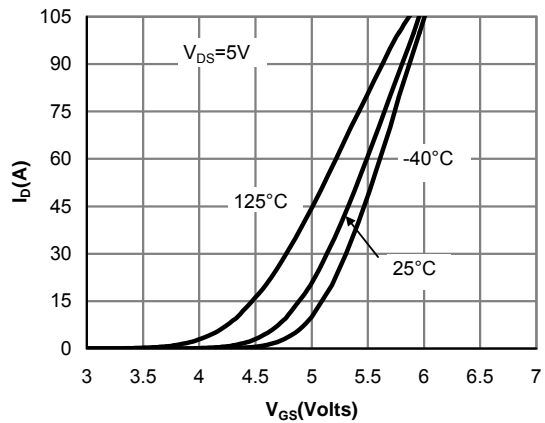
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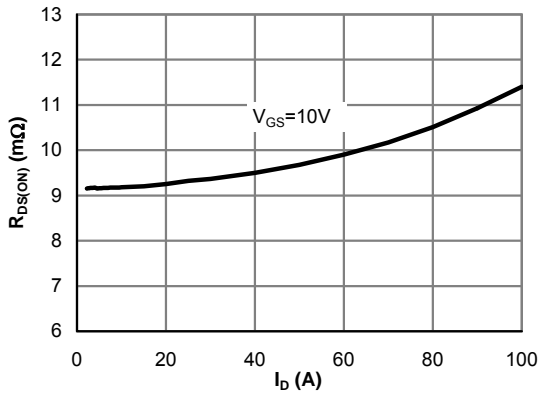
**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



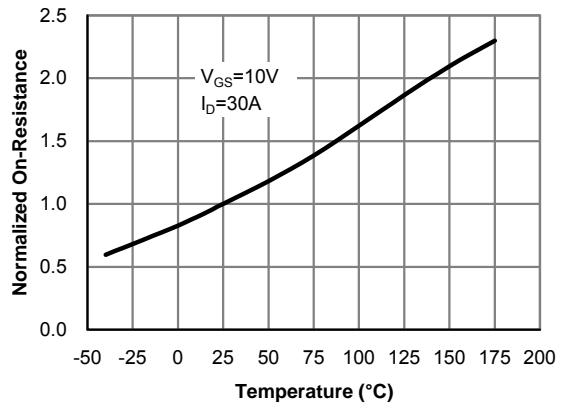
**Fig 1: On-Region Characteristics (Note E)**



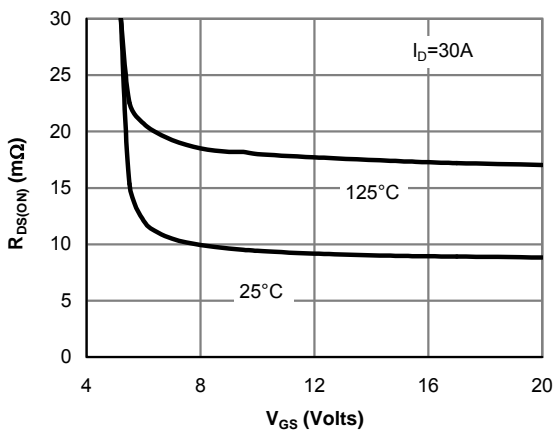
**Figure 2: Transfer Characteristics (Note E)**



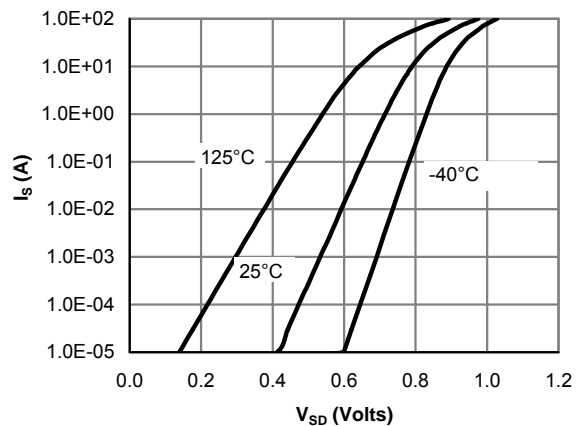
**Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)**



**Figure 4: On-Resistance vs. Junction Temperature (Note E)**



**Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)**



**Figure 6: Body-Diode Characteristics (Note E)**

**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

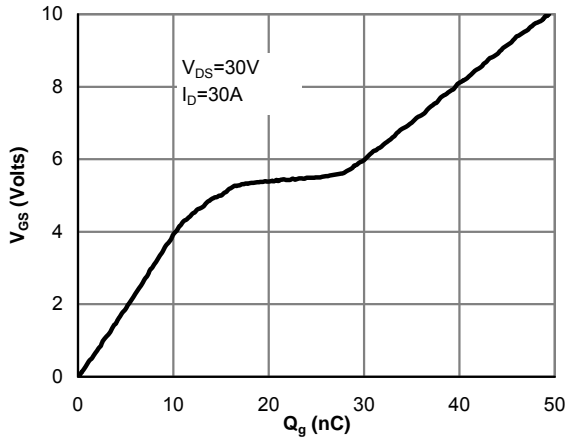


Figure 7: Gate-Charge Characteristics

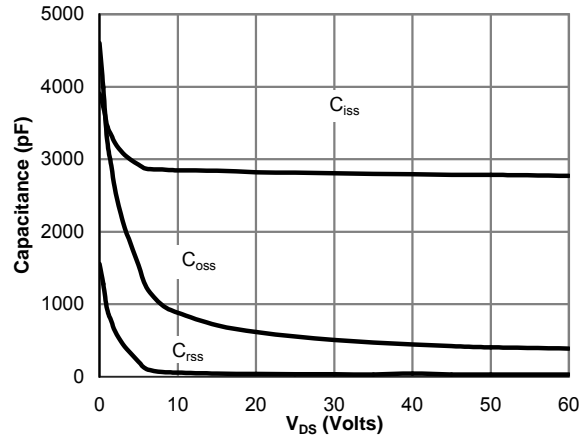


Figure 8: Capacitance Characteristics

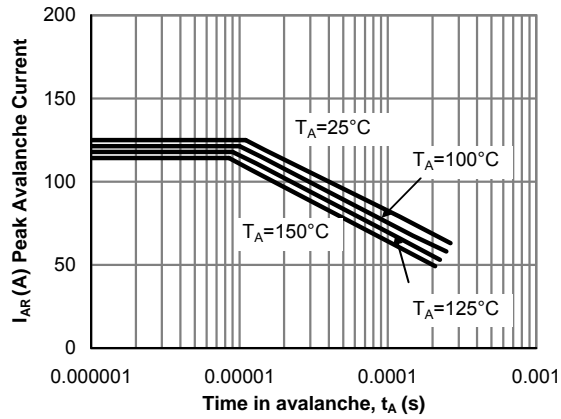


Figure 9: Single Pulse Avalanche capability (Note C)

**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

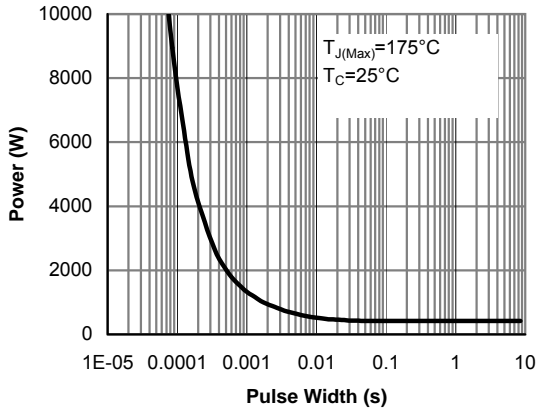


Figure 10: Single Pulse Power Rating Junction-to-Case for AOT474 (Note F)

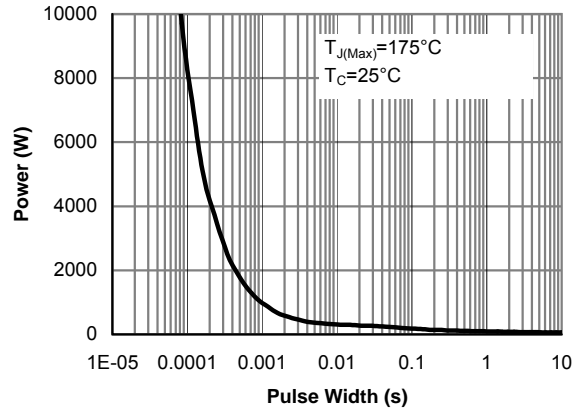


Figure 11: Single Pulse Power Rating Junction-to-Case for AOTF474 (Note F)

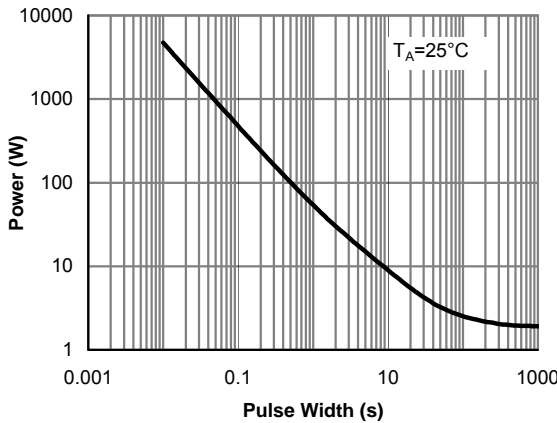


Figure 12: Single Pulse Power Rating Junction-to-Ambient for AOT474 (Note G)

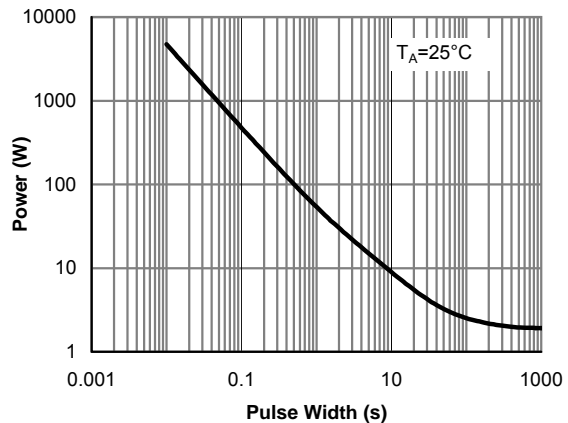


Figure 13: Single Pulse Power Rating Junction-to-Ambient for AOTF474 (Note G)

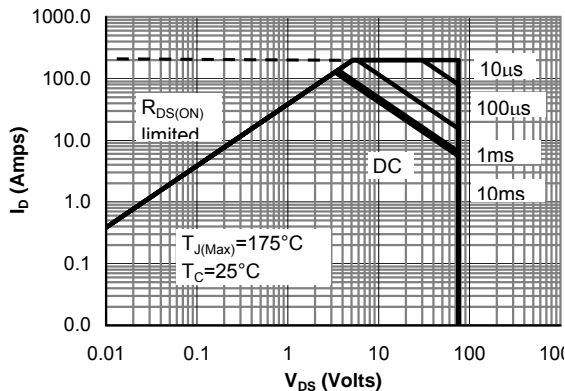


Figure 14: Maximum Forward Biased Safe Operating Area for AOT474 (Note F)

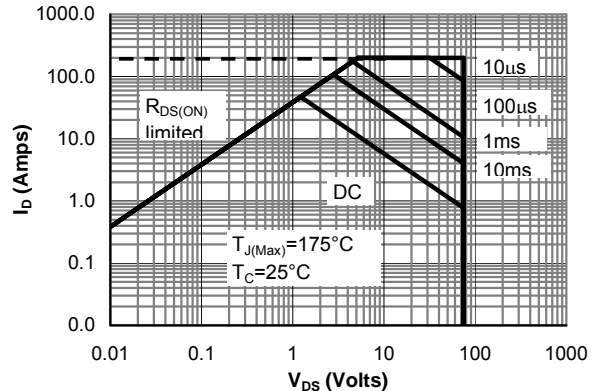
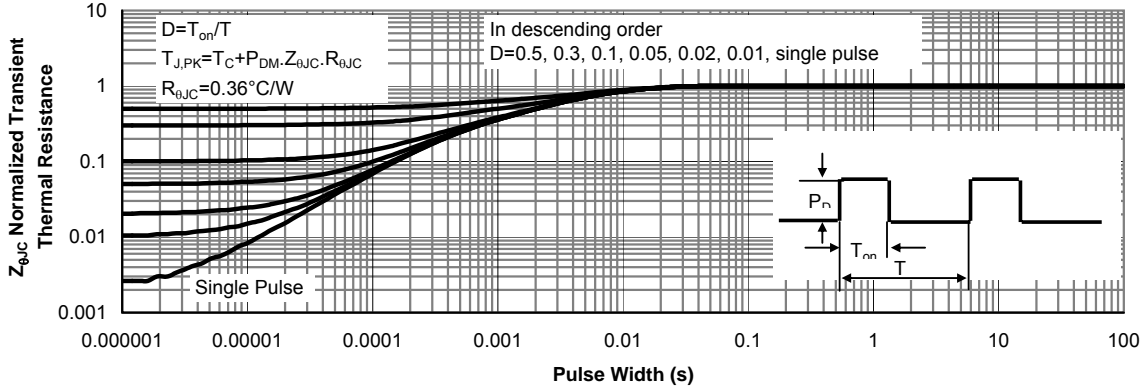
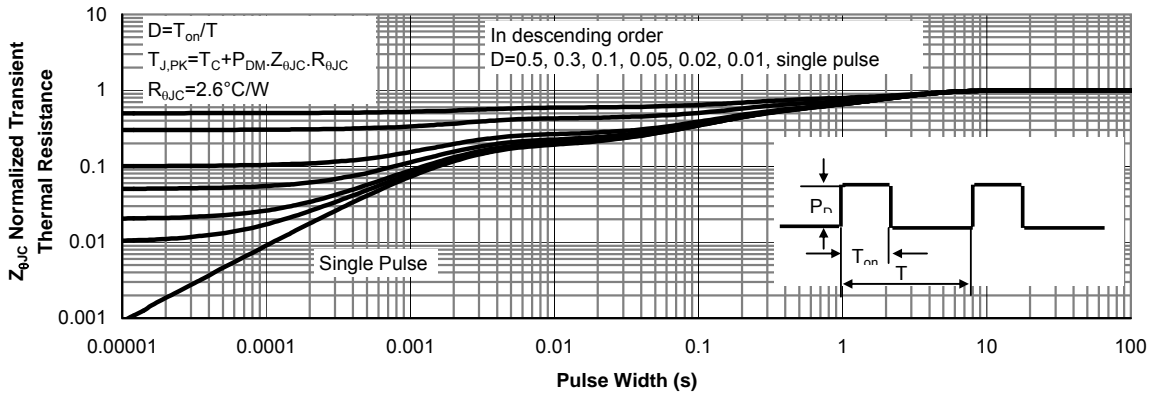


Figure 15: Maximum Forward Biased Safe Operating Area for AOTF474 (Note F)

**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

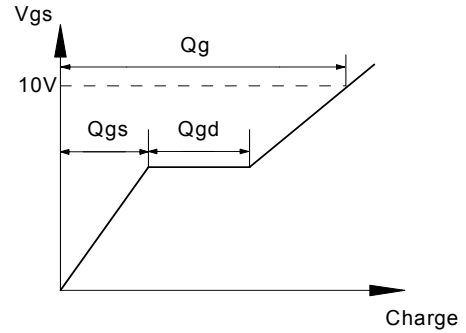
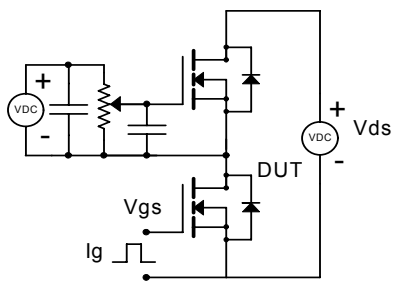


**Figure 16: Normalized Maximum Transient Thermal Impedance for AOT474 (Note F)**

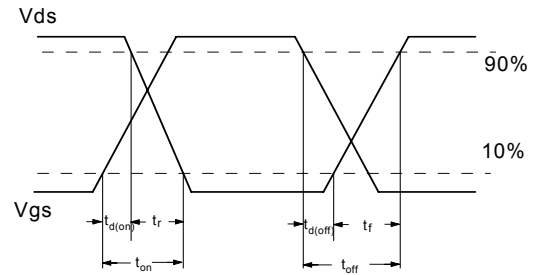
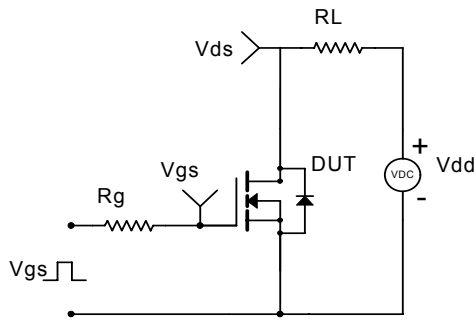


**Figure 17: Normalized Maximum Transient Thermal Impedance for AOTF474 (Note F)**

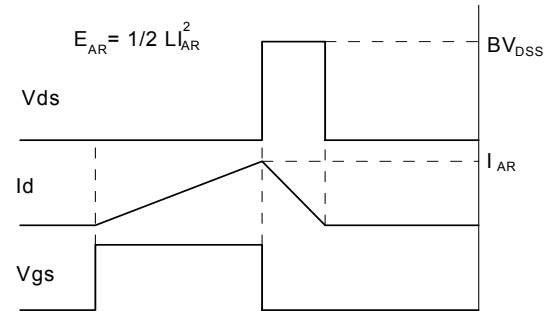
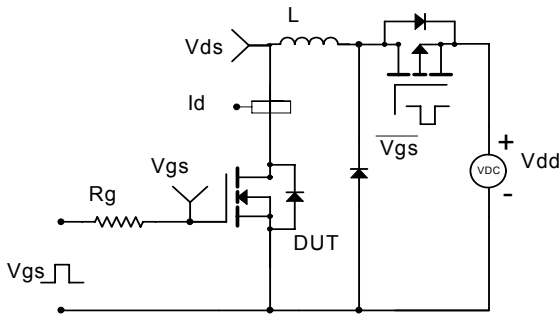
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

