LTC3824

High Voltage Step-Down Controller With 40µA Quiescent Current

FEATURES

- **Wide Input Range: 4V to 60V**
- **Current Mode Constant Frequency PWM**
- **Very Low Dropout Operation: 100% Duty Cycle**
- **Programmable Switching Frequency: 200kHz to 600kHz**
- **Selectable High Efficient Burst Mode® Operation: 40µA Quiescent Current**
- **Easy Synchronization**
- 8V, 2A Gate Drive (V_{CC} > 10V) for Industrial High Voltage P-channel MOSFET
- Programmable Soft-Start
- Programmable Current Limit
- Available in a Small 10-Pin Thermally Enhanced MSE Package

APPLICATIONS

- Industrial and Automotive Power Supplies
- Telecom Power Supplies
- Distributed Power Systems

DESCRIPTION

The LTC®3824 is a step-down DC/DC controller designed to drive an external P-channel MOSFET. With a wide input range of 4V to 60V and a high voltage gate driver, the LTC3824 is suitable for many industrial and automotive high power applications. Constant frequency current mode operation provides excellent performance.

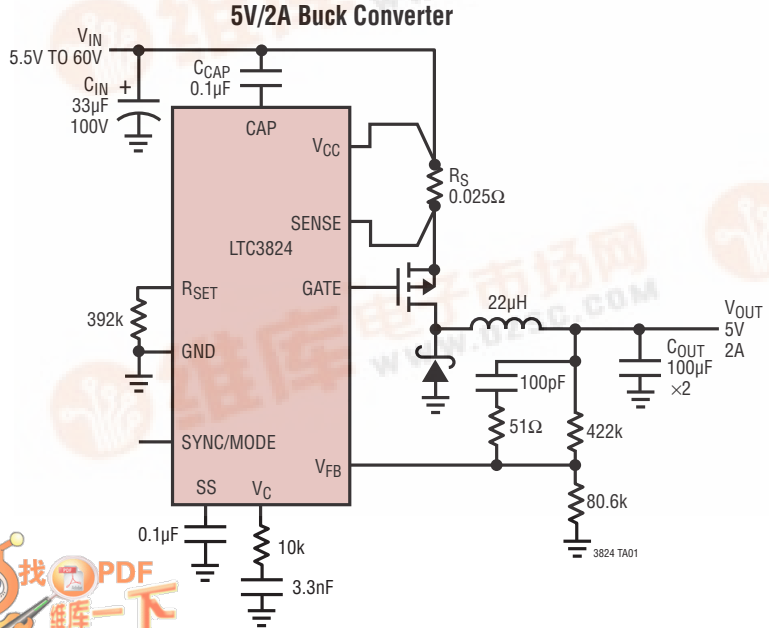
The LTC3824 can be configured for Burst Mode operation. Burst Mode operation enhances low current efficiency (only 40µA quiescent current) and extends battery run time. The switching frequency can be programmed up to 600kHz and is easily synchronizable.

Other features include current limit, soft-start, micropower shutdown, and Burst Mode disable.

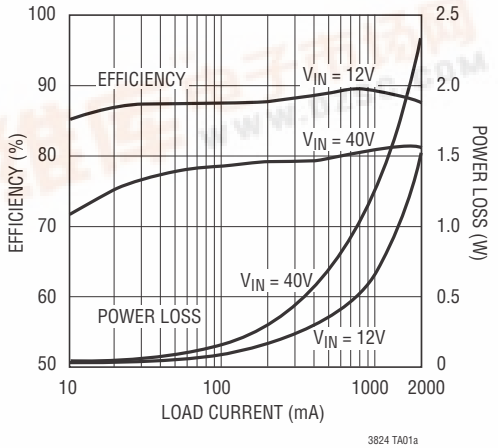
The LTC3824 is available in a 10-lead MSE power package.

TYPICAL APPLICATION

5V/2A Buck Converter



Efficiency and Power Loss vs Load Current

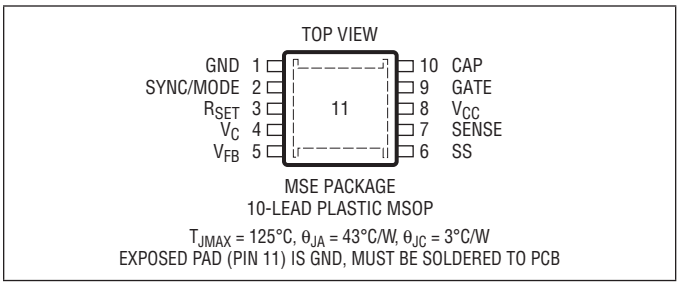


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{CC} 65V
SS, R_{SET}, V_{FB} 4V
V_C 3V
SYNC/MODE 6V
$V_{CC} – V_{SENSE}$ 1V
Maximum Temperatures (Note 2)
LTC3824E..... –40°C to 85°C
LTC3824I..... –40°C to 125°C
Storage Temperature Range..... –65° to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PIN CONFIGURATION



MSE PACKAGE
10-LEAD PLASTIC MSOP

T_{JMAX} = 125°C, θ_{JA} = 43°C/W, θ_{JC} = 3°C/W
EXPOSED PAD (PIN 11) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3824EMSE#PBF	LTC3824EMSE#TRPBF	LTBRZ	10-Lead Plastic MSOP	–40°C to 85°C
LTC3824IMSE#PBF	LTC3824IMSE#TRPBF	LTCGZ	10-Lead Plastic MSOP	–40°C to 125°C
LEAD BASED FINISH	**TAPE AND REEL**	**PART MARKING**	**PACKAGE DESCRIPTION**	**TEMPERATURE RANGE**
LTC3824EMSE	LTC3824EMSE#TR	LTBRZ	10-Lead Plastic MSOP	–40°C to 85°C
LTC3824IMSE	LTC3824IMSE#TR	LTCGZ	10-Lead Plastic MSOP	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 12V, R_{SET} = 392k, C_{CAP} = 0.1µF. No load on any outputs, unless otherwise specified.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage (V_{CC})		●	4		60	V
Supply Current (I_{VCC})	$V_C \le 0.4V$ (Switching Off), $V_{CC} \le 60V$ V_{SYNC} = 0V (Burst Mode Operation Disable)			0.8	1.3	mA
Supply Current (I_{VCC}) Burst Mode Operation	$V_{CC} \le 60V$, SYNC/MODE Open, V_C = 0.6V			40	65	µA
Supply Current in Shutdown	$V_C \le 25mV$, $V_{CC} \le 60V$			7		µA
VOLTAGE AMPLIFIER gm						
Reference Voltage (V_{REF})		 ●	0.792 0.788	0.8	0.808 0.812	V V
Transconductance	V_C = 0.8V, ΔI_{VC} = ±2µA		220	260	370	µmho
FB Input Current	$V_{FB} = V_{REF}$ (Note 3)	●		10	30	nA
V_C High	I_{VC} = 0			1.6		V
V_C Low	I_{VC} = 0			0.35	0.5	V
V_C Source Current	V_{VC} = 0.5V to 1.3V, $V_{FB} = V_{REF}$ –100mV (V_{SYNC} = 0V)			15		µA
V_C Sink Current	V_{VC} = 0.7V to 1.3V, $V_{FB} = V_{REF}$ +100mV (V_{SYNC} = 0V)			15		µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 12V, R_{SET} = 392k, C_{CAP} = 0.1µF. No load on any outputs, unless otherwise specified.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_C Threshold for Switching Off	$V_{SYNC/MODE}$ = 0V (Note 4)	●			0.4	V
Soft-Start Current I_{SS}	V_{SS} = 0.1V to 1.5V			5		µA
V_C Burst Mode Threshold	V_{CC} ≤ 60V, V_C Rising, SYNC/MODE Open			0.84		V
V_C Burst Mode Threshold Hysteresis	V_{CC} ≤ 60V			0.04		V
SENSE Voltage at Burst Mode Operation	(V_{CC}–V_{SENSE}) at 30% Duty Cycle 70% Duty Cycle			30 20		mV mV
Current Limit Threshold (V_{CC}–V_{SENSE})	V_{CC} ≤ 60V	●	80	100	120	mV
FB Overvoltage Threshold	V_C = 1.6V			8		%
Sense Input Current	V_{SENSE} = V_{CC}			0.1	2	µA
OSCILLATOR						
Switching Frequency	R_{SET} = 392k R_{SET} = 200k	● ●	170 320	200 400	230 460	kHz kHz
Synchronization Pulse Threshold on SYNC Pin	Rising Edge V_{SYNC}				1.3	V
Synchronization Frequency Range	R_{SET} = 392k R_{SET} = 200k	● ●	230 460		300 600	kHz kHz
V_{RSET}	R_{SET} = 392k			1.2		V
Minimum On-Time (Measured at GATE Pin)	3V Buck Converter Circuit, I_{LOAD} > 2A			350		ns
Switching Frequency Foldback	V_{FB} = 0.3V	●	35	50	75	kHz
GATE DRIVER						
GATE Bias Voltage (V_{CC}–V_{CAP})	9V ≤ V_{CC} ≤ 60V, I_{GATE} = 10mA V_{CC} = 12V, I_{GATE} = 15mA	● ●	7.0 6.8	7.9	8.8	V V
GATE Bias Voltage (V_{CAP}–GND)	4V ≤ V_{CC} ≤ 8V, I_{GATE} = 10mA 6V ≤ V_{CC} ≤ 8V, I_{GATE} = 15mA, V_{CC} = 12V	 ●	0.2	0.85	1.5 2.8	V V
GATE High Voltage (V_{CC}–V_{GATE})	4V ≤ V_{CC} ≤ 60V, I_{GATE} = –15mA			0.5	0.8	V
GATE Peak Source Current	C_{GATE} = 10nF			2.5		A
GATE Low Voltage (V_{GATE}–V_{CAP})	8V ≤ V_{CC} ≤ 60V, I_{GATE} = 15mA 4V ≤ V_{CC} < 8V, I_{GATE} = 10mA			0.1 0.05	0.5	V V
GATE Peak Sink Current	C_{GATE} = 10nF			2.5		A

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

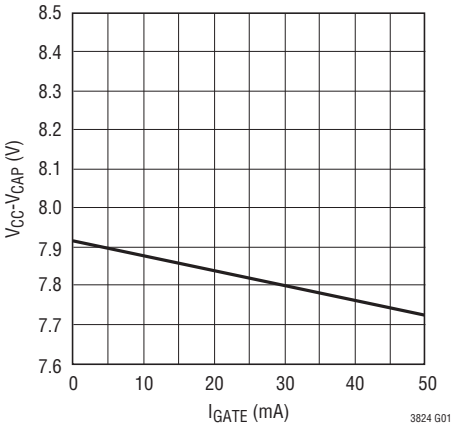
Note 2: The LTC3824E is guaranteed to meet performance specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 85°C temperature range are assured by design characterization and correlation with statistical process controls. The LTC3824I grade is guaranteed over the full –40°C to 125°C operating junction temperature range.

Note 3: This parameter is tested in a feedback loop that servos V_{FB} to the reference voltage with the V_C pin forced to 1V.

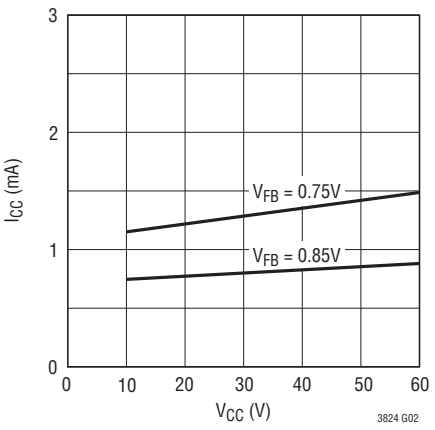
Note 4: This specification represents the maximum voltage on V_C where switching (GATE pin) is guaranteed to be off.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise noted.

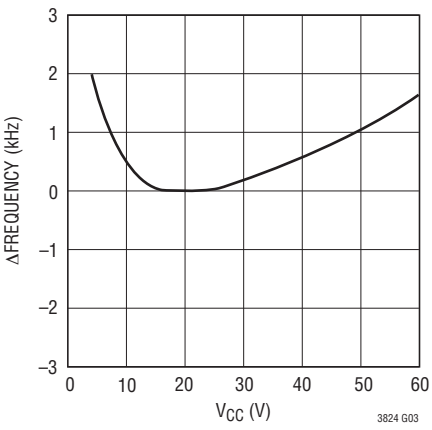
(V_{CC}-V_{CAP}) vs I_{GATE} at V_{DRIVE} Low



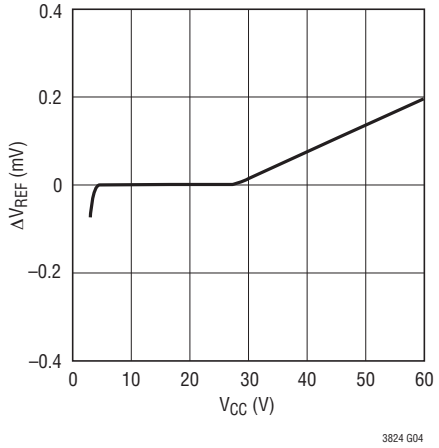
I_{CC} vs V_{CC}



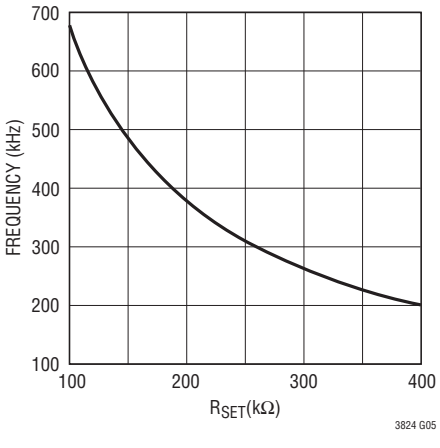
Switching Frequency Change vs V_{CC} at R_{SET} = 392kΩ



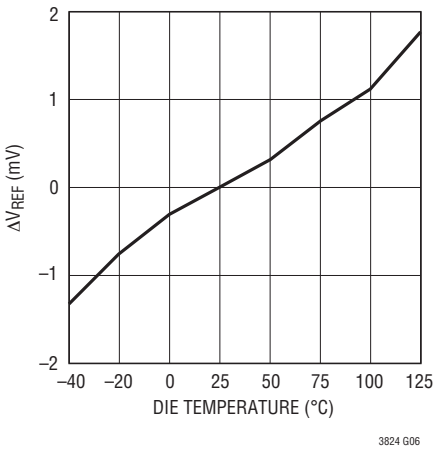
V_{REF} Change vs V_{CC}



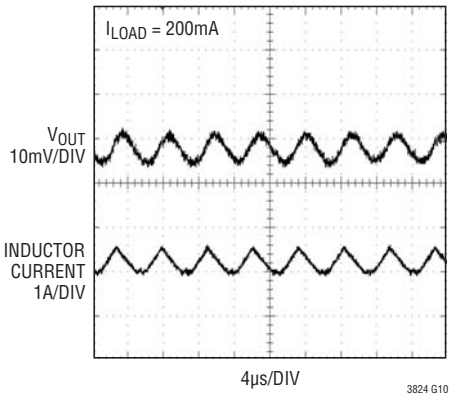
Switching Frequency vs R_{SET}



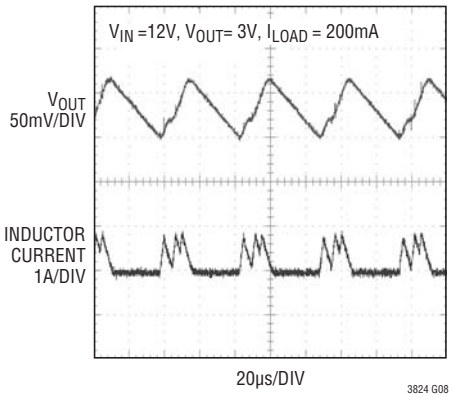
ΔV_{REF} vs Temperature



Burst Mode Disabled at I_{LOAD} = 200mA, V_{OUT} = 5V

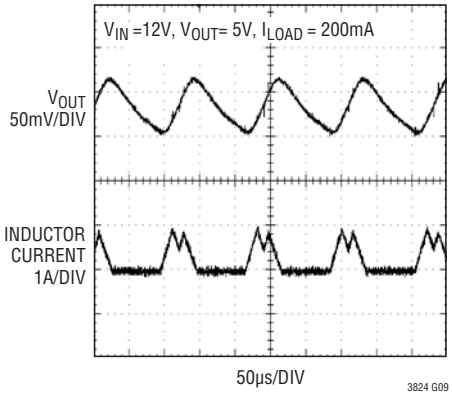


Burst Mode Operation V_{OUT} = 3V

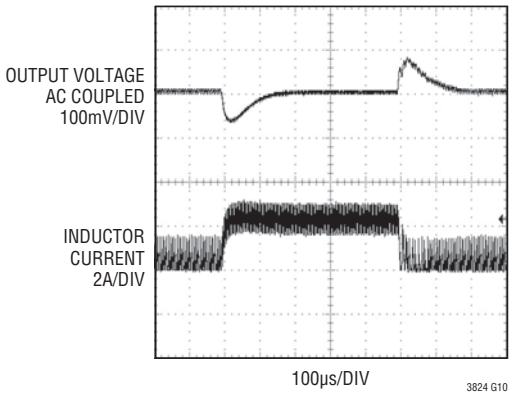


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise noted.

Burst Mode Operation V_{OUT} = 5V



Load Current Step Response



PIN FUNCTIONS

GND (Pin 1): Chip Ground Pin.

SYNC/MODE (Pin 2): Synchronization Input and Burst Mode Operation Enable/Disable. If this pin is left open or pulled higher than 2V, Burst Mode operation will be enabled at light load and the typical threshold of entering Burst Mode operation is one third of current limit. If this pin is grounded or the synchronization pulse is present with a frequency greater than 20kHz then Burst Mode operation is disabled and the LTC3824 goes into pulse skipping at light loads. To synchronize the LTC3824, the duty cycle of the synchronizing pulse can range from 10% to 70% and the synchronizing frequency has to be higher than the programmed frequency.

R_{SET} (Pin 3): A resistor from R_{SET} to ground sets the LTC3824 switching frequency.

V_C (Pin 4): The Output of the voltage error amplifier gm and the control signal of the current mode PWM control loop. Switching starts at 0.7V, and higher V_C corresponds to higher inductor current. When V_C is pulled below 25mV, the LTC3824 goes into micropower shutdown.

V_{FB} (Pin 5): Error Amplifier Inverting Input. A resistor divider to this pin sets the output voltage. When V_{FB} is less than 0.5V, the switching frequency will fold back to 50kHz to reduce the minimum on-cycle.

SS (Pin 6): Soft-Start Pin. A capacitor on this pin sets the output ramp-up rate. The typical time for SS to reach the programmed level is (C • 0.8V)/7µA.

SENSE (Pin 7): Current Sense Input Pin. A sense resistor, R_S, from V_{IN} to SENSE sets the current limit to 100mV/R_S.

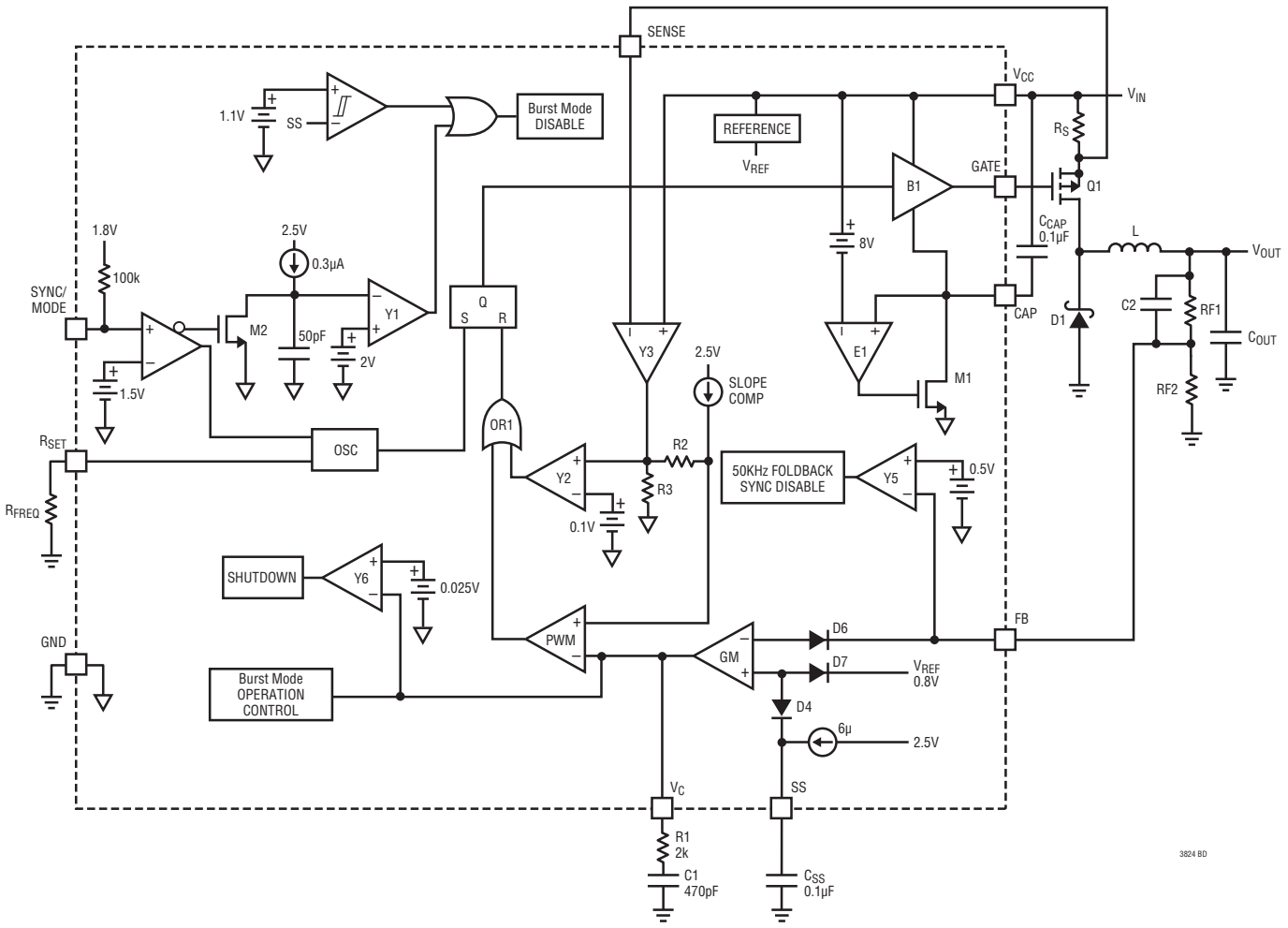
V_{CC} (Pin 8): Chip Power Supply. Power supply bypassing is required.

GATE (Pin 9): Gate Drive for The External P-channel MOSFET. Typical peak drive current is 2.5A and the drive voltage is clamped to 8V when V_{CC} is higher than 9V.

CAP (Pin 10): A Low ESR Capacitor of at Least 0.1µF is required from this pin to V_{CC} to bypass the internal regulator for biasing the gate driver circuitry.

Exposed Pad (Pin 11): GND. Must be soldered to PCB with expanded metal trace for rated thermal performance.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

Operation

The LTC3824 is a constant frequency current mode buck controller with programmable switching frequency up to 600kHz.

Referring to the Block Diagram, the LTC3824's basic functions include a transconductance amplifier gm to regulate the output voltage and control the current mode PWM current loop, the necessary logic to control the PWM switching cycles, a high speed gate driver to drive an external high power P-channel MOSFET and a voltage regulator to bias the gate driver circuit.

In normal operation each switching cycle starts with switch turn-on and the inductor current is sampled through the current sense resistor. This current is amplified and then compared to the error amplifier output V_C to turn the switch off. Voltage loop regulates the output voltage to the programmed level through the output resistor divider and the error amplifier. Amplifier E1 regulates the gate drive low to approximately 8V below V_{CC} for V_{CC} higher than 9V, and C_{CAP} stabilizes the voltage. Note that when V_{CC} is lower than 9V, gate drive high will be within 0.5V of V_{CC} and gate drive low within 1V of ground.

Important features include shutdown, current limit, soft-start, synchronization and low quiescent current.

APPLICATIONS INFORMATION

Burst Mode Operation

The LTC3824 can be configured for Burst Mode operation to enhance light load efficiency (only 40µA quiescent current) and extend battery run time by leaving the SYNC/MODE pin open or pulling it higher than 2V. In this mode, when output load drops the loop control voltage V_C also drops and when V_C reaches approximately 0.9V at low duty cycle the LTC3824 goes into sleep mode with the switch turned off. During sleep mode the output voltage drops and V_C rises up. When V_C goes up to around 70mV the LTC3824 will turn on the switch and the burst cycle repeats. If the SYNC/MODE pin is grounded the Burst Mode operation will be disabled and the LTC3824 skips cycles at light load.

Oscillation Frequency Setting and Synchronization

The switching frequency of the LTC3824 can be set up to 600kHz by a resistor, R_{FREQ}, from the R_{SET} pin to ground.

For 200kHz, R_{FREQ} = 392k. See the Switching Frequency vs R_{FREQ} graph in the Typical Performance Characteristics section. With a 100ns one-shot timer on-chip, the LTC3824 provides flexibility on the sync pulse width. The sync pulse threshold voltage level is about 1.2V.

Short-Circuit Protection

In normal operation when the output voltage is in regulation, V_{FB} is regulated to 0.8V. If the output is shorted to ground and V_{FB} drops below 0.5V the switching frequency will be reduced to 50kHz to allow the inductor current to discharge and prevent current runaway. Note that synchronization is enabled only when V_{FB} is above 0.5V.

Soft-Start

During soft-start, the voltage on the SS pin (V_{SS}) is the reference voltage that controls the output voltage and the output ramps up following V_{SS}. The effective range of V_{SS} is from 0V to 0.8V. The typical time for the output to reach the programmed level is:

$$t_{SS} = \frac{C_{SS} \bullet 0.8V}{7\mu A}$$

where C_{SS} is the capacitor connected from the SS pin to GND.

Overvoltage Protection

To achieve good output regulation in Burst Mode operation, an overvoltage comparator, OVP, with a threshold adaptive to the V_C voltage is used to monitor the FB voltage. In Burst Mode operation with low V_C voltage, the OVP threshold is approximately 2% above V_{REF} and the V_{REF} is also shifted lower by 2% to contain the output ripple and to keep output regulation constant. As output load increases, OVP threshold increases with V_C voltage to up to 8% above V_{REF}.

Undervoltage Lockout and Shutdown

The undervoltage lockout threshold on V_{CC} is 4V. The switch is allowed to turn on only when V_{CC} is higher than 4V. When the V_C pin is pulled down below 25mV the LTC3824 goes into micropower shutdown mode and only draws 7µA.

Output Voltage Programming

With a 0.8V feedback reference voltage, V_{REF}, the output voltage, V_{OUT}, is programmed by a resistor divider as shown in the Block Diagram.

$$V_{OUT} = 0.8V\ (1+R_{F1}/R_{F2})$$

Current Sense Resistor R_S and Current Limit

The maximum current the LTC3824 can deliver is determined by:

$$I_{OUT(MAX)} = 100mV/R_S - I_{RIPPLE}/2$$

where 100mV is the internal 100mV threshold across V_{CC} and V_{SENSE}, and I_{RIPPLE} is the inductor peak-to-peak ripple current. R_S should be placed very close to the power switch with very short traces. Good kelvin sensing is required for accurate current limit.

APPLICATIONS INFORMATION

Inductor Selection

The maximum inductor current is determined by :

$$I_{L(MAX)} = I_{OUT(MAX)} + \frac{I_{RIPPLE}}{2}$$

$$\text{where } I_{RIPPLE} = \frac{(V_{IN} - V_{OUT}) \bullet D}{f \bullet L}$$

$$\text{and Duty Cycle } D = \frac{V_{OUT} + V_D}{V_{IN} + V_D}$$

V_D is the catch diode D1 forward voltage and f is the switching frequency.

A small inductance will result in larger ripple current, output ripple voltage and also larger inductor core loss. An empirical starting point for the inductor ripple current is about 40% of maximum DC current.

$$L = \frac{(V_{IN} - V_{OUT}) \bullet D}{f \bullet 0.4 \bullet I_{OUT(MAX)}}$$

The saturation current level of the inductor should be sufficiently larger than $I_{L(MAX)}$.

Power MOSFET Selection

Important parameters for the power MOSFET include the drain-to-source breakdown voltage (BV_{DSS}), the threshold voltage ($V_{GS(TH)}$), the on-resistance ($R_{DS(ON)}$) versus gate-to-source voltage, the gate-to-source and gate-to-drain charges (Q_{GS} and Q_{GD}, respectively), the maximum drain current ($I_{D(MAX)}$) and the MOSFET's thermal resistance ($R_{TH(JC)}$) and $R_{TH(JA)}$.

The gate drive voltage is set by the 8V internal regulator. Consequently, at least 10V V_{GS} rated MOSFETs are required in high voltage applications.

In order to calculate the junction temperature of the power MOSFET, the power dissipated by the device must be known. This power dissipation is a function of the duty cycle, the load current and the junction temperature itself (due to the positive temperature coefficient of $R_{DS(ON)}$). The power dissipation calculation should be based on the worst-cast specifications for $V_{SENSE(MAX)}$, the required load current at maximum duty cycle, the voltage and temperature ranges, and the $R_{DS(ON)}$ of the MOSFET listed in the data sheet.

The power dissipated by the MOSFET when the LTC3824 is in continuous mode is given by :

$$P_{MOSFET} = \frac{V_{OUT+} V_D}{V_{IN} + V_D} (I_{OUT})^2 (1+\delta) R_{DS(ON)} + K(V_{IN})^2 (I_{OUT})(C_{RSS})(f)$$

The first term in the equation represents the I^2R losses in the device and the second term is the switching losses. K (estimated as 1.7) is an empirical factor inversely related to the gate drive current and has the unit of 1/Amps. The δ term accounts for the temperature coefficient of the $R_{DS(ON)}$ of the MOSFET, which is typically 0.4%/°C. C_{RSS} is the MOSFET reverse transfer capacitance. Figure 1 illustrates the variation of normalized $R_{DS(ON)}$ over temperature for a typical power MOSFET.

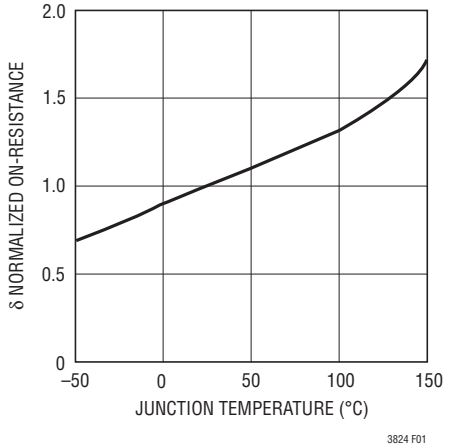


Figure 1. Normalized $R_{DS(ON)}$ vs Temperature

From a known power dissipated in the power MOSFET, its junction temperature can be obtained using the following formula:

$$T_J = T_A + P_{MOSFET} \bullet R_{TH(JA)}$$

The $R_{TH(JA)}$ to be used in this equation normally includes the $R_{TH(JC)}$ for the device plus the thermal resistance from the case to the ambient temperature ($R_{TH(CA)}$). This value of T_J can then be compared to the original assumed value used in the calculation.

Output Diode Selection

The catch diode carries load current during the switch off-time. The average diode current is therefore dependent

APPLICATIONS INFORMATION

on the P-channel switch duty cycle. At high input voltages the diode conducts most of the time. As V_{IN} approaches V_{OUT} the diode conducts only a small fraction of the time. The worst condition for the diode is when the output is shorted to ground. Under this condition the diode must safely handle the maximum current at close to 100% of the time. Therefore, the diode must be carefully chosen to meet the worst case voltage and current requirements.

Under normal conditions, the average current conducted by the diode is:

$$I_D = I_{OUT} \bullet (1 - D)$$

A fast switching Schottky diode must be used to optimize efficiency.

C_{IN} and C_{OUT} Selection

A low ESR input capacitor, C_{IN}, sized for the maximum RMS P-channel switch current is required to prevent large input voltage transients. The maximum RMS capacitor current is given by:

$$I_{RMS} = I_{OUT(MAX)} \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life which makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design.

The selection of C_{OUT} is determined by the effective series resistance (ESR) that is required to minimize voltage ripple and load step transients as well as the amount of bulk capacitance that is necessary to ensure that the control loop is stable.

The output ripple, ΔV_{OUT} , is determined by:

$$\Delta V_{OUT} \leq \Delta I_L \left(ESR + \frac{1}{8fC_{OUT}} \right)$$

The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Special polymer capacitors offer very low ESR but have lower capacitance density than other types. Tantalum capacitors have the highest capacitance density but it is important to only use types that have been surge tested for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR, but can be used in cost-sensitive applications provided that consideration is given to ripple current ratings and long-term reliability. Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient and audible noise.

Efficiency Considerations

The efficiency of a switching regulator is equal to the output power divided by the input power. Percentage efficiency can be expressed as:

$$\% \text{ Efficiency} = 100\% - (L1 + L2 + L3 + ...)$$

where L1, L2, L3...are the individual loss components as a percentage of the input power. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Although all dissipative elements in the circuit produce losses, the following are the main sources:

1. The supply current into V_{CC}. The V_{CC} current is the sum of the DC supply current and the MOSFET driver and control currents. The DC supply current into the V_{CC} pin is typically about 1mA. The driver current results from switching the gate capacitance of the power MOSFET; this current is typically much larger than the DC current. Each time the MOSFET is switched on and off, a packet of gate charge Q_G is transferred from the CAP pin to V_{CC} throughout the external bypass capacitor, C_{CAP}. The resulting dQ/dt is a current that must be supplied to the capacitor by the internal regulator.

$$I_Q = 1mA + f \bullet Q_G$$

$$P_{IC} = V_{IN} \bullet I_Q$$

APPLICATIONS INFORMATION

2. Power MOSFET switching and condution losses:

$$P_{MOSFET} = \frac{V_{OUT} + V_D}{V_{IN} + V_D}(I_{OUT})^2(1+\delta)R_{DS(ON)} + K(V_{IN})^2(I_{OUT})(C_{RSS})(f)$$

3. The I^2R losses of the current sense resistor:

$$P_{(SENSE\ R)} = (I_{OUT})^2 \bullet R \bullet D$$

where D is the duty cycle

4. The inductor loss due to winding resistance:

$$P_{(WINDING)} = (I_{OUT})^2 \bullet R_W$$

5. Loss of the catch diode:

$$P_{(DIODE)} = I_{OUT} \bullet V_D \bullet (1–D)$$

6. Other losses, including C_{IN} and C_{OUT} ESR dissipation and inductor core losses, generally account for less than 2% of total losses.

PCB Layout Considerations

To achieve best performance from a LTC3824 circuit, the PC board layout must be carefully designed. For lower power applications, a 2-layer PC board is sufficient. However, at higher power levels, a multiple layer PC board is recommended. Using a solid ground plane under the circuit is the easiest way to ensure that switching noise does not affect the operation.

In order to help dissipate the power from the MOSFET and diode, keep the ground plane on the layers closest to the layers where power components are mounted. Use power planes for the MOSFET and diode in order to improve the spreading of heat from these components into the PCB.

For best electrical performance the LTC3824 circuit should be laid out as following:

Place all power components in a tight area. This will minimize the size of high current loops. Orient the input and output capacitors and current sense resistor in a way that minimizes the distance between the pads connected to ground plane.

Place the LTC3824 and associated components tightly together and next to the section with power components.

Use a local via to ground plane for all pads that connect to ground. Use multiple vias for power components.

Connect the current sense input directly to the current sense resistor pad. V_{CC} and SENSE are the inputs of the internal current sense amplifier and should be connected as close to the sense resistor pads as possible. A 100pF capacitor is required across the V_{CC} and sense pins for noise filtering and should be placed as close to the pins as possible.

Design Example

As an example, the LTC3824 is designed for an automotive 5V power supply with the following specifications:

Maximum I_{OUT} = 2A, typical V_{IN} = 6V to 18V and can reach 60V briefly during load dump condition, and operating switching frequency = 400kHz.

For f = 400kHz, R_{SET} is chosen to be 180k.

Allow inductor ripple current to be 0.8A (40% of the maximum output current) at V_{IN} = 18V,

$$L = \frac{(18V - 5V)5V}{(400kHz \bullet 0.8A)18V} = 12\mu H$$

C_{OUT} will be selected based on the ESR that is required to satisfy the output voltage ripple requirement and the bulk capacitance needed for loop stability. For this design a 220µF tantalum capacitor is used.

For worse-case conditions C_{IN} should be rated for at least 1A ripple current (half of the maximum output current). A 47µF tantalum capacitor is adequate.

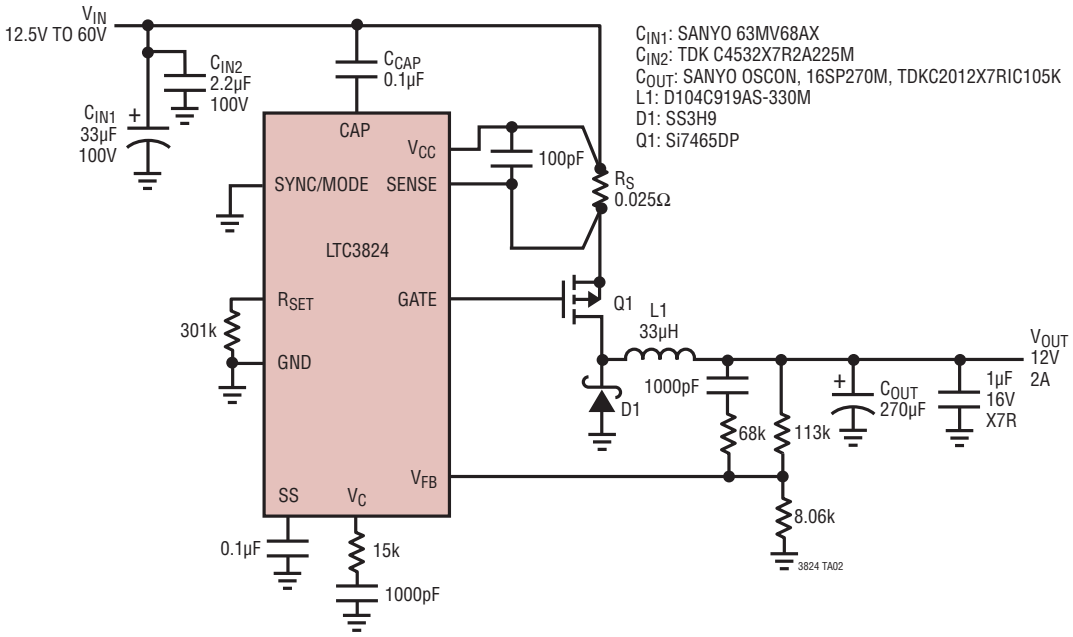
A current limit of 3.3A is selected and R_{SENSE} can be calculated by :

$$R_{SENSE} = \frac{100mV}{3.3A} = 0.03\Omega$$

and a 25mΩ resistor can be used.

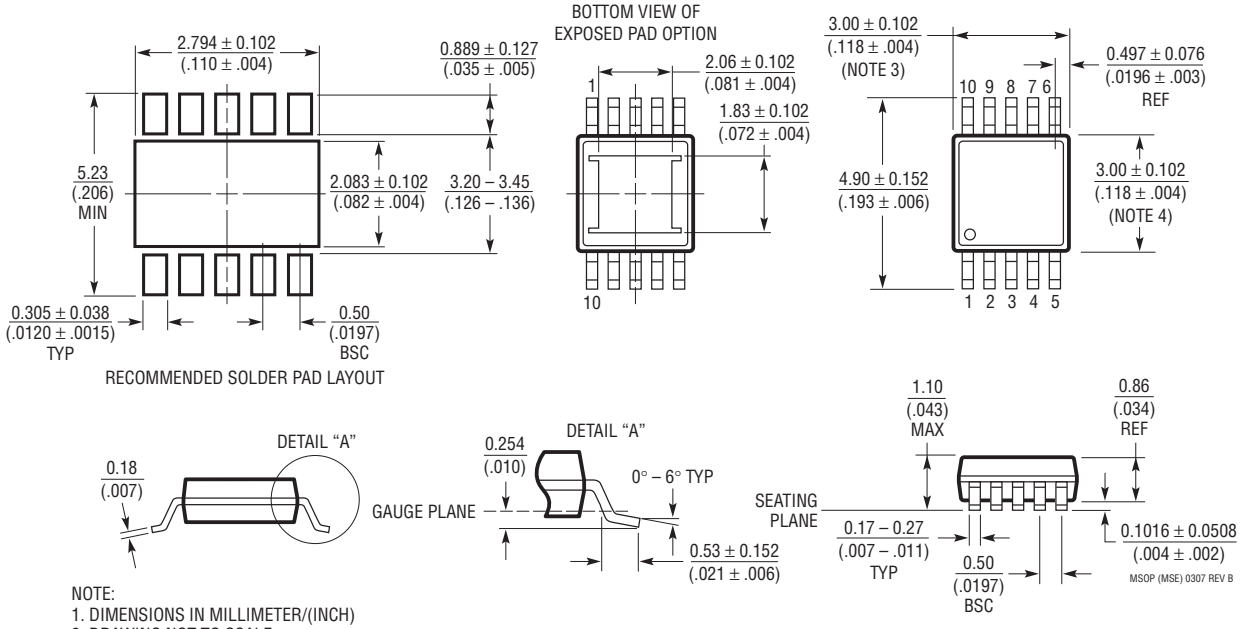
TYPICAL APPLICATION

12V 2A Buck Converter



PACKAGE DESCRIPTION

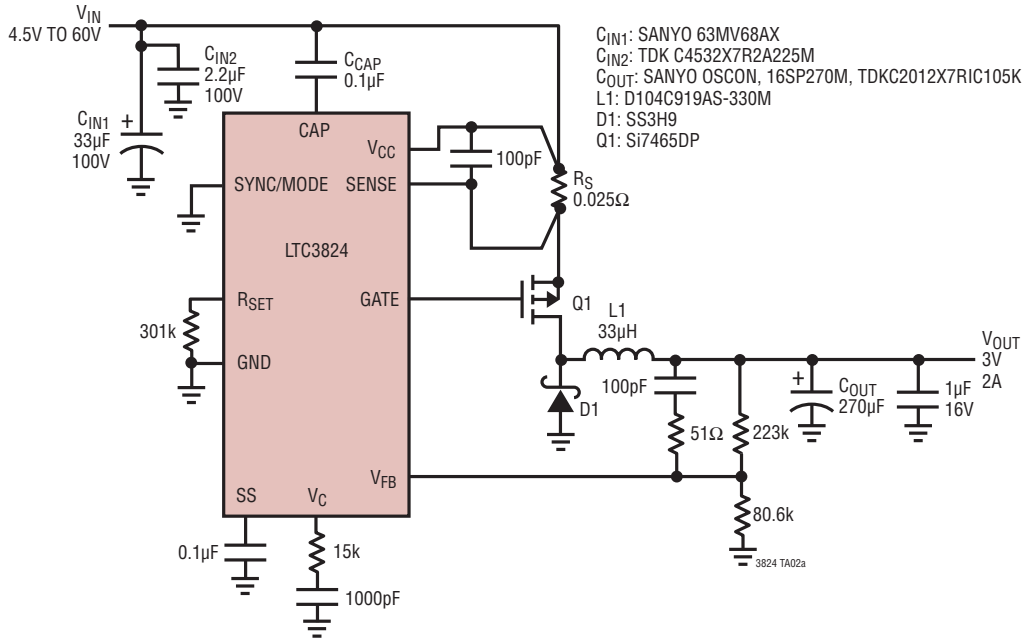
MSE Package
10-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1664 Rev B)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

TYPICAL APPLICATION

3V 2A Buck Converter



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1624	36V Current Mode Controller	3.5V ≤ V_{IN} ≤ 36V; N-Channel MOSFET; S8
LT1976	60V Monolithic Regulator	3.3V ≤ V_{IN} ≤ 60V; 1.5A Peak Switch Current
LT3724	60V Current Mode DC/DC Controller	4V ≤ V_{IN} ≤ 60V; 1.223V ≤ V_{OUT} ≤ 36V; 200kHz
LTC3703/LTC3703-5	100V and 60V Synchronous Controllers	High Efficiency; Buck or BOOST Topology
LT3800	60V Current Mode Step-Down Controller, Synchronous	4V ≤ V_{IN} ≤ 60V; 0.8V ≤ V_{OUT} ≤ 36V; 16-Lead TSSOP
LT3844	60V Current Mode Step-Down Controller	Synchronizable, Adjustable Frequency; 4V ≤ V_{IN} ≤ 60V