Silicon PNP Power Transistors 2SB1419

DESCRIPTION

·With TO-3PL package
·Wide area of safe operation
·Low collector saturation voltage

APPLICATIONS

·For low frequency and high power amplifier applications

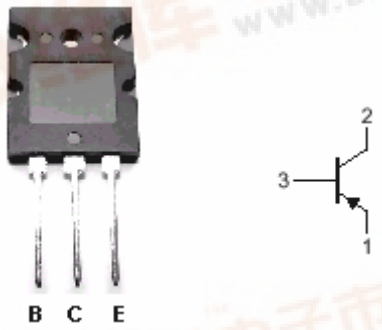

Fig.1 simplified outline (TO-3PL) and symbol

PINNING

PIN	DESCRIPTION
1	Emitter
2	Collector;connected to mounting base
3	Base

Absolute maximum ratings(Ta=25□)

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V_{CBO}	Collector-base voltage	Open emitter	-160	V
V_{CEO}	Collector-emitter voltage	Open base	-160	V
V_{EBO}	Emitter-base voltage	Open collector	-5	V
I_C	Collector current		-12	A
I_{CM}	Collector current-peak		-20	A
P_C	Collector power dissipation	T_C=25□	120	W
T_j	Junction temperature		150	□
T_{stg}	Storage temperature		-55~150	□

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CHARACTERISTICS

Tj=25□ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
$V_{(BR)CEO}$	Collector-emitter breakdown voltage	I_C=-50mA ;I_B=0	-160			V
V_{CEsat}	Collector-emitter saturation voltage	I_C=-8A ;I_B=-0.8A			-1.8	V
V_{BE}	Base-emitter voltage	I_C=-8A ; V_{CE}=-5V			-1.8	V
I_{CBO}	Collector cut-off current	V_{CB}=-160V; I_E=0			-50	μA
I_{EBO}	Emitter cut-off current	V_{EB}=-5V; I_C=0			-50	μA
h_{FE-1}	DC current gain	I_C=-20mA ; V_{CE}=-5V	20			
h_{FE-2}	DC current gain	I_C=-1A ; V_{CE}=-5V	60		200	
h_{FE-3}	DC current gain	I_C=-8A ; V_{CE}=-5V	20			

◆ **h_{FE-2} classifications**

Q	S	P
60-120	80-160	100-200

PACKAGE OUTLINE

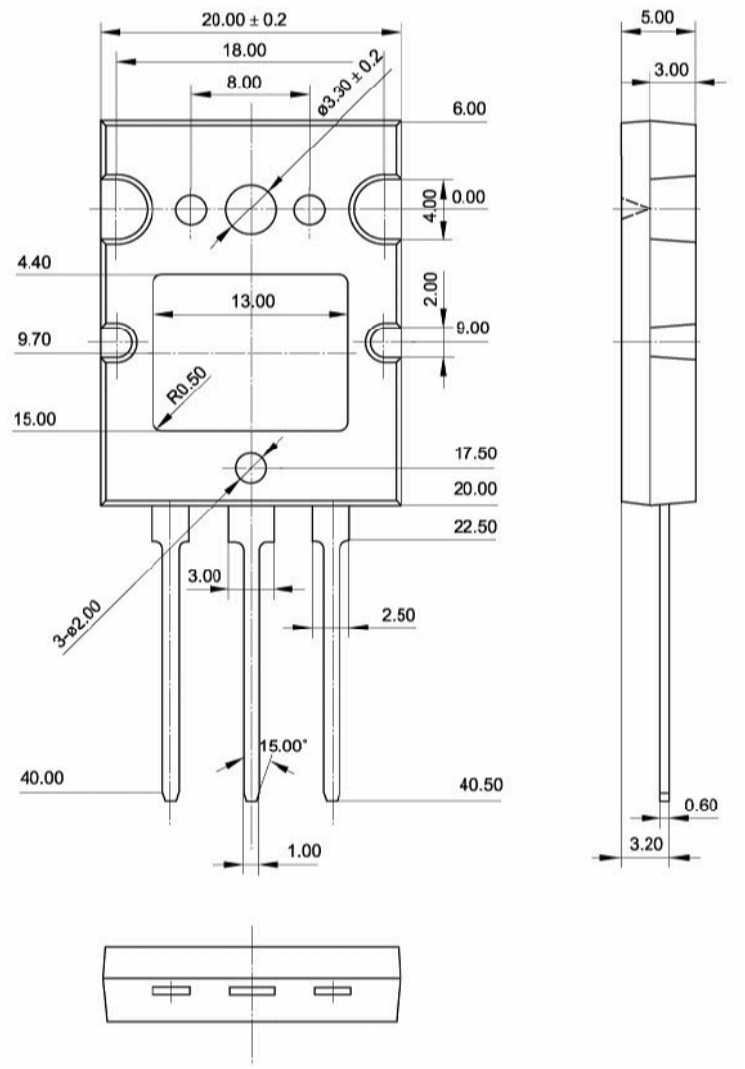

Fig.2 Outline dimensions (unindicated tolerance:±0.50 mm)