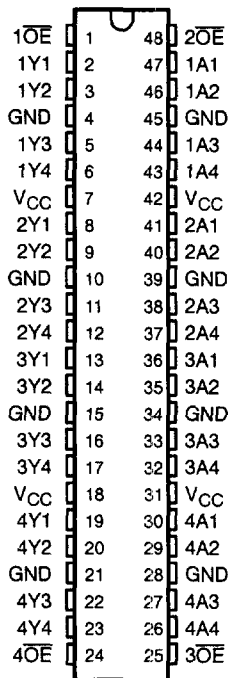


54AC16240, 74AC16240 16-BIT BUS DRIVERS WITH 3-STATE OUTPUTS

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- **Members of the Texas Instruments Widebus™ Family**
- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) Package Using 25-mil Center-to-Center Pin Spacings and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Pin Spacings**

54AC16240 . . . WD PACKAGE
74AC16240 . . . DL PACKAGE
(TOP VIEW)



description

The 'AC16240 are 16-bit buffers and line drivers designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

They can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. These devices provide inverting outputs and symmetrical active-low output-enable (\overline{OE}) inputs.

The 74AC16240 is packaged in TI's shrink small-outline package, which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed circuit board area.

The 54AC16240 is characterized for operation over the full military temperature range of -55°C to 125°C .

The 74AC16240 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
(each 4-bit buffer)

INPUTS		OUTPUT
\overline{OE}	A	Y
L	H	L
L	L	H
H	X	Z

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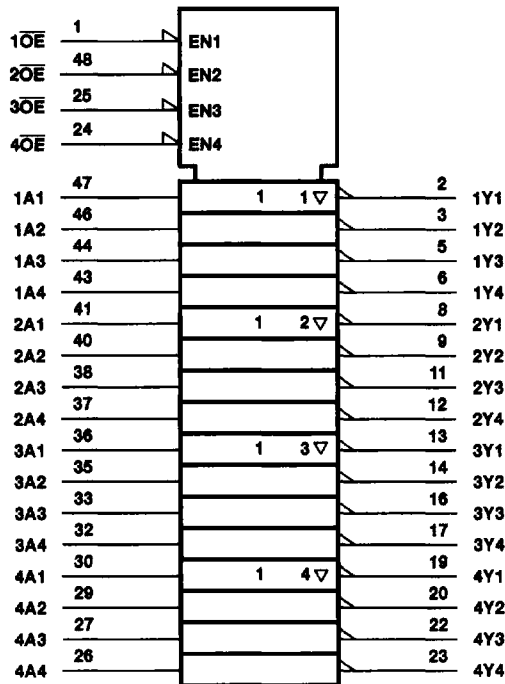


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54AC16240, 74AC16240
16-BIT BUS DRIVERS
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logic symbol†

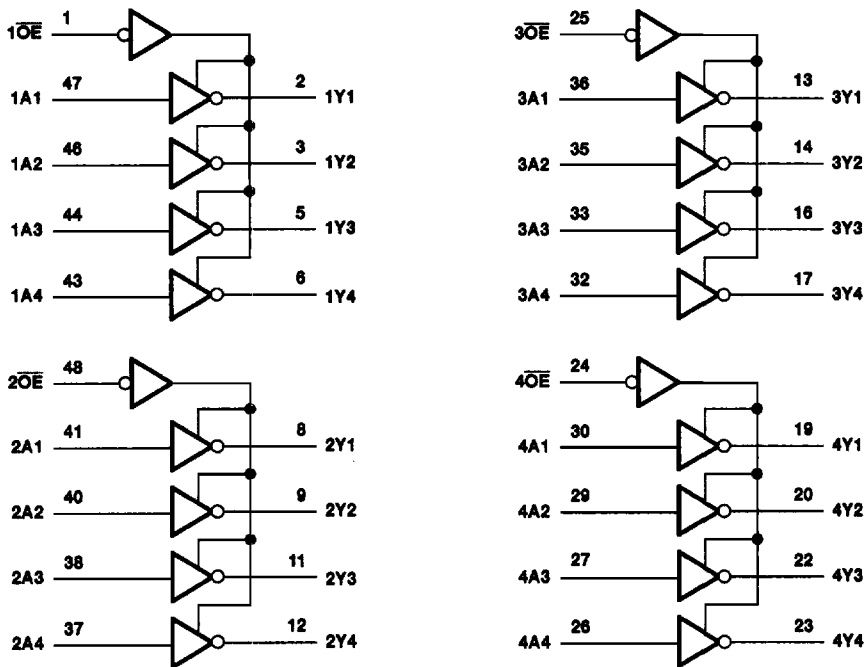


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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16-BIT BUS DRIVERS
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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND	± 400 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air)(see Note 2): DL package	1.2 W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

54AC16240, 74AC16240 16-BIT BUS DRIVERS WITH 3-STATE OUTPUTS

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recommended operating conditions (see Note 3)

		54AC16240			74AC16240			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	3	5	5.5	3	5	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 3 V	2.1		2.1			V
		V _{CC} = 4.5 V	3.15		3.15			
		V _{CC} = 5.5 V	3.85		3.85			
V _{IL}	Low-level input voltage	V _{CC} = 3 V			0.9			V
		V _{CC} = 4.5 V			1.35			
		V _{CC} = 5.5 V			1.65			
V _I	Input voltage	0		V _{CC}	0		V _{CC}	V
V _O	Output voltage	0		V _{CC}	0		V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 3 V			-4			mA
		V _{CC} = 4.5 V			-24			
		V _{CC} = 5.5 V			-24			
I _{OL}	Low-level output current	V _{CC} = 3 V			12			mA
		V _{CC} = 4.5 V			24			
		V _{CC} = 5.5 V			24			
Δt/Δv	Input transition rise or fall rate	0		10	0		10	ns/V
T _A	Operating free-air temperature	-55		125	-40		85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			54AC16240		74AC16240		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 μA	3 V	2.9			2.9		2.9	V	
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I _{OH} = -4 mA	3 V	2.58			2.48		2.48		
		4.5 V	3.94			3.8		3.8		
		5.5 V	4.94			4.8		4.8		
I _{OH} = -75 mA†	5.5 V				3.85		3.85			
V _{OL}	I _{OL} = 50 μA	3 V				0.1		0.1	V	
		4.5 V				0.1		0.1		
		5.5 V				0.1		0.1		
	I _{OL} = 12 mA	3 V			0.36		0.44	0.44		
		4.5 V			0.36		0.44	0.44		
		5.5 V			0.36		0.44	0.44		
I _{OL} = 75 mA†	5.5 V				1.65		1.65			
I _I	V _I = V _{CC} or GND	5.5 V			±0.1		±1	±1	μA	
I _{OZ}	V _O = V _{CC} or GND	5.5 V			±0.5		±5	±5	μA	
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			8		80	80	μA	
C _i	V _I = V _{CC} or GND	5 V			4.5				pF	
C _o	V _O = V _{CC} or GND	5 V			12				pF	

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



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switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 3.3 V \pm 0.3 V$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ C$			54AC16240		74AC16240		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1.8	5.4	7.5	1.8	8.3	1.8	8.3	ns
t_{PHL}			2.5	7	9.3	2.5	10.2	2.5	10.2	
t_{PZH}	\overline{OE}	Y	2.1	6.1	8.5	2.1	9.5	2.1	9.5	ns
t_{PZL}			2.9	8.4	11.3	2.9	12.6	2.9	12.6	
t_{PHZ}	\overline{OE}	Y	4.3	6.2	8.3	4.3	8.7	4.3	8.7	ns
t_{PLZ}			3.6	6	7.8	3.6	8.4	3.6	8.4	

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5 V \pm 0.5 V$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ C$			54AC16240		74AC16240		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1.3	3.3	5.3	1.3	5.8	1.3	5.8	ns
t_{PHL}			1.9	4.3	6.5	1.9	7.1	1.9	7.1	
t_{PZH}	\overline{OE}	Y	1.6	3.8	5.9	1.6	6.6	1.6	6.6	ns
t_{PZL}			3.2	4.7	7.2	3.2	8.1	3.2	8.1	
t_{PHZ}	\overline{OE}	Y	4.2	6	7.7	4.2	8.1	4.2	8.1	ns
t_{PLZ}			3.4	5.1	6.9	3.4	7.3	3.4	7.3	

operating characteristics, $V_{CC} = 5 V$, $T_A = 25^\circ C$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per latch	Outputs enabled	42	pF
		Outputs disabled	6	

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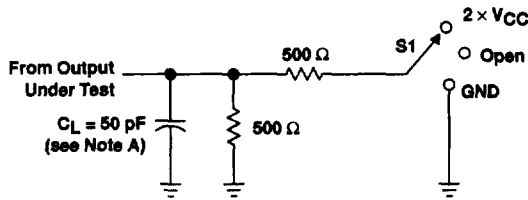


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16-BIT BUS DRIVERS
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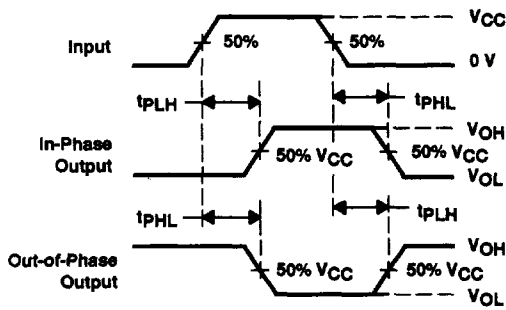
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PARAMETER MEASUREMENT INFORMATION

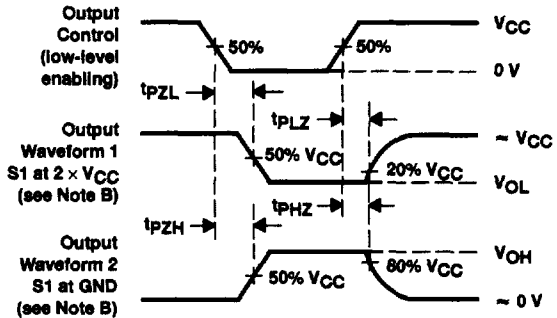


LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 3 \text{ ns}$, $t_f = 3 \text{ ns}$.
 D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms