National Semiconductor

MICROCIRCUIT DATA SHEET

CN54F38-X REV 0A0

Original Creation Date: 10/21/98
Last Update Date: 11/12/98
Last Major Revision Date: 10/21/98

QUAD 2-INPUT NAND BUFFER (OPEN COLLECTOR)

General Description

The device contains four independent gates, each of which performs the logic NAND function. The open-collector outputs require external pull-up resistors for proper logical operation.

Industry Part Number

54F38

NS Part Numbers

54F38DC

Prime Die

M038

Processing

(blank)

Quality Conformance Inspection

(blank)

Subgrp	Description	Temp (^{o}C)
1	Static tests at	+25
2	Static tests at	+70
3	Static tests at	0
4	Dynamic tests at	+25
5	Dynamic tests at	+70
6	Dynamic tests at	0
7	Functional tests at	+25
8A	Functional tests at	+70
8B	Functional tests at	0
9	Switching tests at	+25
10	Switching tests at	+70
11	Switching tests at	0

(Absolute Maximum Ratings)

(Note 1)

Storage Temperature	-65 C to +150 C
Ambient Temperature under Bias	-55 C to +125 C
Junction Temperature under Bias	-55 C to +175 C
Vcc Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0mA
Voltage Applied to Output in HIGH State (with Vcc=0V)	
Standard Output	-0.5V to Vcc
TRI-STATE Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated Iol(mA)
ESD Last Passing Voltage (Min)	4000V

Note 1: Absolute Maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.
Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	0 C to +70 C
Supply Voltage	+4.5V to +5.5V

Electrical Characteristics

DC PARAMETER

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: VCC 4.5V to 5.5V, Temp range: 0C to +70C

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
IIH	Input High Current	VCC=5.5V, VM=2.7V, VINH=5.5V, VINL=0.0V	1, 2	INPUTS		5.0	uA	1, 2, 3
IBVI	Input High Current	VCC=5.5V, VM=7.0V, VINH=5.5V, VINL=0.0V	1, 2	INPUTS		7.0	uA	1, 2, 3
IIL	Input LOW Current	VCC=5.5V, VM=0.5V, VINH=5.5V, VINL=0.0V	1, 2	INPUTS		-1.2	mA	1, 2, 3
IOH	Open Collector Output	VCC=4.5V, VM=4.5V, VIL=0.8V, VINH=5.5V	1, 2	OUTPUTS		250	uA	1, 2, 3
VOLB	Output LOW Voltage	VCC=4.5V, VIL=0.8V, VIH=2.0V, IOLB=64mA, VINH=5.5V	1, 2	OUTPUTS		0.55	V	1, 2, 3
VCD	Input Clamp Diode Voltage	VCC=4.5V, IM=-18mA, VINH=5.5V	1, 2	INPUTS		-1.2	V	1, 2, 3
VID	Input Leakage Test	VCC=0V, IID=1.9uA, All other pins grounded	1, 2	INPUTS	4.75		V	1, 2, 3
IOD	Output Leakage Circuit Current	VCC=0V, VIOD=150mV, All other pins grounded	1, 2	OUTPUTS		4.75	uA	1, 2, 3
VIH	Input HIGH Voltage	Recognized as a HIGH signal	4	INPUTS	2.0		V	1, 2, 3
VIL	Input LOW Voltage	Recognized as a LOW signal	4	INPUTS		0.8	V	1, 2, 3
ICCH	Supply Current	VCC=5.5V, VINL=0.0V, VINH=5.5V	1, 2	VCC		7.0	mA	1, 2, 3
ICCL	Supply Current	VCC=5.5V, VINL=0.0V, VINH=5.5V	1, 2	VCC		30.0	mA	1, 2, 3

AC PARAMETER

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: CL=50pf, RL=500 OHMS, TR=2.5ns, TF=2.5ns

tpLH	Propagation Delay	VCC=5.0V @25C, VCC=4.5V & 5.5V @ 0C/ +70C	1, 2	An/Bn to $\overline{On}$	6.5	12.5	ns	9
			1, 2	An/Bn to $\overline{On}$	6.5	13.0	ns	10, 11
tpHL	Propagation Delay	VCC=5.0V @25C, VCC=4.5V & 5.5V @ 0C/ +70C	1, 2	An/Bn to $\overline{On}$	1.0	5.0	ns	9
			1, 2	An/Bn to $\overline{On}$	1.0	5.5	ns	10, 11

Note 1: Screen tested 100% on each device at +75C temperature only, subgroups 2, 8A & 10.
Note 2: Sample tested (Method 5005, Table 1) on each MFG. lot at +75C temperature only, subgroups 2, 8A & 10.
Note 3: Guaranteed, but not tested.
Note 4: Guaranteed by applying specific input condition and testing VOLB & IOH.

Revision History

Rev	ECN #	Rel Date	Originator	Changes
0A0	M0003057	11/12/98	Donald B. Miller	Initial MDS Release