



54LS298/DM74LS298 Quad 2-Port Register Multiplexer with Storage

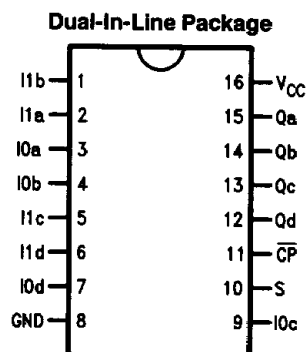
General Description

The 'LS298 is a quad 2-port register. It is the logical equivalent of a quad 2-input multiplexer followed by a quad 4-bit edge-triggered register. A Common Select input selects between two 4-bit input ports (data sources). The selected data is transferred to the output register synchronous with the HIGH-to-LOW transition of the Clock input.

Features

- Select from two data sources
- Fully edge-triggered operation
- Typical power dissipation of 65 mW

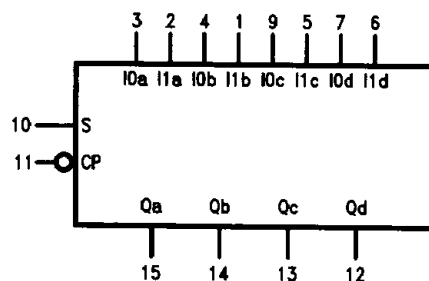
Connection Diagram



TL/F/9826-1

Order Number 54LS298DMQB, 54LS298FMB,
DM74LS298M or DM74LS298N
See NS Package Number J16A, N16E or W16A

Logic Symbol



VCC = Pin 16
GND = Pin 8

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Pin Names	Description
S	Common Select Inputs
$\overline{CP}$	Clock Pulse Input (Active Falling Edge)
I0a, I0d	Source 0 Data Inputs
I1a, I1d	Source 1 Data Inputs
Qa, Qd	Flip-Flip Outputs

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage 7V

Input Voltage 10V

Operating Free Air Temperature Range

54LS -55°C to +125°C

DM74LS 0°C to +70°C

Storage Temperature Range -65°C to +150°C

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	54LS298			DM74LS298			Units
		Min	Nom	Max	Min	Nom	Max	
V _{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High Level Input Voltage	2			2			V
V _{IL}	Low Level Input Voltage			0.7			0.8	V
I _{OH}	High Level Output Current			-0.4			-0.4	mA
I _{OL}	Low Level Output Current			4			8	mA
T _A	Free Air Operating Temperature	-55		125	0		70	°C
t _s (H)	Setup Time HIGH or LOW	25			25			ns
t _s (L)	S to $\overline{CP}$	25			25			ns
t _h (H)	Hold Time HIGH or LOW	0			0			ns
t _h (L)	S to $\overline{CP}$	0			0			ns
t _s (H)	Setup Time HIGH or LOW	15			15			ns
t _s (L)	I _{0x} or I _{1x} to $\overline{CP}$	15			15			ns
t _h (H)	Hold Time HIGH or LOW	5.0			5.0			ns
t _h (L)	I _{0x} or I _{1x} to $\overline{CP}$	5.0			5.0			ns
t _w (H)	$\overline{CP}$ Pulse Width HIGH or LOW	20			20			ns
t _w (L)		20			20			ns

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V _I	Input Clamp Voltage	V _{CC} = Min, I _I = -18 mA			-1.5	V
V _{OH}	High Level Output Voltage	V _{CC} = Min, I _{OH} = Max, V _{IL} = Max	54LS	2.5		V
			DM74	2.7	3.4	
V _{OL}	Low Level Output Voltage	V _{CC} = Min, I _{OL} = Max, V _{IH} = Min	54LS		0.4	V
			DM74		0.35	
		I _{OL} = 4 mA, V _{CC} = Min	DM74		0.25	
I _I	Input Current @ Max Input Voltage	V _{CC} = Max, V _I = 10V			0.1	mA
I _{IH}	High Level Input Current	V _{CC} = Max, V _I = 2.7V			20	μA
I _{IL}	Low Level Input Current	V _{CC} = Max, V _I = 0.4V			-0.4	mA
I _{OS}	Short Circuit Output Current	V _{CC} = Max (Note 2)	54LS	-20	-100	mA
			DM74	-20	-100	
I _{CC}	Supply Current	V _{CC} = Max, I _{0n} , I _{1n} , S = GND, $\overline{CP}$ = 			21	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

at $V_{CC} = +5V$ and $T_A = +25^\circ C$ (See Section 1 for test waveforms and output load)

Symbol	Parameter	$R_L = 2\text{ k}\Omega, C_L = 15\text{ pF}$		Units
		Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output $\overline{CP}$ to Q_n		25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output $\overline{CP}$ to Q_n		25	ns

Functional Description

This device is a high speed quad 2-port register. It selects four bits of data from two sources (ports) under the control of a Common Select input (S). The selected data is transferred to the 4-bit output register synchronous with the HIGH-to-LOW transition of the Clock input ($\overline{CP}$). The 4-bit output register is fully edge-triggered. The Data inputs (I_{nx}) and Select input (S) need be stable only one setup time prior to the HIGH-to-LOW transition of the clock for predictable operation.

Truth Table

Inputs			Output
S	$I0_x$	$I1_x$	Q_x
l	l	X	L
l	h	X	H
h	X	l	L
h	X	h	H

l = LOW Voltage Level one setup time prior to the HIGH-to-LOW clock transition.

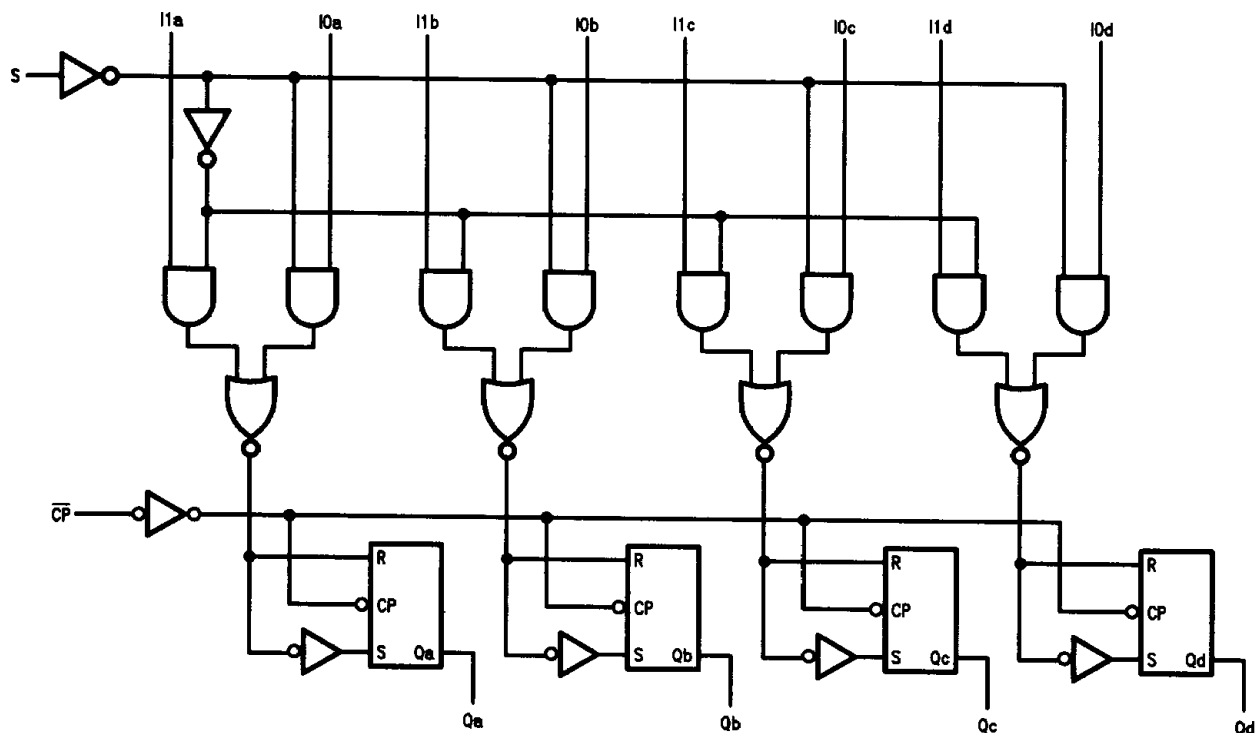
h = HIGH Voltage Level one setup time prior to the HIGH-to-LOW clock transition.

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Logic Diagram



TL/F/9826-3