First-In First-Out (FIFO) 64x4 64x5 Standalone Memory

5/67401 5/67401A 67401B
5/67402 5/67402A 67402B

Features/Benefits

- Choice of 16.7, 15 and 10 MHz shift-out/shift-in rates
- Choice of 4-bit or 5-bit data width
- TTL inputs and outputs
- Readily expandable in the word dimension only
- Structured pin outs. Output pins directly opposite corresponding input pins
- Asynchronous operation
- Pin-compatible with Fairchild's F3341 MOS FIFO and many times as fast

Description

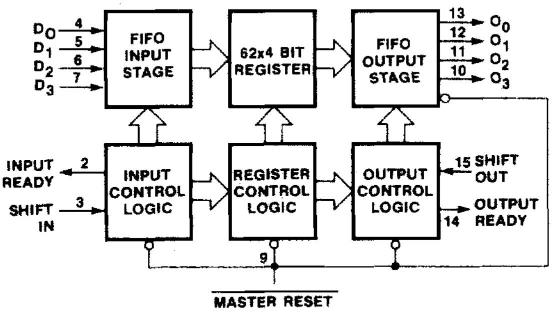
The 5/67401B/2B/1A/2A/1/2 are "fall-through" high speed First-In First-Out (FIFO) memory organized 64 words by 4-bits and 64 words by 5-bits respectively. A 16.7 MHz data rate allows usage in digital video systems; a 15 MHz data rate allows usage in high speed tape or disc controllers and communication buffer applications. Word length is expandable; FIFO depth is not expandable.

Ordering Information

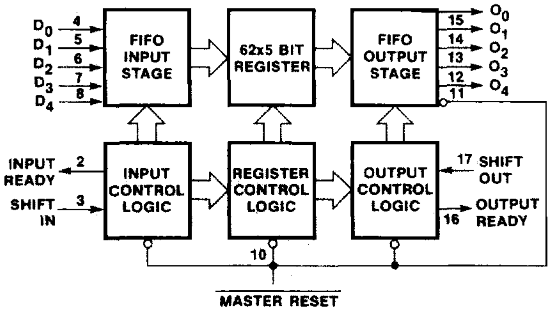
PART NUMBER	PKG	TEMP	DESCRIPTION
57401	J,W(20)(L)	Mil	7 MHz 64x4 FIFO
67401	J,N	Com	10 MHz 64x4 FIFO
57402	J,W(20)(L)	Mil	7MHz 64x5 FIFO
67402	J,N	Com	10 MHz 64x5 FIFO
57401A	J,W(20)(L)	Mil	10 MHz 64x4 FIFO
67401A	J	Com	15 MHz 64x4 FIFO
57402A	J,W(20)(L)	Mil	10 MHz 64x5 FIFO
67402A	J	Com	15 MHz 64x5 FIFO
67401B	J	Com	16.7 MHz 64x4 FIFO
67402B	J	Com	16.7 MHz 64x5 FIFO

Block Diagrams

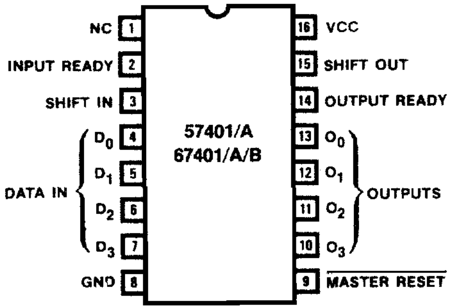
67401/A/B 64x4
57401/A 64x4

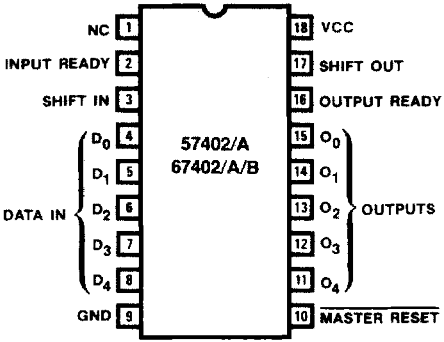


5/67402/A/B 64x5
57402/A 64x5



Pin Configurations





Absolute Maximum Ratings

Supply voltage V_{CC}	-1.5 V to 7 V
Input voltage	-1.5 V to 7 V
Off-state output voltage	-0.5 V to 5.5 V
Storage temperature	-65° to +150° C

Operating Conditions 67401B/2B

SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
T_A	Operating free-air temperature		0		75	°C
t_{SIH}†	Shift in HIGH time	1	18			ns
t_{SIL}	Shift in LOW time	1	18			ns
t_{IDS}	Input data setup	1	5			ns
t_{IDH}	Input data hold time	1	40			ns
t_{SOH}†	Shift Out HIGH time	5	18			ns
t_{SOL}	Shift Out LOW time	5	18			ns
t_{MRW}	Master Reset pulse	10	35			ns
t_{MRS}	Master Reset to SI	10	35			ns

* Case temperature

Switching Characteristics 67401B/2B

Over Operating Conditions

SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
f_{IN}	Shift in rate	1	16.7			MHz
t_{IRL}	Shift In to input ready LOW	1			35	ns
t_{IRH}	Shift In to input ready HIGH	1			37	ns
f_{OUT}	Shift Out rate	5	16.7			MHz
t_{ORL}†	Shift Out to Output Ready LOW	5			38	ns
t_{ORH}†	Shift Out to Output Ready HIGH	5			44	ns
t_{ODH}	Output Data Hold (previous word)	5	5			ns
t_{ODS}	Output Data Shift (next word)	5			44	ns
t_{PT}	Data throughput or "fall through"	4,8			1.3	µs
t_{MRORL}	Master Reset to OR LOW	10			55	ns
t_{MRIRH}	Master Reset to IR HIGH	10			55	ns
t_{IPH}	Input Ready pulse HIGH	4	15			ns
t_{OPH}	Output Ready pulse HIGH	8	15			ns

†See A/C Test and High Speed Application Note.

Absolute Maximum Ratings

Supply voltage V_{CC}	-0.5 V to 7 V
Input voltage	-1.5 V to 7 V
Off-state output voltage	-0.5 V to 5.5 V
Storage temperature	-65° to +150°C

Operating Conditions 5/67401A/2A

SYMBOL	PARAMETER	FIGURE	MILITARY			COMMERCIAL			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature		-55		*125	0		75	°C
t_{SIH}†	Shift in HIGH time	1	35			23		28†	ns
t_{SIL}	Shift in LOW time	1	35			25			ns
t_{IDS}	Input data setup	1	5			5			ns
t_{IDH}	Input data hold time	1	45			40			ns
t_{SOH}†	Shift Out HIGH time	5	35			23			ns
t_{SOL}	Shift Out LOW time	5	35			25			ns
t_{MRW}	Master Reset pulse	10	40			35			ns
t_{MRS}	Master Reset to SI	10	45			35			ns

*Case temperature

Switching Characteristics 5/67401A/2A

Over Operating Conditions

SYMBOL	PARAMETER	FIGURE	MILITARY			COMMERCIAL			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
f_{IN}	Shift in rate	1	10			15			MHz
t_{IRL}†	Shift In to Input Ready LOW	1			50			40	ns
t_{IRH}†	Shift In to Input Ready HIGH	1			50			40	ns
f_{OUT}	Shift Out rate	5	10			15			MHz
t_{ORL}†	Shift Out to Output Ready LOW	5			65			45	ns
t_{ORH}†	Shift Out to Output Ready HIGH	5			65			50	ns
t_{ODH}	Output Data Hold (previous word)	5	10			10			ns
t_{ODS}	Output Data Shift (next word)	5			60			45	ns
t_{PT}	Data throughput or "fall through"	4, 8			2.2			1.6	µs
t_{MRORL}	Master Reset to OR LOW	10			65			60	ns
t_{MRIRH}	Master Reset to IR HIGH	10			65			60	ns
t_{IPH}	Input Ready pulse HIGH	4	20			20			ns
t_{OPH}	Output Ready pulse HIGH	8	20			20			ns

Absolute Maximum Ratings

Supply voltage V_{CC}	−0.5 V to 7 V
Input voltage	−1.5 V to 7 V
Off-state output voltage	−0.5 V to 5.5 V
Storage temperature	−65° to +150° C

Operating Conditions 5/67401/2

SYMBOL	PARAMETER	FIGURE	MILITARY			COMMERCIAL			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature		−55		*125	0		75	°C
t_{SIH}†	Shift in HIGH time	1	45			35			ns
t_{SIL}	Shift in LOW time	1	45			35			ns
t_{IDS}	Input data setup	1	10			5			ns
t_{IDH}	Input data hold time	1	55			45			ns
t_{SOH}†	Shift Out HIGH time	5	45			35			ns
t_{SOL}	Shift Out LOW time	5	45			35			ns
t_{MRW}	Master Reset pulse†	10	30			35			ns
t_{MRS}	Master Reset to SI	10	45			35			ns

*Case temperature

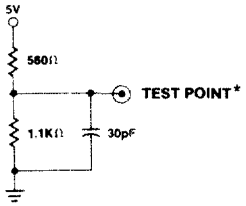
Switching Characteristics 5/67401/2

Over Operating Conditions

SYMBOL	PARAMETER	FIGURE	MILITARY			COMMERCIAL			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
f_{IN}	Shift in rate	1	7			10			MHz
t_{IRL}†	Shift In to input ready LOW	1			60			45	ns
t_{IRH}†	Shift In to input ready HIGH	1			60			45	ns
f_{OUT}	Shift Out rate	5	7			10			MHz
t_{ORL}†	Shift Out to Output Ready LOW	5			65			55	ns
t_{ORH}†	Shift Out to Output Ready HIGH	5			70			60	ns
t_{ODH}	Output Data Hold (previous word)	5	10			10			ns
t_{ODS}	Output Data Shift (next word)	5			65			55	ns
t_{PT}	Data throughput or "fall through"	4,8			4			3	μs
t_{MRORL}	Master Reset to OR LOW	10			65			60	ns
t_{MRIRH}	Master Reset to IR HIGH	10			65			60	ns
t_{IPH}	Input Ready pulse HIGH	4	20			20			ns
t_{OPH}	Output Ready pulse HIGH	8	20			20			ns

†See AC test and high speed application note.

Test Load



* The "TEST POINT" is driven by the output under test, and observed by instrumentation.

Input Pulse 0 to 3 V
Input Rise and Fall Time (10% to 90%)
2 - 5 ns.
Measurements made at 1.5 V

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage						0.8†	V
V_{IH}	High-level input voltage				2†			V
V_{IC}	Input clamp voltage		V_{CC} = MIN	I_I = −18mA			−1.5	V
I_{IL1}	Low-level input current	D_0–D_4, $\overline{MR}$	V_{CC} = MAX	V_I = 0.45V			−0.8	mA
I_{IL2}		SI, SO					−1.6	mA
I_{IH}	High-level input current		V_{CC} = MAX	V_I = 2.4V			50	μA
I_I	Maximum input current		VCC = MAX	V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage		V_{CC} = MIN	I_{OL} = 8mA			0.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN	I_{OH} = −0.9mA	2.4			V
I_{OS}	Output short-circuit current *		V_{CC} = MAX	V_O = 0V	−20		−90	mA
I_{CC}	Supply current		V_{CC} = MAX Inputs low, outputs open.	5/67401			160	
				5/67402			180	
				5/67401A			170	
				5/67402A			190	
				67401B			180	
				67402B			200	

* Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second

†There are absolute voltages with respect to degree GND (PIN 8 or 9) and includes all overshoots due to test equipment.

Functional Description

Data Input

After power up the Master Reset is pulsed low (Fig. 10) to prepare the FIFO to accept data in the first location. When Input Ready (IR) is HIGH the location is ready to accept data from the D_x inputs. Data then present at the data inputs is entered into the first location when the Shift In (SI) is brought HIGH. A SI HIGH signal causes the IR to go LOW. Data remains at the first location until SI is brought LOW. When SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating that more room is available. Simultaneously, data will propagate to the second location and continue shifting until it reaches the output stage or a full location. The first word is present at the outputs before a shift out is applied. If the memory is full, IR will remain LOW.

Data Transfer

Once data is entered into the second cell, the transfer of any full cell to the adjacent (downstream) empty cell is automatic, activated by an on-chip control. Thus data will stack up at the end of the device while empty locations will "bubble" to the front. t_{PT} defines the time required for the first data to travel from input to the output of a previously empty device.

Data Output

Data is read from the O_X outputs. When data is shifted to the output stage, Output Ready (OR) goes HIGH, indicating the presence of valid data. When the OR is HIGH, data may be shifted out by bringing the Shift Out (SO) HIGH. A HIGH signal at SO causes the OR to go LOW. Valid data is maintained while the SO is HIGH. When SO is brought LOW the upstream data, provided that stage has valid data, is shifted to the output stage. When new valid data is shifted to the output stage, OR goes HIGH. If the FIFO is emptied, OR stays LOW, and O_X remains as before, (i.e. data does not change if FIFO is empty).

Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least t_{PT}) or completely empty (Output Ready stays LOW for at least t_{PT}).

AC Test and High Speed App. Notes

Since the FIFO is a very-high-speed device, care must be exercised in the design of the hardware and the timing utilized within the design. The internal shift rate of the FIFO typically exceeds 20 MHz in operation. Device grounding and decoupling is crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitance and/or poor supply decoupling and grounding. We recommend a monolithic ceramic capacitor of 0.1 μF directly between V_{CC} and GND with very short lead length. In addition, care must be exercised in how the timing is set up and how the parameters are measured. For example, since an AND gate function is associated with both the Shift In-Input Ready combination, as well as the Shift Out-Output Ready combination, timing measurements may be misleading, i.e., rising edge of the Shift-In pulse is not recognized until Input-Ready is High. If Input-Ready is not high due to too high a frequency or FIFO being full or affected by Master Reset, the Shift-In activity will be ignored. This will affect the device from a functional standpoint, and will also cause the "effective" timing of Input Data Time (t_{IDH}) and the next activity of Input Ready (t_{IRL}) to be extended relative to Shift-In going High. This same type of problem is also related to t_{IRH}, t_{ORL} and t_{ORH} as related to Shift-Out.

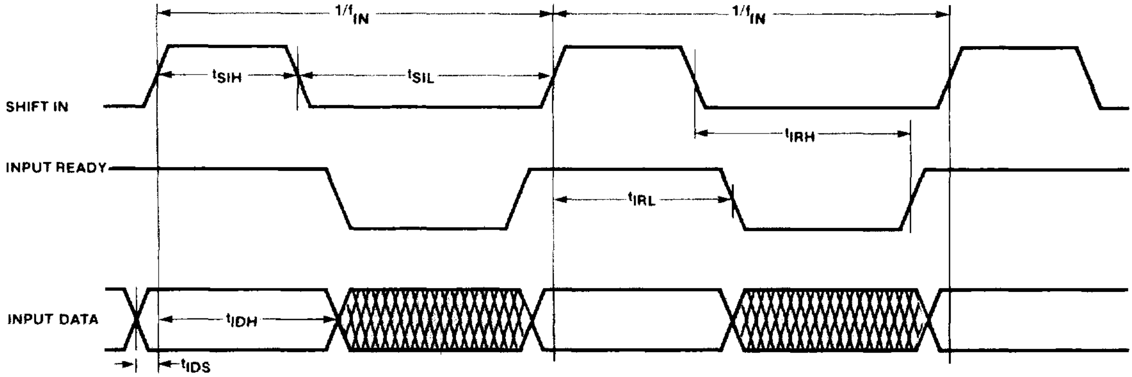


Figure 1. Input Timing

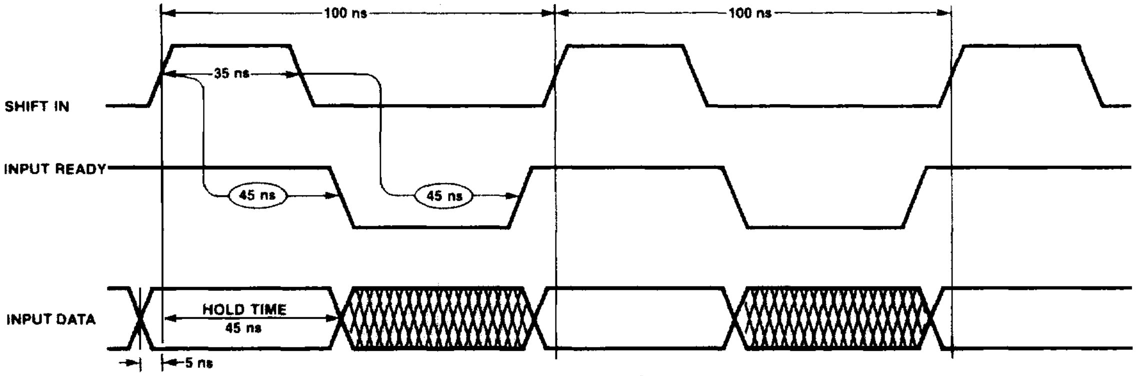


Figure 2. Typical Waveforms for 10 MHz Shift In Data Rate (67401/2)

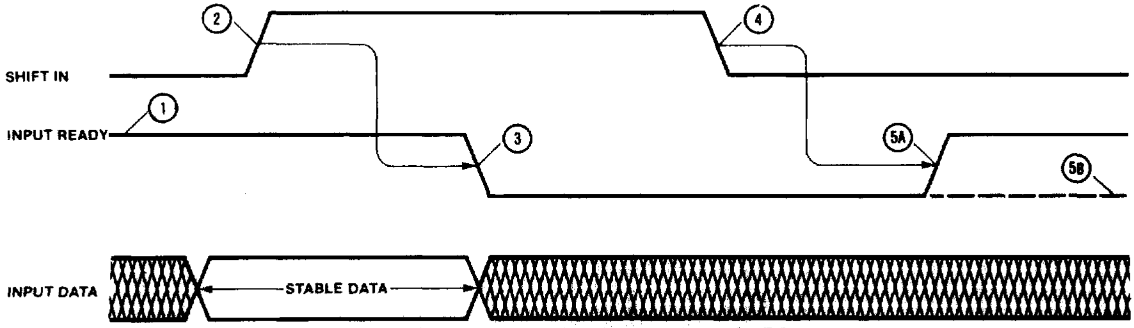


Figure 3. The Mechanism of Shifting Data Into the FIFO

① Input Ready HIGH indicates space is available and a Shift In pulse may be applied.

② Input Data is loaded into the first word.

③ Input Ready goes LOW indicating the first word is full.

④ The Data from the first word is released for "fall-through" to second word.

(5A) The Data from the first word is transferred to second word. The first word is now empty as indicated by Input Ready HIGH.

(5B) If the second word is already full then the data remains at the first word. Since the FIFO is now full Input Ready remains low.

NOTE: Shift In pulses applied while Input Ready is LOW will be ignored. (See Figure 4.)

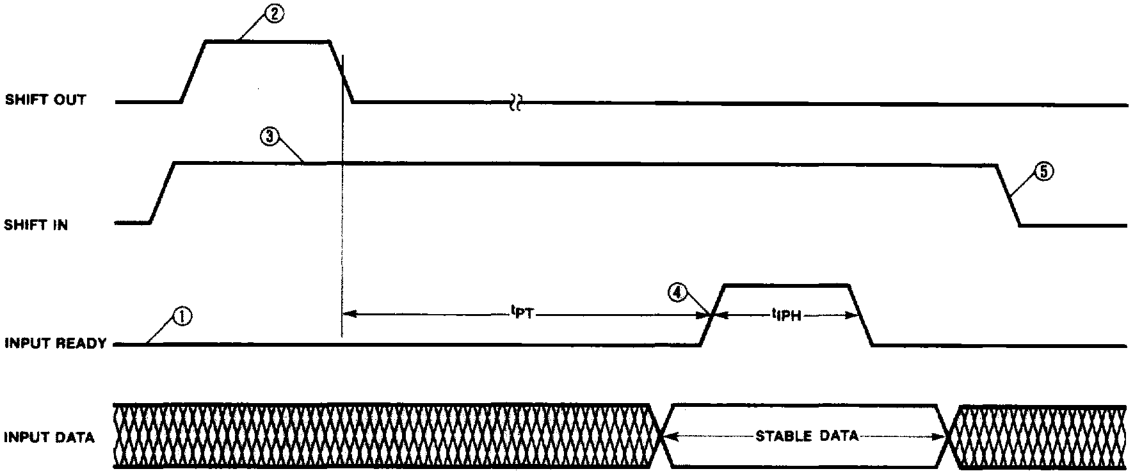


Figure 4. Data is Shifted In Whenever Shift In and Input Ready are Both HIGH

① FIFO is initially full.

② Shift Out pulse is applied. An empty location starts "bubbling" to the front.

③ Shift In is held HIGH.

④ As soon as Input Ready becomes HIGH the Input Data is loaded into the first word.

⑤ The Data from the first word is released for "fall through" to second word.

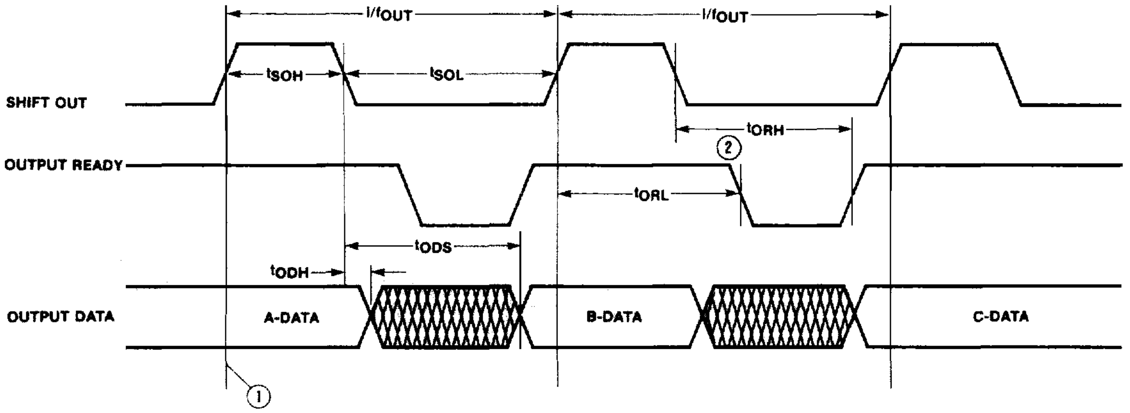


Figure 5. Output Timing

① The diagram assumes that at this time words 63, 62, 61 are loaded with A, B, C Data, respectively.

② Data is shifted out when Shift Out makes a HIGH to LOW transition.

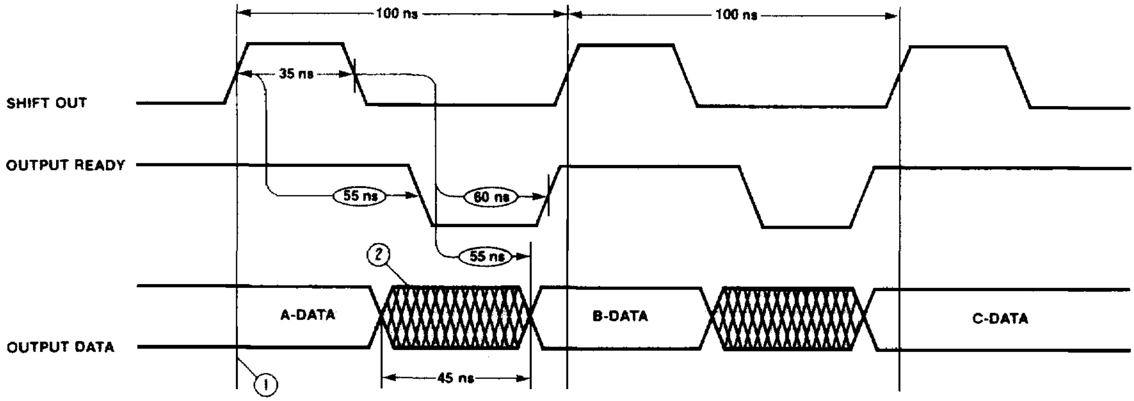


Figure 6. Typical Waveforms for 10 MHz Shift Out Data Rate (67401/2)

① The diagram assumes, that at this time, words 63, 62, 61 are loaded with A, B, C Data, respectively

② Data in the crosshatched region may be A or B Data

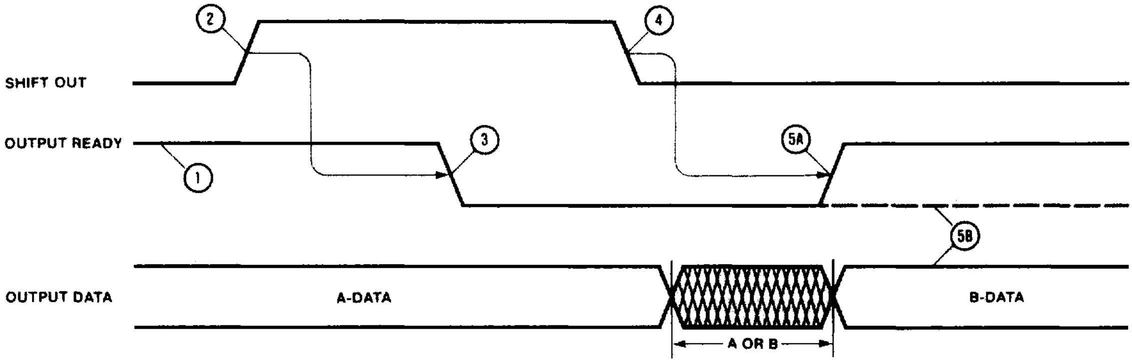


Figure 7. The Mechanism of Shifting Data Out of the FIFO.

① Output Ready HIGH indicates that data is available and a Shift Out pulse may be applied.

② Shift Out goes HIGH causing the next step.

③ Output Ready goes LOW.

④ Contents of word 62 (B-DATA) is released for "fall through" to word 63.

(5A) Output Ready goes HIGH indicating that new data (B) is now available at the FIFO outputs.

(5B) If the FIFO has only one word loaded (A-DATA) then Output Ready stays LOW and the A-DATA remains unchanged at the outputs.

NOTE: Shift Out pulses applied when Output Ready is LOW will be ignored.

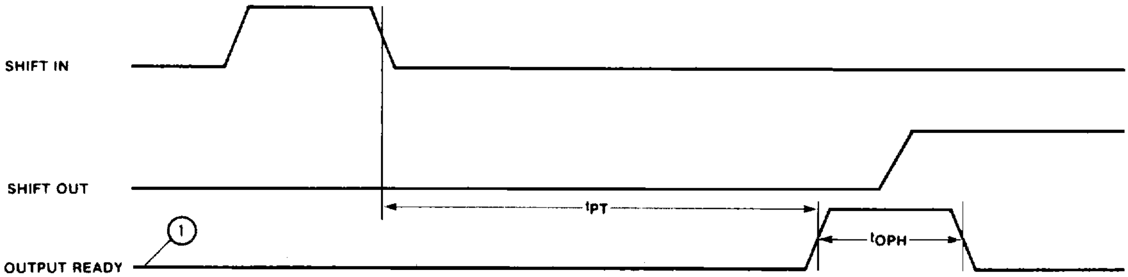


Figure 8. t_{PT} and t_{OPH} Specification

① FIFO initially empty.

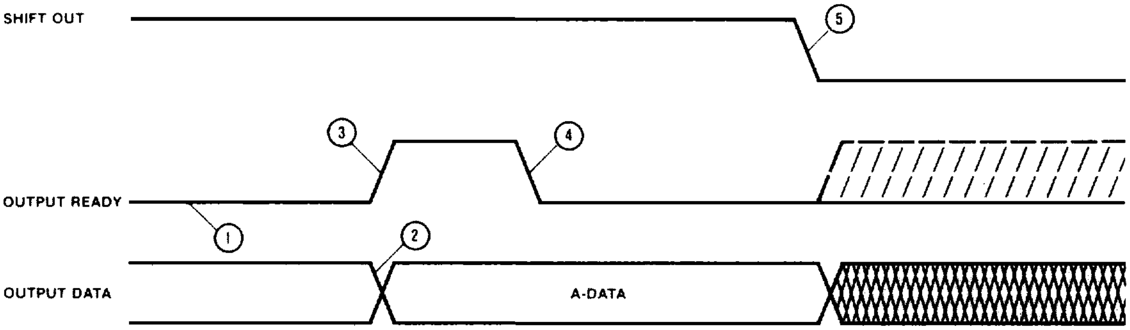


Figure 9. Data is Shifted Out Whenever Shift Out and Output Ready are Both HIGH.

① Word 63 is empty

② New data (A) arrives at the outputs (word 63).

③ Output Ready goes HIGH indicating the arrival of the new data

④ Since Shift Out is held HIGH, Output Ready goes immediately LOW

⑤ As soon as Shift Out goes LOW the Output Data is subject to change as shown by the dashed line on Output Ready

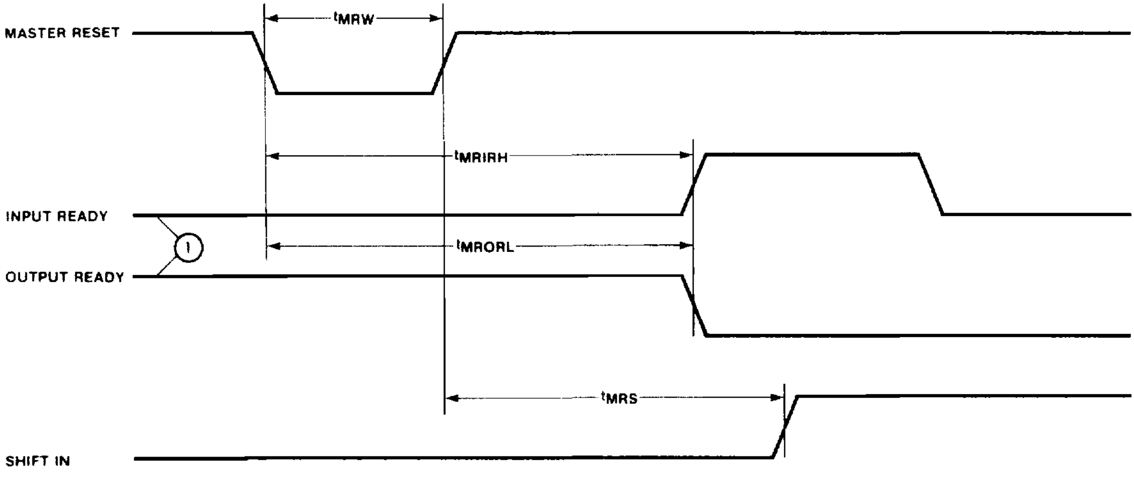
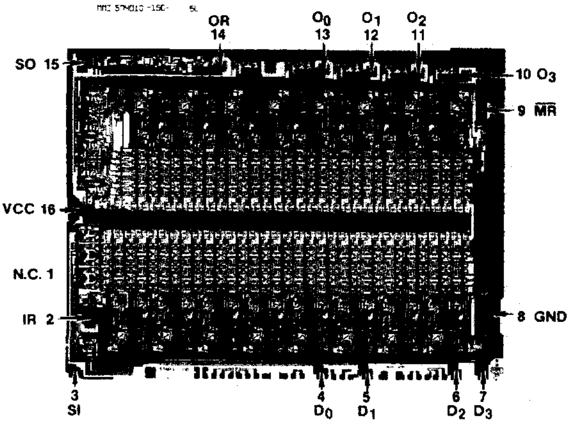


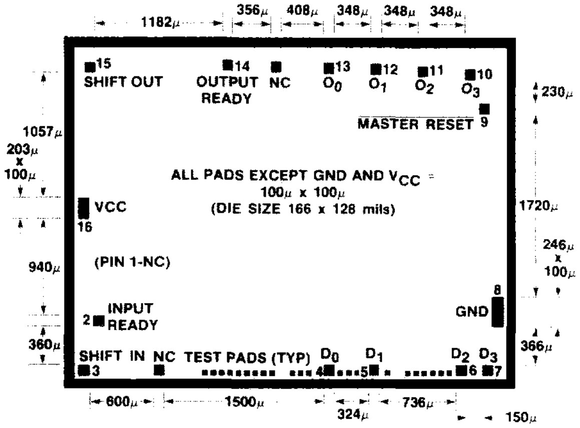
Figure 10. Master Reset Timing

① FIFO initially full

Die Configurations

57401 Die Pattern
Step: G
Die Size: 128x166 mil^2





57402 Die Pattern
Step: G
Die Size: 128x166 mil^2