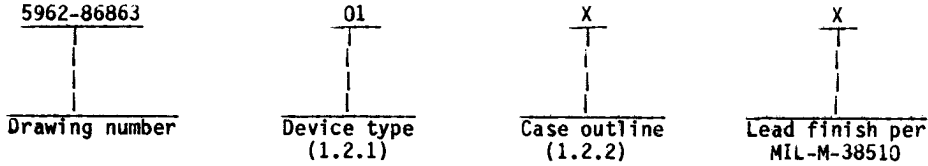


1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:



1.2.1 Device type. The device type shall identify the circuit function as follows:

Device type	generic number	Circuit function
01	29116	High-performance 16-bit bipolar microprocessor

1.2.2 Case outline. The case outline shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
X	See figure 1 (52-lead, 13/16" x 2 5/8"), <i>dip, 52, .9</i> dual-in-line package

1.3 Absolute maximum ratings. 1/

Supply voltage range - - - - -	-0.5 V dc to +7.0 V dc
Input voltage range - - - - -	-0.5 V dc to +5.5 V dc
Storage temperature range - - - - -	-65°C to +150°C
Maximum power dissipation (P _D) 2/ - - - - -	4.1 W
Lead temperature (soldering, 10 seconds) - - - - -	+300°C
Thermal resistance, junction-to-case (θ _{JC}):	
Case X - - - - -	4°C/W
Junction temperature (T _J) - - - - -	+200°C
DC voltage applied to outputs for high output state - - - - -	-0.5 V dc to +5.5 V dc
DC input voltage - - - - -	-0.5 V dc to +5.5 V dc
DC output current, into outputs - - - - -	30 mA
DC input current - - - - -	-30 mA to +5.0 mA

1.4 Recommended operating conditions. 1/

Supply voltage (V _{CC}) - - - - -	+4.5 V dc to +5.5 V dc
Minimum high level input voltage (V _{IH}) - - - - -	2.0 V dc
Maximum low level input voltage (V _{IL}) - - - - -	0.8 V dc
Case operating temperature range (T _C) - - - - -	-55°C to +125°C

1/ Ratings and conditions apply to heat sink configuration supplied by the manufacturer (see figure 1).

2/ Must withstand the added P_D due to short-circuit test (e.g., I_{OS}).

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2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.2 Block diagram. The block diagram shall be as specified on figure 3.

3.2.3 Case outline. The case outline shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full recommended case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ -55°C < T _C < +125°C V _{CC} = 4.5 V dc to 5.5 V dc (unless otherwise specified)		Group A subgroups	Limits		Unit
					Min	Max	
Output high voltage	V _{OH}	V _{CC} = 4.5 V dc V _{IN} = V _{IH} or V _{IL} I _{OH} = -1.2 mA	Y ₀₋₁₅ T ₁₋₄ CT	1, 2, 3	2.4		V
Output low voltage	V _{OL}	V _{CC} = 4.5 V dc V _{IN} = V _{IH} or V _{IL} I _{OL} = 12 mA	Y ₀₋₁₅ T ₁₋₄ CT	1, 2, 3		0.5	V
Input logical high voltage	V _{IH}			1, 2, 3	2.0		V
Input logical low voltage	V _{IL}			1, 2, 3		0.8	V
Input clamp voltage	V _I	V _{CC} = 4.5 V dc I _{IN} = -18 mA	All inputs	1, 2, 3		-1.5	V
Input low current	I _{IL}	V _{CC} = 5.5 V dc V _{IN} = 0.5 V 2/	I _{EN} SRE DLE I ₀₋₄ I ₅₋₁₅ OET OEY CP T ₁₋₄ Y ₀₋₁₅	1, 2, 3		-0.50 -0.50 -1.00 -1.00 -0.50 -0.50 -0.50 -1.50 -0.55 -0.55	mA
Input high current	I _{IH1}	V _{CC} = 5.5 V dc V _{IN} = 2.4 V 2/	I _{EN} SRE DLE I ₀₋₄ I ₅₋₁₅ OET OEY CP T ₁₋₄ Y ₀₋₁₅	1, 2, 3		50 50 100 100 50 50 50 150 100 100	μA
Input high current	I _{IH2}	V _{CC} = 5.5 V dc V _{IN} = 5.5 V	All inputs	1, 2, 3		1.0	mA
Off state (high impedance) output current	I _{OZH}	V _{CC} = 5.5 V dc V _O = 2.4 V 2/	T ₁₋₄ Y ₀₋₁₅	1, 2, 3		100	μA

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C < T _C < +125°C V _{CC} = 4.5 V dc to 5.5 V dc (unless otherwise specified)	1/ T ₁₋₄ Y ₀₋₁₅	Group A subgroups	Limits		Unit
					Min	Max	
Off state (high impedance) output current	I _{OZL}	V _{CC} = 5.5 V dc V _O = 0.5 V <u>2/</u>	T ₁₋₄ Y ₀₋₁₅	1, 2, 3		-550	μA
Output short-circuit current	I _{OS}	V _{CC} = 6.0 V dc V _O = 0.5 V <u>1/</u>	T ₁₋₄ Y ₀₋₁₅	1, 2, 3	-30	-85	mA
Power supply current <u>3/</u>	I _{CC}	V _{CC} = 5.5 V dc T _C = -55° to +125°C		1, 2, 3		745	mA
		V _{CC} = 5.5 V dc T _C = +125°C		2		525	
Setup time <u>1</u> <u>4/</u> Hold time <u>1</u> <u>4/</u> Input: I ₀₋₄ (RAM ADDR) with respect to: CP	t _{S1} t _{h1}	C _L = 50 pF (See figure 4) Single address (source)		9, 10, 11	24 0		ns
Setup time <u>2</u> <u>4/</u> Hold time <u>7</u> <u>5/</u> Input: I ₀₋₄ (RAM ADDR) with respect to: CP and IEN, both low	t _{S2} t _{h7}	C _L = 50 pF (See figure 4) Two address (destination)		9, 10, 11	10 0		ns
Setup time <u>3</u> <u>4/</u> <u>6/</u> Hold time <u>3</u> <u>4/</u> <u>6/</u> Setup time <u>9</u> <u>5/</u> Hold time <u>9</u> <u>5/</u> Input: I ₀₋₁₅ (INSTR) with respect to: CP	t _{S3} t _{h3} t _{S9} t _{h9}	C _L = 50 pF (See figure 4)		9, 10, 11	57 17 76 3		ns
Setup time <u>4</u> <u>4/</u> Hold time <u>10</u> <u>5/</u> Input: IEN HIGH with respect to: CP	t _{S4} t _{h10}	C _L = 50 pF (See figure 4) (Disable)		9, 10, 11	10 1		ns
Setup time <u>5</u> <u>4/</u> <u>7/</u> Hold time <u>5</u> <u>4/</u> <u>6/</u> <u>7/</u> Setup time <u>11</u> <u>5/</u> <u>8/</u> Hold time <u>11</u> <u>5/</u> <u>8/</u> <u>9/</u> Input: IEN LOW with respect to: CP	t _{S5} t _{h5} t _{S11} t _{h11}	C _L = 50 pF (See figure 4)		9, 10, 11	20 3 28 1		ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C < T _C < +125°C V _{CC} = 4.5 V dc to 5.5 V dc (unless otherwise specified)	Group A subgroups	Limits		Unit
				Min	Max	
Setup time 6 4/ Hold time 6 4/ Input: Y with respect to: DLE	t _{S6} t _{h6}	C _L = 50 pF (See figure 4)	9, 10, 11	11 7		ns
Setup time 8 5/ Hold time 8 5/ Input: I ₀₋₁₅ (DATA) with respect to: CP	t _{S8} t _{h8}	C _L = 50 pF (See figure 4)	9, 10, 11	76 3		ns
Setup time 12 5/ Hold time 12 5/ Input: SRE with respect to: CP	t _{S12} t _{h12}	C _L = 50 pF (See figure 4)	9, 10, 11	19 0		ns
Setup time 13 5/ Hold time 13 5/ Input: Y with respect to: CP	t _{S13} t _{h13}	C _L = 50 pF (See figure 4)	9, 10, 11	50 2		ns
Setup time 14 5/ Hold time 14 5/ Input: DLE with respect to: CP	t _{S14} t _{h14}	C _L = 50 pF (See figure 4)	9, 10, 11	50 0		ns
Propagation delays 1, 2 10/ From: I ₀₋₄ (ADDR) To: (output) Y ₀₋₁₅ To: T ₁₋₄	t _{pd1} t _{pd2}	C _L = 50 pF (See figure 4)	9, 10, 11		100 103	ns
Propagation delays 3, 4 10/ From: I ₀₋₁₅ (DATA) To: (output) Y ₀₋₁₅ To: T ₁₋₄	t _{pd3} t _{pd4}	C _L = 50 pF (See figure 4)	9, 10, 11		100 103	ns
Propagation delays 5, 6, 7 From: I ₀₋₁₅ (INSTR) To: (output) Y ₀₋₁₅ 10/ To: T ₁₋₄ To: CT	t _{pd5} t _{pd6} t _{pd7}	C _L = 50 pF (See figure 4)	9, 10, 11		100 103 50	ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C < T _C < +125°C V _{CC} = 4.5 V dc to 5.5 V dc (unless otherwise specified)	Group A subgroups	Limits		Unit
				Min	Max	
Propagation delays 8, 9 10/ From: (input) DLE To: (output) Y ₀₋₁₅ 11/ To: T ₁₋₄	t _{pd8} t _{pd9}	C _L = 50 pF (See figure 4)	9, 10, 11		68 70	ns
Propagation delay 10 From: t ₁₋₄ To: CT	t _{pd10}	C _L = 50 pF (See figure 4)	9, 10, 11		46	ns
Propagation delays 11, 12, 13 10/ From: CP To: Y ₀₋₁₅ To: T ₁₋₄ To: CT	t _{pd11} t _{pd12} t _{pd13}	C _L = 50 pF (See figure 4)	9, 10, 11		70 73 43	ns
Propagation delays 14, 15 10/ From: Y ₀₋₁₅ To: Y ₀₋₁₅ 11/ To: T ₁₋₄	t _{pd14} t _{pd15}	C _L = 50 pF (See figure 4)	9, 10, 11		70 72	ns
Propagation delay 16 From: IEN To: CT	t _{pd16}	C _L = 50 pF (See figure 4)	9, 10, 11		50	ns
Enable time 1 From input: OE _Y To output: Y ₀₋₁₅	t _{pZH1} t _{pZL1}	C _L = 50 pF (See figure 4)	9, 10, 11	25 25		ns
Disable time 1 From input: OE _Y To output: Y ₀₋₁₅	t _{pHZ1} t _{pLZ1}	C _L = 5 pF (See figure 4)	9, 10, 11		25 25	ns
Enable time 2 From input: OE _T To output: T ₁₋₄	t _{pZH2} t _{pZL2}	C _L = 50 pF (See figure 4)	9, 10, 11	30 30		ns
Disable time 2 From input: OE _T To output: T ₁₋₄	t _{pHZ2} t _{pLZ2}	C _L = 5 pF (See figure 4)	9, 10, 11		30 30	ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C < T _C < +125°C V _{CC} = 4.5 V dc to 5.5 V dc (unless otherwise specified)	Group A subgroups	Limits		Unit
				Min	Max	
Minimum clock and pulse low time Input CP Input IEN	t _{CL1} t _{CL2}		9, 10, 11	33 33		ns
Minimum clock and pulse high time Input CP Input DLE	t _{CH1} t _{CH2}		9, 10, 11	50 20		ns

- 1/ Not more than one output should be shorted at a time. Duration of the short-circuit test should not exceed one second.
- 2/ Y₀₋₁₅, t₁₋₄ are three-state outputs internally connected to TTL inputs. Input characteristics are measured under conditions such that the outputs are in the off state.
- 3/ Worst case I_{CC} is at minimum temperature.
- 4/ High-to-low transition.
- 5/ Low-to-high transition.
- 6/ Timing for immediate instruction for first cycle.
- 7/ These limits apply to the immediate first cycle, not to the enable state.
- 8/ Enable state.
- 9/ Status register and accumulator destination only.
- 10/ Y₀₋₁₅ must be stored in the data latch and its source disabled before the delay to Y₀₋₁₅ as an output can be measured.
- 11/ Guaranteed indirectly by other tests.

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

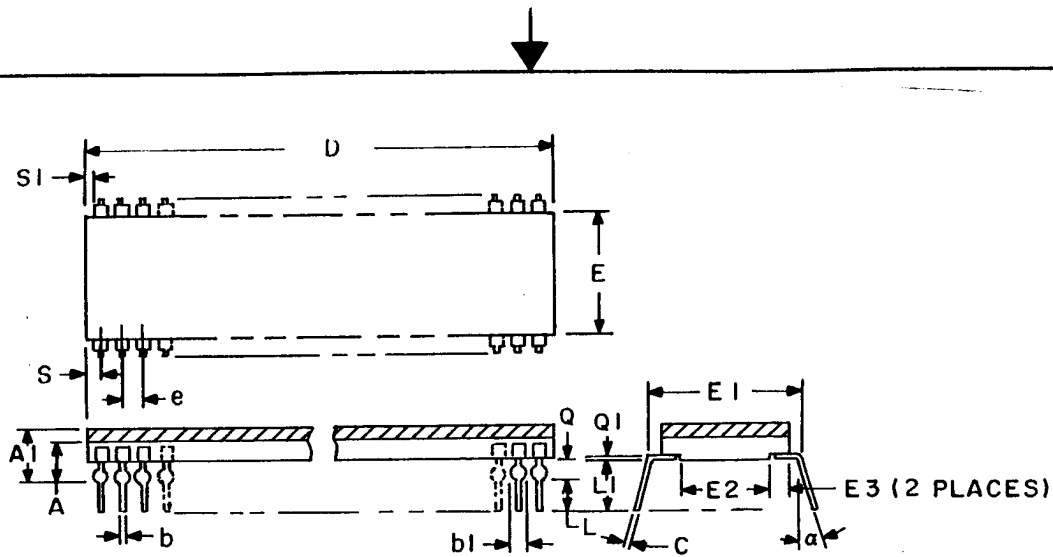
3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

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Parameter	Min.	Max.
A	.145	.195
A1	.210	.270
b	.015	.020
b1	.030	.060
C	.008	.013
D	2.565	2.640
E	.780	.825
E1	.870	.920
E2	.630	----
E3	.050	----
e	.090	.110
L	.100	.160
Q	.070	.130
S	----	.098
SI	.005	----
α	0°	15°
L1	.150	----
Q1	.020	----

NOTES:

1. Index area: A notice, tab or pin one identification mark shall be located adjacent to pin one.
2. A1 dimension includes heat sink; also D and E dimensions allow for heat sink off-centering.
3. E1 and α are measured at the centerline of the leads.
4. Dimensions b, b1 and C increase by 3 mils maximum when tin plate or solder dip lead finish is applied.
5. Dimensions A, A1, Q and L are measured at the seating plane or lead frame shoulder width at .0415/.043 inch.
6. Dimensions are in inches.

FIGURE 1. Case outline.

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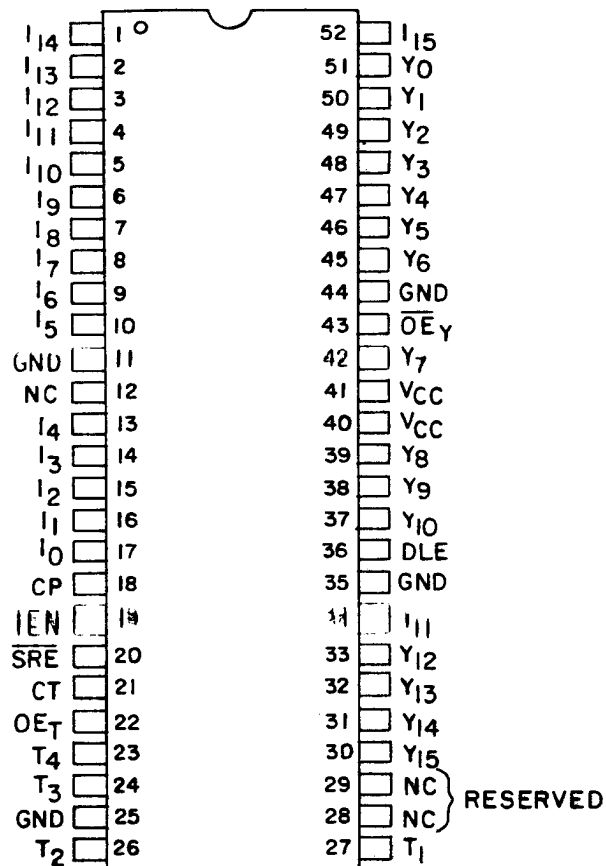


FIGURE 2. Terminal connections (top view).

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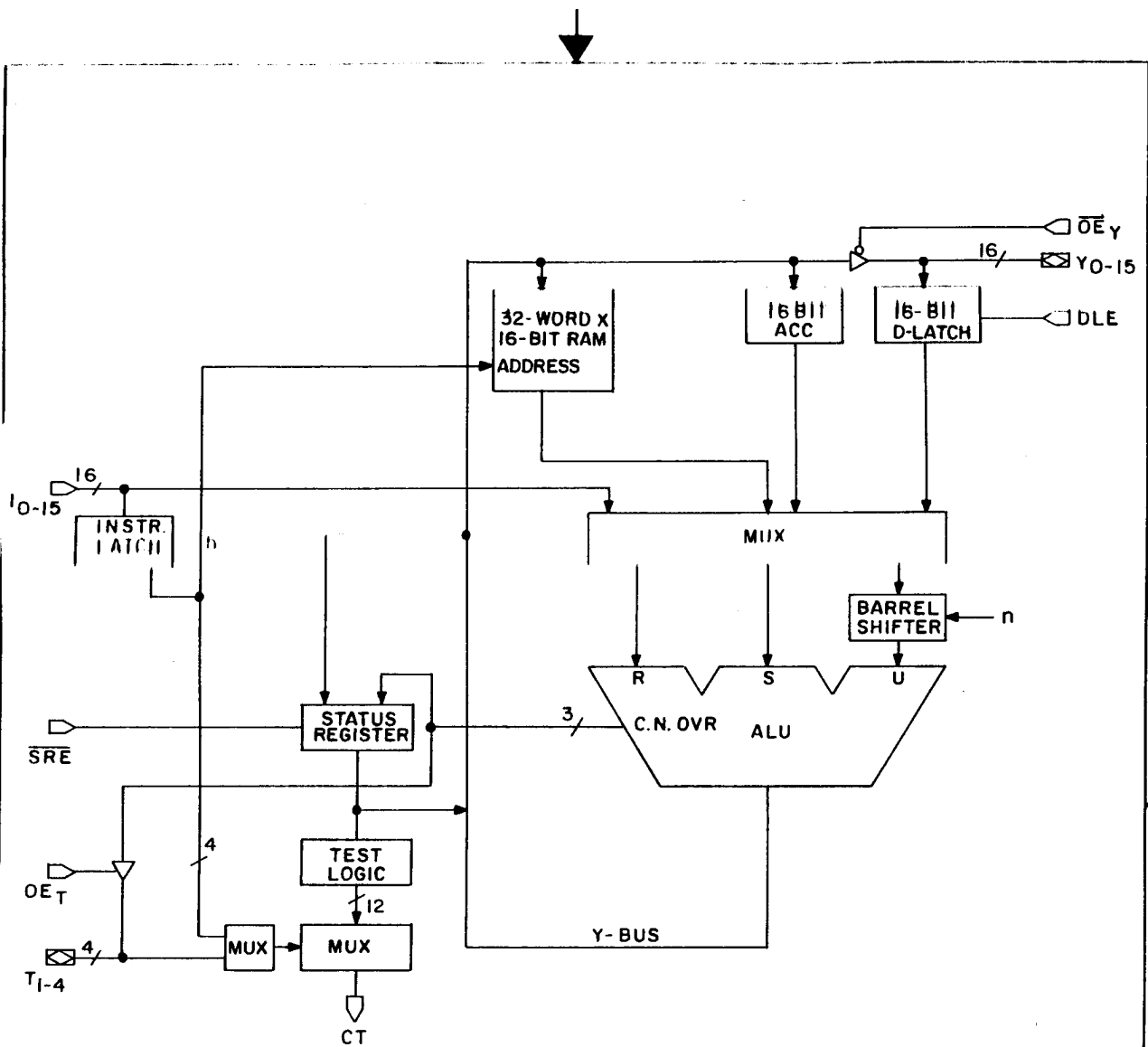
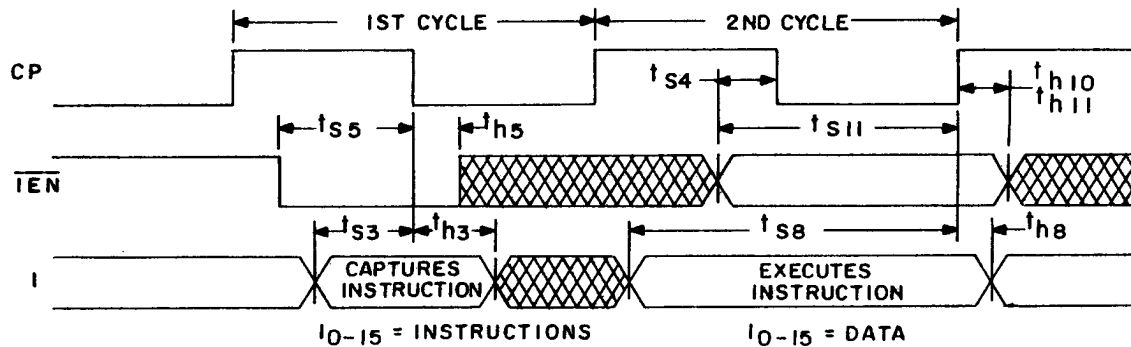


FIGURE 3. Block diagram.

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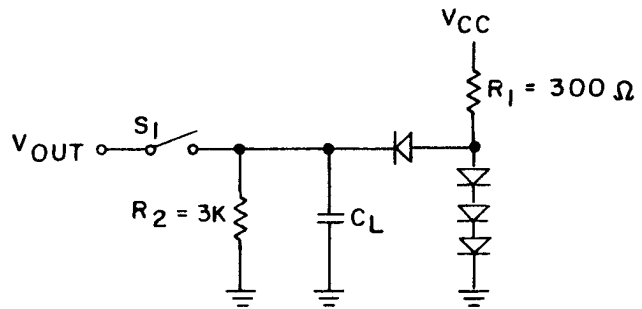
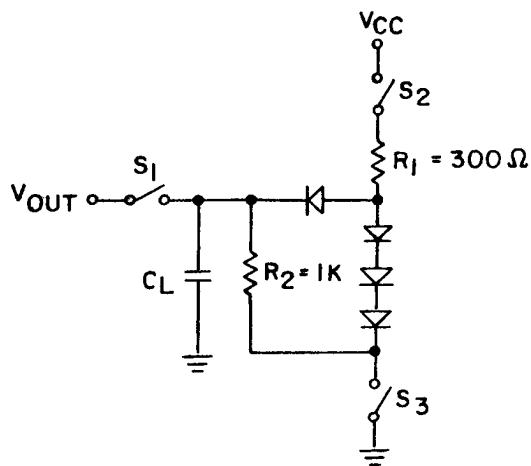


IMMEDIATE INSTRUCTION CYCLE TIMING

SWITCHING TEST CIRCUITS

A. THREE-STATE OUTPUTS

B. NORMAL OUTPUTS

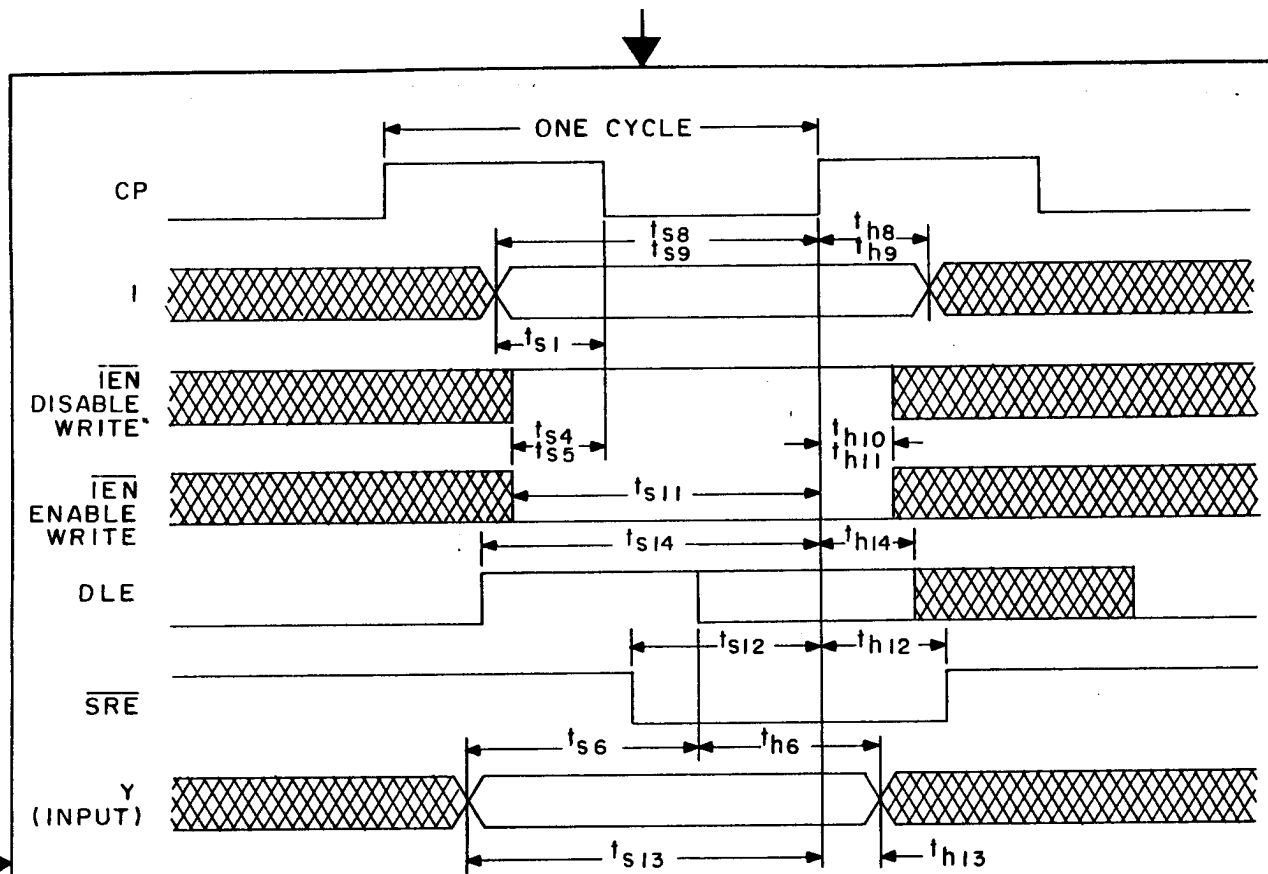


NOTES:

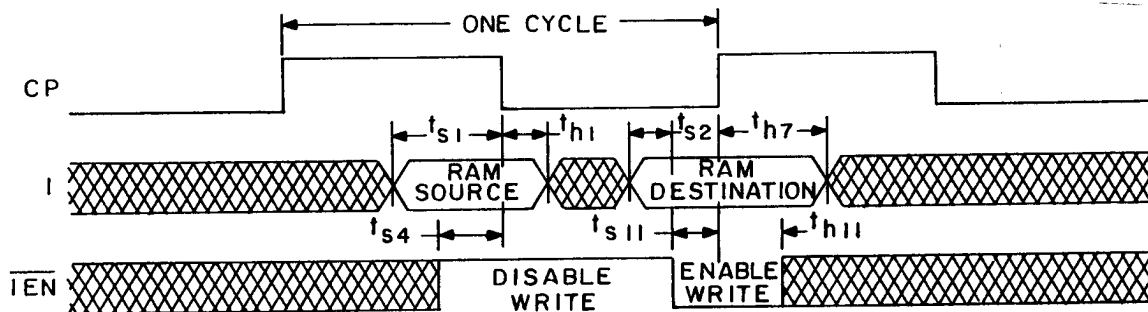
1. $C_L = 50 \text{ pF}$ includes scope probe, wiring and stray capacitances without device in test fixture.
2. S_1, S_2, S_3 are closed during function tests and all AC tests except output enable tests.
3. S_1 and S_3 are closed while S_2 is open for t_{pZH} test.
 S_1 and S_3 are closed while S_2 is open for t_{pZL} test.
4. $C_L = 5.0 \text{ pF}$ for output disable tests.

FIGURE 4. Switching waveforms.

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SINGLE ADDRESS ACCESS TIMING
 (IF t_{h6} IS SATISFIED, t_{h13} NEED NOT BE SATISFIED)

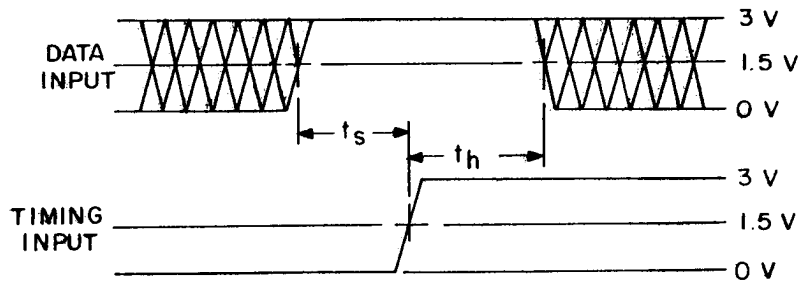


DOUBLE ADDRESS ACCESS TIMING

FIGURE 4. Switching waveforms - Continued.

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SETUP, HOLD, AND RELEASE TIMES



NOTES:

1. Diagram shown for HIGH data only. Output transition may be opposite sense.
2. Cross-hatched area is don't care condition.

PROPAGATION DELAY

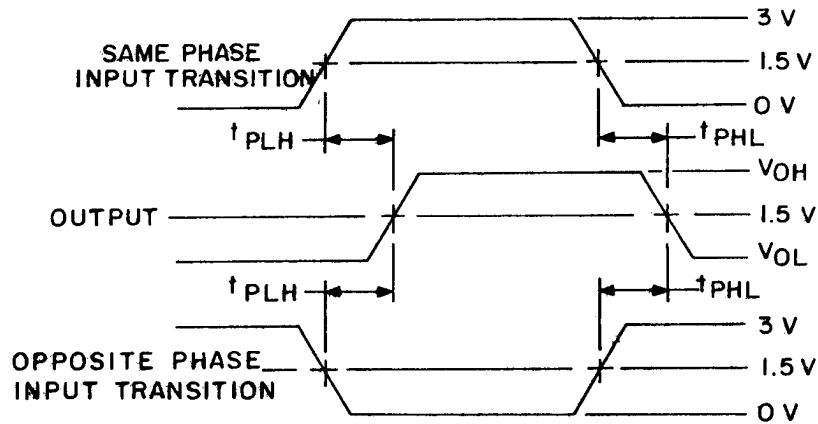
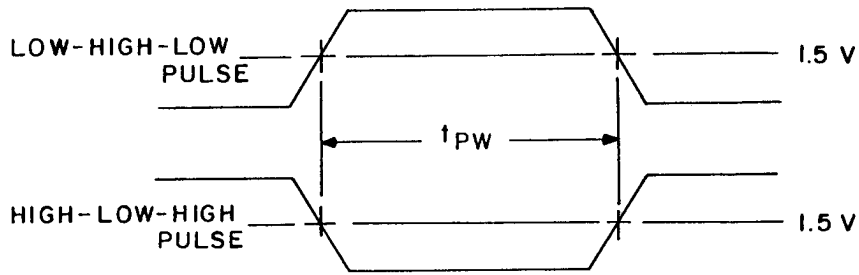


FIGURE 4. Switching waveforms - Continued.

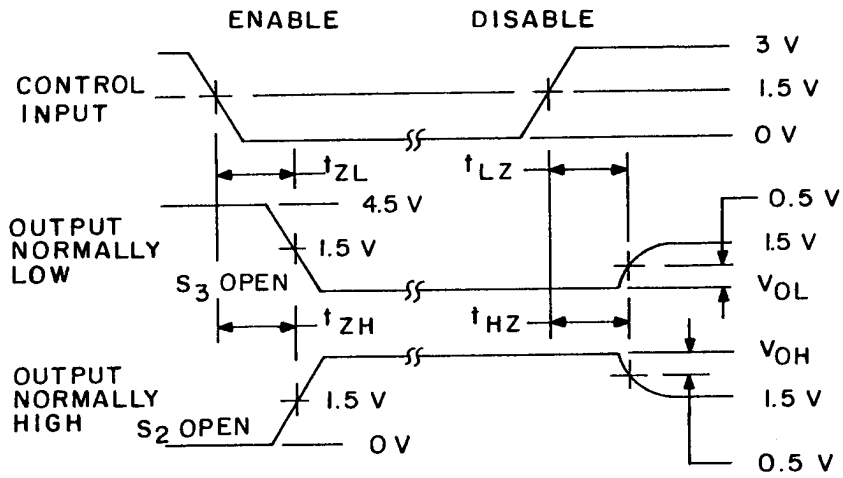
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PULSE WIDTH



ENABLE AND DISABLE TIMES



NOTES:

1. Diagram shown for input control enable low and input control disable high.
2. S_1 , S_2 and S_3 of load circuit are closed except where shown.
3. Pulse generator for all pulses: Rate ≤ 1.0 MHz, $Z_0 = 50\Omega$; $t_r \leq 2.5$ ns.

FIGURE 4. Switching waveforms - Continued.

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4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

- a. Burn-in test (method 1015 of MIL-STD-883).
 - (1) Test condition C or D, using the circuit submitted with the certificate of compliance (see 3.5 herein).
 - (2) $T_A = +125^\circ\text{C}$, minimum.
- b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

- a. Tests shall be as specified in table II herein.
- b. Subgroups 4, 5, 6, 7, and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004)	1*, 2, 3, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3
Additional electrical subgroups for group C periodic inspections	---

* PDA applies to subgroup 1.

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4.3.2 Groups C and D inspections.

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady-state life test (method 1005 of MIL-STD-883) conditions:
 - (1) Test condition C or D, using the circuit submitted with the certificate of compliance (see 3.5 herein).
 - (2) $T_A = +125^{\circ}\text{C}$, minimum.
 - (3) Test duration: 1,000 hours, except as permitted by appendix B of MIL-M-38510 and method 1005 of MIL-STD-883.
- c. Some group C and group D tests may be performed without the heat sink attached.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.4 Approved source of supply. An approved source of supply is listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.5 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number ^{1/}
5962-8686301XX	34335	AM29116/BXC

^{1/} Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number

34335

Vendor name and address

Advanced Micro Devices
901 Thompson Place
Sunnyvale, CA 94086

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