REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Technical and editorial changes throughout. Add vendor CAGE 04713 for device type 01. Add characterization for device classes B, S, Q and V. Add ground bounce and latch-up immunity characterization. Add 10.1 substitution statement.	92-12-15	Monica L. Poelking
B	Technical and editorial changes throughout. Add RHA requirements. - CS	97-10-16	Monica L. Poelking

REV																				
SHEET																				
REV	B	B	B	B	B	B	B	B	B	B	B	B	B							
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27							
REV STATUS				REV			B	B	B	B	B	B	B	B	B	B	B	B	B	B
OF SHEETS				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
Greg A. Pitz

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
D. A. DiCenzo

APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
88-01-06

REVISION LEVEL
B

MICROCIRCUIT, DIGITAL, ADVANCED CMOS, DUAL D-TYPE FLIP-FLOP, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-87525**

SHEET 1 OF 27

DSCC FORM 2233
APR 97

5962-E305-97

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

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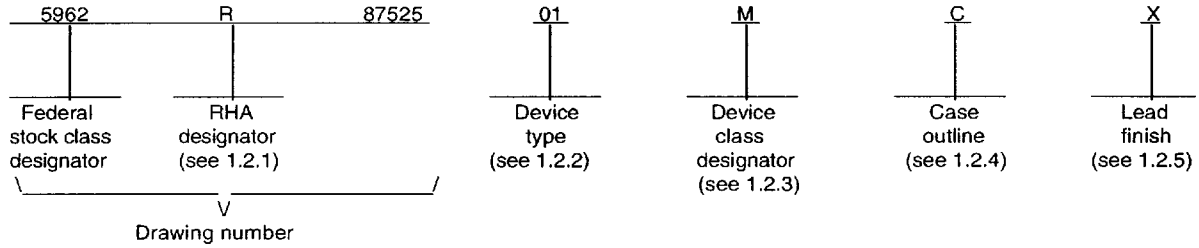
1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes B, Q and M), and space application (device classes S and V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device classes M, B, and S RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54ACT74	Dual D-type flip-flop with preset and clear, TTL compatible inputs
02	54ACT11074	Dual D-type flip-flop with preset and clear, TTL compatible inputs

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
B or S	Certification and qualification to MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
C	GDIP1-T14 or CDIP2-T14	14	Dual-in-line
D	GDFP1-F14 or CDFP2-F14	14	Flat
2	CQCC1-N20 or CQCC2-N20	20	Leadless-chip-carrier

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q, and V or MIL-PRF-38535, appendix A for device classes M, B, and S.

1.3 Absolute maximum ratings. 1/ 2/

Supply voltage range (V_{CC}) ..... -0.5 V dc to +6.0 V dc
DC input voltage range (V_{IN}) ..... -0.5 V dc to V_{CC} + 0.5 V dc
DC output voltage range (V_{OUT}) ..... -0.5 V dc to V_{CC} + 0.5 V dc
Clamp diode current (I_{IK}, I_{OK}) ..... ±20 mA
DC output current (I_{OUT}) ..... ±50 mA
DC V_{CC} or GND current (I_{CC}, I_{GND}) ..... ±100 mA 3/
Storage temperature range (T_{STG}) ..... -65°C to +150°C
Maximum power dissipation (P_D) ..... 500 mW
Lead temperature (soldering, 10 seconds) ..... +300°C
Thermal resistance, junction-to-case (θ_{JC}) ..... See MIL-M-1835
Junction temperature (T_J) ..... +175°C
Case operating temperature (T_C) ..... -55°C to +125°C

1.4 Recommended operating conditions. 1/ 2/ 4/

Supply voltage range (V_{CC}) ..... +4.5 V dc to +5..5 V dc
Input voltage range (V_{IN}) ..... +0.0 V dc to V_{CC}
Output voltage range (V_{OUT}) ..... +0.0 V dc to V_{CC}
Maximum low level input voltage (V_{IL}) ..... 0.8 V dc at V_{CC} = 4.5 V dc
0.8 V dc at V_{CC} = 5.5 V dc
Minimum high level input voltage (V_{IH}) ..... 2.0 V dc at V_{CC} = 4.5 V dc
2.0 V dc at V_{CC} = 5.5 V dc
Case operating temperature range (T_C) ..... -55°C to +125°C
Input rise and fall rate (t_r, t_f) maximum:
V_{CC} = 4.5 V ..... 10 ns/V
V_{CC} = 5.5 V ..... 8 ns/V
Maximum high level output current (I_{OH}) ..... -24 mA
Maximum low level output current (I_{OL}) ..... 24 mA

1.5 Digital logic testing for device classes Q, and V.

Fault coverage measurement of manufacturing
logic tests (MIL-STD-883, test method 5012) ..... XX percent 5/

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability. The maximum junction temperature may be exceeded for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.
2/ Unless otherwise noted, all voltages are referenced to GND.
3/ For packages with multiple V_{CC} and GND pins, this value represents the maximum total current flowing into or out of all V_{CC} or GND pins.
4/ Unless otherwise specified, the values listed above shall apply over the full V_{CC} and T_C recommended operating range.
5/ Values will be added when they become available.

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2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Interface Standard For Microcircuit Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DOD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

ELECTRONIC INDUSTRIES ASSOCIATION (EIA)

JEDEC Standard No. 17 - A Standardized Test Procedure for the Characterization of the LATCH-UP in CMOS Integrated Circuits.

JEDEC Standard No. 20 - Standardized for Description of 54/74ACXXXX and 54/74ACTXXXX Advanced High-Speed CMOS Devices.

(Applications for copies should be addressed to the Electronics Industries Association, 2001 Eye Street, NW, Washington, DC 20006.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents may also be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

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3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q, and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device classes M, B, and S shall be in accordance with MIL-PRF-38535, appendix A and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q, and V or MIL-PRF-38535, appendix A and herein for device classes M, B, and S.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 2.

3.2.4 Block or logic diagram(s). The block or logic diagram(s) shall be as specified on figure 3.

3.2.5 Ground bounce waveforms and test circuit. The ground bounce waveforms and test circuit shall be as specified on figure 4.

3.2.6 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 5.

3.2.7 Schematic circuits. The schematic circuits shall be submitted to the preparing activity prior to the inclusion of a manufacturer's device in this drawing and shall be submitted to the qualifying activity as a prerequisite for qualification for device classes B and S. All qualified manufacturer's schematics shall be maintained and available upon request.

3.2.8 Radiation exposure circuit. The radiation exposure circuit shall be as specified when available.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range. Test conditions for these specified characteristics and limits are as specified in table I. For device classes B and S, a pin-for-pin conditions and testing sequence for table I parameters shall be maintained and available upon request from the qualifying activity on qualified devices.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q, and V shall be in accordance with MIL-PRF-38535. Marking for device classes M, B, and S shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q, V, B and S shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.5.2 Correctness of indexing and marking for device classes B and S. For device classes B and S, all devices shall be subjected to the final electrical tests specified in table II after PIN marking (marked in accordance with MIL-PRF-38535, appendix A) to verify that they are correctly indexed and identified by PIN. Optionally, an approved electrical test may be devised especially for this requirement.

3.6 Certificate of compliance. For device classes Q, and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device classes M, B and S a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q, and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

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3.7 Certificate of conformance. A certificate of conformance as required for device classes Q, and V in MIL-PRF-38535 or for device classes M, B, and S in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device classes M, B and S. For device classes M, B and S, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device classes M, B, and S. Device classes M, B, and S devices covered by this drawing shall be in microcircuit group number 38 (see MIL-PRF-38535, appendix A).

3.11 Serialization for device class S. All device class S devices shall be serialized in accordance with MIL-PRF-38535, appendix A.

3.12 Substitution. Substitution data shall be as indicated in the appendix herein.

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TABLE I. Electrical performance characteristics.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified		Device type 3/ and device class	V_{CC}	Group A subgroups	Limits 2/		Unit
							Min	Max	
High level output voltage 3006	V_{OH1} 4/	For all inputs affecting output under test $V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 2.0\ V$ $V_{IL} = 0.8\ V$ For all other inputs $V_{IN} = V_{CC}$ or GND $I_{OH} = -50\ \mu A$		All All	4.5 V	1, 2, 3	4.4		V
	V_{OH2}	For all inputs affecting output under test $V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 2.0\ V$ $V_{IL} = 0.8\ V$		All All	5.5 V	1, 2, 3	5.4		
		For all other inputs $V_{IN} = V_{CC}$ or GND $I_{OH} = -50\ \mu A$	M, D, L, R	01 B, S, Q, V		1			
	V_{OH3}	For all inputs affecting output under test $V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 2.0\ V$ $V_{IL} = 0.8\ V$		All All	4.5 V	1, 2, 3	3.7		
		For all other inputs $V_{IN} = V_{CC}$ or GND $I_{OH} = -24\ mA$	M, D, L, R	01 B, S, Q, V		1			
	V_{OH4} 4/	For all inputs affecting output under test $V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 2.0\ V$ $V_{IL} = 0.8\ V$ For all other inputs $V_{IN} = V_{CC}$ or GND $I_{OH} = -24\ mA$		All All	5.5 V	1, 2, 3	4.7		
	V_{OH5} 5/	For all inputs affecting output under test $V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 2.0\ V$ $V_{IL} = 0.8\ V$		All All	5.5 V	1, 2, 3	3.85		
		For all other inputs $V_{IN} = V_{CC}$ or GND $I_{OH} = -50\ mA$	M, D, L, R	01 B, S, Q, V		1			

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ -55°C ≤ T_C ≤ +125°C 4.5 V ≤ V_{CC} ≤ 5.5 V unless otherwise specified		Device type 3/ and device class	V_{CC}	Group A subgroups	Limits 2/ Min	Limits 2/ Max	Unit
Low level output voltage 3007	V_{OL1} 4/	For all inputs affecting output under test V_{IN} = V_{IH} or V_{IL} V_{IH} = 2.0 V V_{IL} = 0.8 V For all other inputs V_{IN} = V_{CC} or GND I_{OL} = 50 µA		All All	4.5 V	1, 2, 3		0.1	V
	V_{OL2}	For all inputs affecting output under test V_{IN} = V_{IH} or V_{IL} V_{IH} = 2.0 V V_{IL} = 0.8 V		All All	5.5 V	1, 2, 3		0.1	
		For all other inputs V_{IN} = V_{CC} or GND I_{OL} = 50 µA	M, D, L, R	01 B, S, Q, V		1			
	V_{OL3}	For all inputs affecting output under test V_{IN} = V_{IH} or V_{IL} V_{IH} = 2.0 V V_{IL} = 0.8 V		All B, S, Q, V	4.5 V	1, 3		0.4	
						2		0.5	
		For all other inputs V_{IN} = V_{CC} or GND I_{OL} = 24 mA	M, D, L, R	01 B, S, Q, V		1		0.4	
				All		1		0.4	
				M		2, 3		0.5	
	V_{OL4} 4/	For all inputs affecting output under test V_{IN} = V_{IH} or V_{IL} V_{IH} = 2.0 V		All B, S, Q, V	5.5 V	1, 3		0.4	
						2		0.5	
		V_{IL} = 0.8 V For all other inputs V_{IN} = V_{CC} or GND I_{OL} = 24 mA		All M		1		0.4	
						2, 3		0.5	
	V_{OL5} 5/	For all inputs affecting output under test V_{IN} = V_{IH} or V_{IL} V_{IH} = 2.0 V V_{IL} = 0.8 V For all other inputs		All All	5.5 V	1, 2, 3		1.65	
		VIN = VCC or GND IOL = 50 mA	M, D, L, R	01 B, S, Q, V		1			

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified		Device type 3/ and device class	V_{CC}	Group A subgroups	Limits 2/		Unit
							Min	Max	
Positive input clamp voltage 3022	V_{IC+}	V_{CC} = GND For input under test I_{IN} = 1 mA		All B, S, Q, V		1	0.4	1.5	V
			M, D, L, R	01 B, S, Q, V		1			
Negative input clamp voltage 3022	V_{IC-}	V_{CC} = Open For input under test IIN = -1 mA		All B, S, Q, V		1	-0.4	-1.5	V
			M, D, L, R	01 B, S, Q, V		1			
Input current high 3010	I_{IH}	For input under test $V_{IN} = V_{CC}$		All B, S, Q, V	5.5 V	1		0.1	µA
						2		1.0	
		For all other inputs $V_{IN} = V_{CC}$ or GND		All M		1		0.1	
						2, 3		1.0	
			M, D, L, R	01 B, S, Q, V		1		0.1	
Input current low 3009	I_{IL}	For input under test V_{IN} = GND		All B, S, Q, V	5.5 V	1		-0.1	µA
						2		-1.0	
		For all other inputs $V_{IN} = V_{CC}$ or GND		All M		1		-0.1	
						2, 3		-1.0	
			M, D, L, R	01 B, S, Q, V		1		-0.1	
Input capacitance 3012	C_{IN}	See 4.4.1c T_C = +25°C		01 All	GND	4		10	pF
				02 All				7	
Power dissipation capacitance	C_{PD} 6/	See 4.4.1c T_C = +25°C		01 All	5.0 V	4		70	pF
				02 All				38	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified		Device type 3/ and device class	V_{CC}	Group A subgroups	Limits 2/ Min	Limits 2/ Max	Unit
Quiescent supply current delta, TTL input levels 3005	ΔI_{CC} 7/	For input under test $V_{IN} = V_{CC} - 2.1\ V$ For all other inputs $V_{IN} = V_{CC}$ or GND		All B, S, Q, V	5.5 V	3		1.6	mA
						1, 2		1.0	
				All M		1, 2, 3		1.6	
			M	01 B, S, Q, V		1		1.6	
			D					1.6	
			L					3.5	
			R					3.5	
Quiescent supply current, output high 3005	I_{CCH}	For all inputs $V_{IN} = V_{CC}$ or GND		All B, S, Q, V	5.5 V	1		1.0	µA
						2		20.0	
				All M		1		4.0	
						2, 3		80.0	
			M	01 B, S, Q, V		1		100.0	µA
			D					1.0	mA
			L					3.5	
			R					3.5	
Quiescent supply current, output low 3005	I_{CCL}	For all inputs $V_{IN} = V_{CC}$ or GND		All B, S, Q, V	5.5 V	1		1.0	µA
						2		20.0	
				All M		1		4.0	
						2, 3		80.0	
			M	01 B, S, Q, V		1		100.0	µA
			D					1.0	mA
			L					3.5	
			R					3.5	
Low level ground bounce noise	V_{GBL} 8/	$V_{LD} = 2.5\ V$, $I_{OL} = +24\ mA$ (see figure 4)		All B, S, Q, V	4.5 V	4		1000	mV
High level ground bounce noise	V_{GBH} 8/	$V_{LD} = 2.5\ V$, $I_{OH} = -24\ mA$ (see figure 4)		All B, S, Q, V	4.5 V	4		1000	mV

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Device type 3/ and device class	V_{CC}	Group A subgroups	Limits 2/		Unit
						Min	Max	
Latch-up input/ output over-voltage	I_{CC} (O/V1) 9/	$t_w \ge 100\ \mu s$ $t_{cool} \ge t_w$ $5\ \mu s \le t_r \le 5\ ms$ $5\ \mu s \le t_f \le 5\ ms$ $V_{test} = 6.0\ V$ $V_{CCQ} = 5.5\ V$ $V_{over} = 10.5\ V$	All B, S, Q, V	5.5 V	2		200	mA
Latch-up input/ output positive over-current	I_{CC} (O/I1+) 9/	$t_w \ge 100\ \mu s$ $t_{cool} \ge t_w$ $5\ \mu s \le t_r \le 5\ ms$ $5\ \mu s \le t_f \le 5\ ms$ $V_{test} = 6.0\ V$ $V_{CCQ} = 5.5\ V$ $I_{trigger} = +120\ mA$	All B, S, Q, V	5.5 V	2		200	mA
Latch-up input/ output negative over-current	I_{CC} (O/I1-) 9/	$t_w \ge 100\ \mu s$ $t_{cool} \ge t_w$ $5\ \mu s \le t_r \le 5\ ms$ $5\ \mu s \le t_f \le 5\ ms$ $V_{test} = 6.0\ V$ $V_{CCQ} = 5.5\ V$ $I_{trigger} = -120\ mA$	All B, S, Q, V	5.5 V	2		200	mA
Latch-up supply over-voltage	I_{CC} (O/V2) 9/	$t_w \ge 100\ \mu s$ $t_{cool} \ge t_w$ $5\ \mu s \le t_r \le 5\ ms$ $5\ \mu s \le t_f \le 5\ ms$ $V_{test} = 6.0\ V$ $V_{CCQ} = 5.5\ V$ $V_{over} = 9.0\ V$	All B, S, Q, V	5.5 V	2		100	mA
Truth table test output voltage 3014	10/	$V_{IL} = 0.40\ V$ $V_{IH} = 2.40\ V$ Verify output V_O	All All	4.5 V	7, 8	L	H	
			All M	5.5 V	7, 8	L	H	
		M, D, L, R	01 B, S, Q, V	4.5 V	7	L	H	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$, unless otherwise specified		Device type 3/ and device class	Vcc	Group A subgroups	Limits 2/		Unit
							Min	Max	
Propagation delay time, clock to output, CPn to Qn and Qn 3003	t_{PHL}, t_{PLH} 11/ 12/	C_L = 50 pF minimum, R_L = 500Ω, See figure 5		01 B, S, Q, V	4.5 V	9, 11	1.0	11.0	ns
						10	1.0	14.0	
				01 M		9	1.0	11.0	
						10, 11	1.0	14.0	
			M, D, L, R	01 B, S, Q, V		9	1.0	11.0	
				02 M		9	1.0	8.5	
						10, 11	1.0	10.0	
Propagation delay time, clear and set to output, CDn and SDn to Qn and Qn 3003	t_{PHL}, t_{PLH} 11/ 12/	C_L = 50 pF minimum, R_L = 500Ω, See figure 5		01 B, S, Q, V	4.5 V	9, 11	1.0	10.0	ns
						10	1.0	12.5	
				01 M		9	1.0	10.0	
						10, 11	1.0	12.5	
			M, D, L, R	01 B, S, Q, V		9	1.0	10.0	
				02 M		9	1.0	11.3	
						10, 11	1.0	13.3	
Maximum operating frequency 3003	f_{MAX}	C_L = 50 pF minimum, R_L = 500Ω, See figure 5 See 4.4.1f		01 B, S, Q, V	4.5 V	9, 11	95		MHz
						10	85		
				01 M		9	95		
						10, 11	85		
				02 M		9	100		
						10, 11	100		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Device type 3/ and device class	Vcc	Group A subgroups	Limits 2/		Unit
						Min	Max	
Input set-up time, Dn (high and low) to CPn	t_s	C_L = 50 pF minimum, R_L = 500Ω, See figure 5 See 4.4.1g	01 B, S, Q, V	4.5 V	9, 11	3.0		ns
					10	4.0		
			01 M		9	3.0		
					10, 11	4.0		
			02 M		9	4.5		
					10, 11	4.5		
Input hold time, Dn (high and low) after CPn	t_h	C_L = 50 pF minimum, R_L = 500Ω, See figure 5 See 4.4.1g	01 B, S, Q, V	5.5 V	9, 10	1.0		ns
					11	1.0		
			01 M		9	1.0		
					10, 11	1.0		
			02 M		9	0.0		
					10, 11	0.0		
Input recovery time CDn and SDn to CPn	t_{rec}	C_L = 50 pF minimum, R_L = 500Ω, See figure 5 See 4.4.1g	01 B, S, Q, V	5.5 V	9, 10	0.5		ns
					11	0.5		
			01 M		9	0.5		
					10, 11	0.5		
			02 M		9	2.0		
					10, 11	2.0		
Clock pulse width (high and low)	t_w	C_L = 50 pF minimum, R_L = 500Ω, See figure 5 See 4.4.1g	01 B, S, Q, V	4.5 V	9, 11	5.0		ns
					10	5.0		
			01 M		9	5.0		
					10, 11	6.0		
			02 M		9	5.0		
					10, 11	5.0		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Device type 3/ and device class	V_{CC}	Group A subgroups	Limits 2/		Unit
						Min	Max	
---- ---- CDn and SDn pulse width (low)	t_w	C_L = 50 pF minimum,	01	4.5 V	9, 11	6.5		ns
		R_L = 500Ω,	B, S, Q, V		10	7.0		
		See figure 5	01 M		9	6.5		
		See 4.4.1g			10, 11	7.0		
			02 M		9	5.0		
					10, 11	5.0		

1/ For tests not listed in MIL-STD-883 (e.g. ΔI_{CC}), utilize the general test procedure under the conditions listed herein. All inputs and outputs shall be tested, as applicable, to the tests in table 1 herein.

2/ Each input/output, as applicable shall be tested at the specified temperature for the specified limits. Output terminals not designated shall be high level logic, low level logic, or open, except as follows:

a. V_{IC} (pos) tests, the GND terminal can be open. T_C = +25°C.

b. V_{IC} (neg) tests, the V_{CC} terminal shall be open. T_C = +25°C.

c. All I_{CC} and ΔI_{CC} tests, the output terminal shall be open. When performing these tests, the current meter shall be placed in the circuit such that all current flows through the meter.

Additional detailed information on qualified devices (i.e., pin for pin conditions and testing sequence) is available from the qualifying activity (DSCC-VQC) upon request. For negative and positive voltage and current values: The sign designates the potential difference in reference to GND and the direction of current flow respectively; and the absolute value of the magnitude, not the sign, is relative to the minimum and maximum limits, as applicable, listed herein.

3/ The word "All" in the device type and device class column, means limits for all device types and classes.

4/ For device classes B and S, this test is guaranteed, if not tested, to the limits specified in table I.

5/ Transmission driving tests are performed at V_{CC} = 5.5 V dc with a 2 ms duration maximum. This test may be performed using V_{IN} = V CC or GND. When V_{IN} = V_{CC} or GND is used, the test is guaranteed for V_{IN} = 2.0 V or 0.8 V. For device class M, subgroup 1 testing shall be guaranteed if not tested to the limits specified in table I. For radiation hardness assured devices, subgroup 1 tests shall be performed.

6/ Power dissipation capacitance (C_{PD}) determines the no load dynamic power consumption, $P_D = (C_{PD} + C_L) (V_{CC} \times V_{CC})f + (I_{CC} \times V_{CC}) + (n \times d \times \Delta I_{CC} \times V_{CC})$. The dynamic current consumption, $I_S = (C_{PD} + C_L) V_{CC}f + I_{CC} + n \times d \times \Delta I_{CC}$. For both P D and I_S: n is the number of device inputs at TTL levels, f is the frequency of the input signal; and d is the duty cycle of the input signal.

7/ This test may be performed either one input at a time (preferred method) or with all input pins simultaneously at $V_{IN} = V_{CC}$ -2.1 V (alternate method). Classes B, S, Q, and V shall use the preferred method. When the test is performed using the alternate test method, the maximum limit is equal to the number of inputs at a high TTL input level times 1.6 mA; and the preferred method and limits are guaranteed.

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TABLE I. Electrical performance characteristics - Continued.

8/ This test is for qualification only. Ground bounce tests are performed on a nonswitching (quiescent) output and are used to measure the magnitude of induced noise caused by other simultaneously switching outputs. The test is performed on a low noise bench test fixture with all outputs fully dc loaded (I_{OL} maximum and I_{OH} maximum = i.e., ± 24 mA) and 50 pF of load capacitance (see figure 4). The loads must be located as close as possible to the device output. Inputs are then conditioned with 1 MHz pulse ($t_r = t_f$ =3.5.± 1.5 ns) switching simultaneously and in phase such that one output is forced low and all others (possible) are switched. The low level ground bounce noise is measured at the quiet output using a F.E.T. oscilloscope probe with at least 1 MΩ impedance. Measurement is taken from the peak of the largest positive pulse with respect to the nominal low level output voltage (figure 4). The device inputs are then conditioned such that the output under test is at a high nominal V_{OH} level. The high level ground bounce measurement is then measured from nominal V_{OH} level to the largest negative peak. This procedure is repeated such that all outputs are tested at a high and low level with a maximum number of outputs switching.

9/ See JEDEC Standard No. 17 for electrically induced latch-up test methods and procedures. The values listed for $V_{trigger}$, $I_{trigger}$, and V_{over}, are to be accurate within ± 5 percent.

10/ Tests shall be performed in sequence, attributes data only. Functional tests shall include the truth table and other logic patterns used for fault detection. Functional tests shall be performed in sequence as approved by the qualifying activity on qualified devices. H ≥ 2.5 V, L < 2.5 V; high inputs = 2.4 V and low inputs = 0.4 V. The input voltage levels have the allowable tolerances in accordance with MIL-STD-883 already incorporated.

11/ Device classes B and S are tested at V_{CC} = 4.5 V at T_C = +125°C for sample testing and at V_{CC} = 4.5 V at T_C = +25°C for screening. Other voltages of V_{CC} and temperatures are guaranteed, if not tested (see 4.4.1d).

12/ AC limits at V_{CC} = 5.5 V are equal to the limits at V_{CC} = 4.5 V and guaranteed by testing at V_{CC} = 4.5 V. Minimum ac limits for V_{CC} = 5.5 V are 1.0 ns and guaranteed by guardbanding the V_{CC} = 4.5 V minimum limits to 1.5 ns. For propagation delay tests, all paths must be tested.

Device types	01		02	
Case outlines	C and D	2	C and D	2
Terminal number	Terminal symbol			
1	CD1	NC	$\overline{SD1}$	NC
2	D1	CD1	Q1	CD1
3	CP1	D1	Q1	D1
4	SD1	CP1	GND	CP1
5	Q1	NC	Q2	NC
6	Q1	SD1	Q2	SD1
7	GND	NC	SD2	NC
8	Q2	Q1	CP2	Q1
9	Q2	Q1	D2	Q1
10	SD2	GND	CD2	GND
11	CP2	NC	V_{CC}	NC
12	D2	Q2	CD1	Q2
13	CD2	Q2	D1	Q2
14	V_{CC}	SD2	CP1	SD2
15	---	NC	---	NC
16	---	CP2	---	CP2
17	---	NC	---	NC
18	---	D2	---	D2
19	---	CD2	---	CD2
20	---	V_{CC}	---	V_{CC}

FIGURE 1. Terminal connections.

Device types 01 and 02					
Inputs				Outputs	
$\overline{SDn}$	$\overline{CDn}$	CP	Dn	Qn	$\overline{Qn}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q0	Q0

H = High voltage level
L = Low voltage level
X = Immaterial
* = This configuration is nonstable; that is, it will not persist when either preset (SDn) or clear (CDn) returns to its inactive state (high voltage level).
↑ = Low-to-high clock transition
Q0 (Q0) = Previous Qn (Qn) before low-to-high transition of clock

FIGURE 2. Truth table.

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Device types 01 and 02

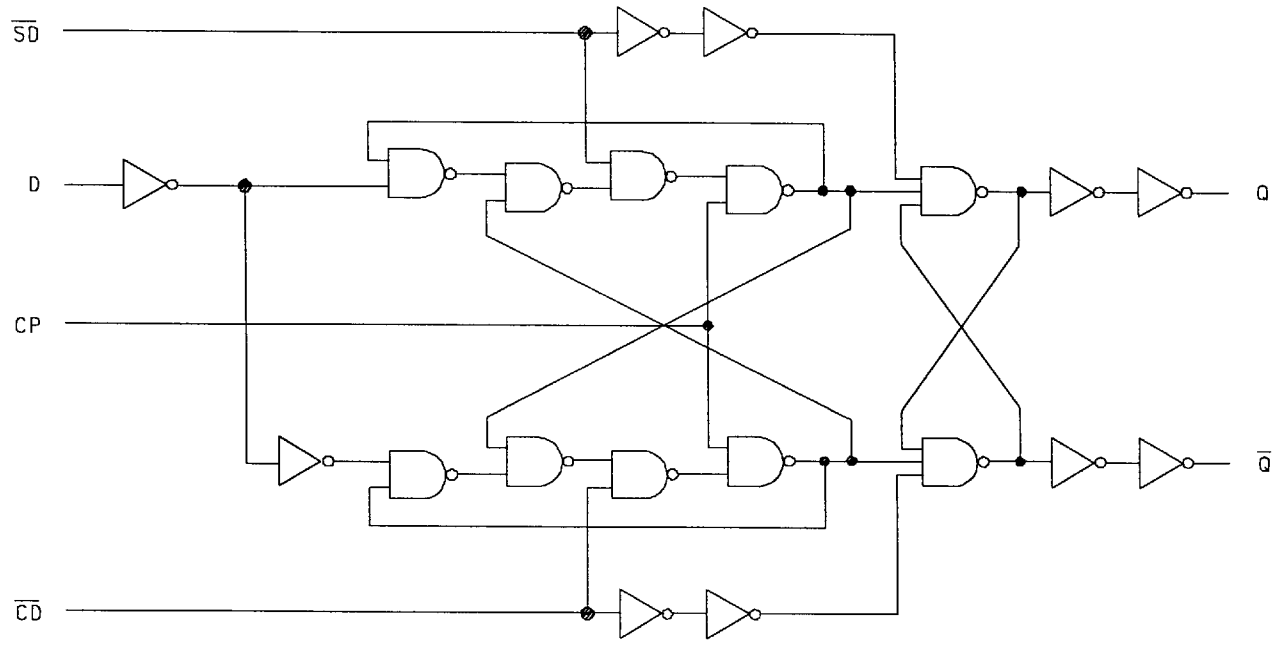
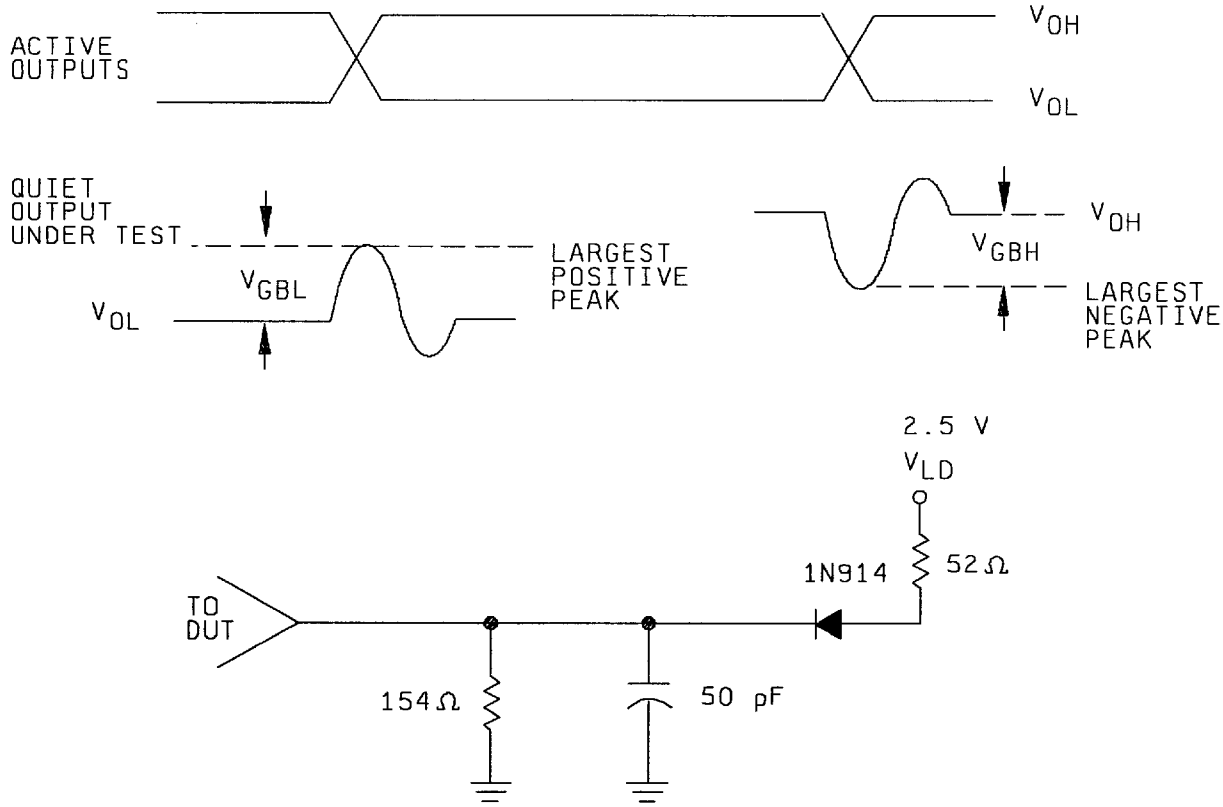


FIGURE 3. Logic diagram.



NOTE: Resistor and capacitor tolerances = ±10 percent.

FIGURE 4. Ground bounce waveforms and test circuit.

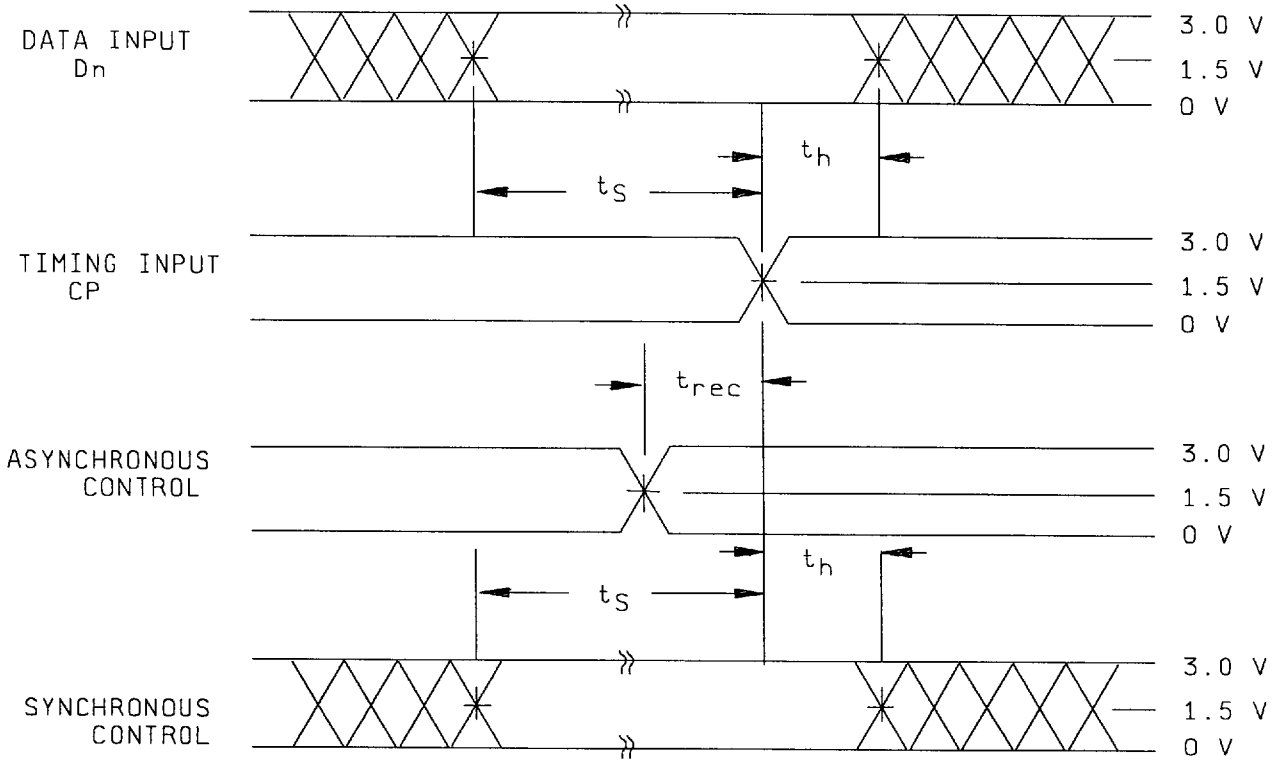
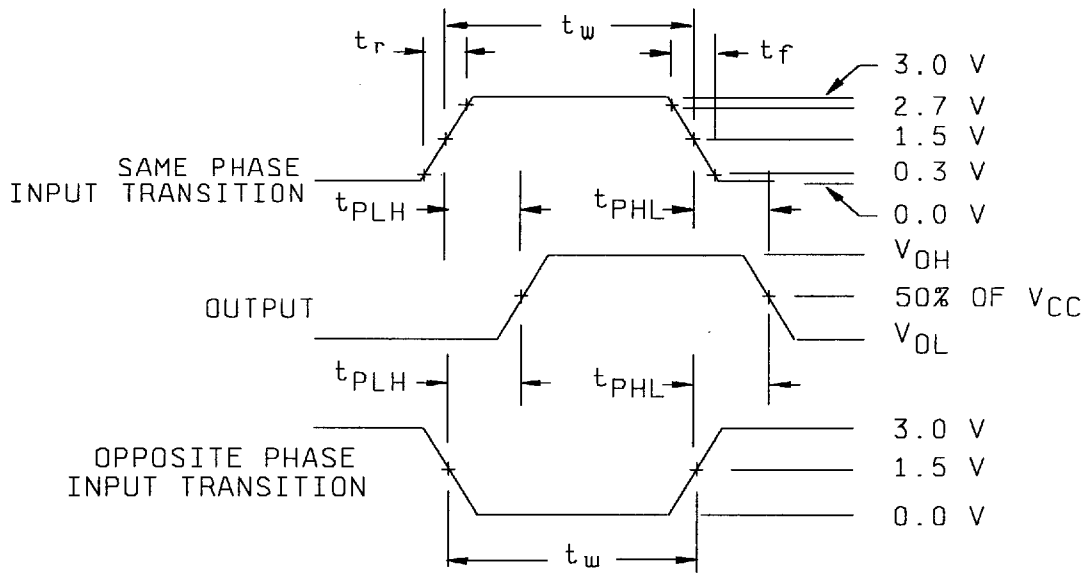
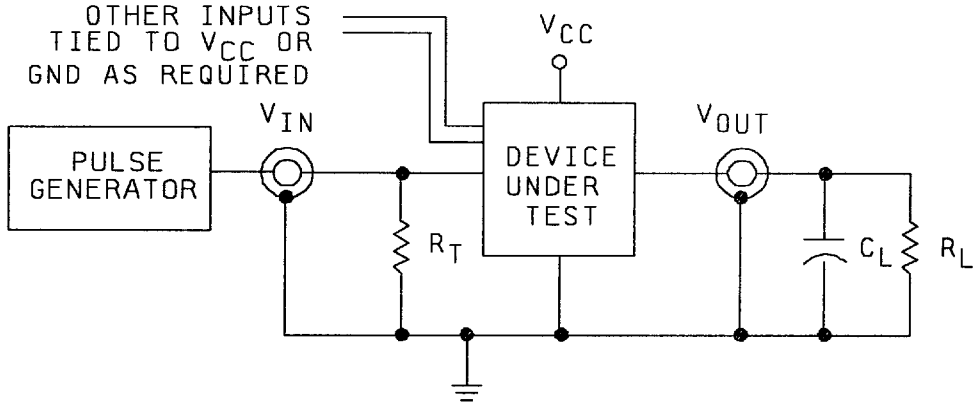


FIGURE 5. Switching waveforms and test circuit.





NOTES:
1. C_L = 50 pF minimum or equivalent (includes test jig and probe capacitance).
2. R_L = 500Ω or equivalent.
3. R_T = 50Ω or equivalent.
4. Input signal from pulse generator: V_{IN} = 0.0 V to 3.0 V; PRR ≤ 10 MHz; t_r ≤ 3 ns; t_f ≤ 3 ns; duty cycle = 50 percent.
5. Timing parameters shall be tested at a minimum input frequency of 1 MHz.

FIGURE 5. Switching waveforms and test circuit - Continued.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q, and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device classes M, B, and S, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.1.1 Burn-in and life test circuits. For device classes B and S, the burn-in and life test circuits shall be constructed so that the devices are stressed at the maximum operating conditions stated in 4.2.1a(5) or 4.2.1a(6) as applicable, or equivalent, as approved by the qualifying activity.

4.2 Screening. For device classes Q, and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device classes M, B, and S, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device classes M, B, and S.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

(3) Delete the sequence specified in 3.1.10 through 3.1.14 of method 5004 and substitute the first 7 test requirements of table II herein.

(4) For device class M, unless otherwise specified, the requirements for device class B in method 1015 of MIL-STD-883 shall be followed.

(5) Static burn-in, device classes B and S, test condition A, test method 1015 of MIL-STD-883. Test duration for each static test shall be 24 hours minimum for class S devices and in accordance with table I of method 1015 for class B devices.

(a) For static burn-in I, all inputs shall be connected to GND. Outputs may be open or connected to $V_{CC}/2 \pm 0.5$ V. Resistors R1 are optional on both inputs and open outputs, and required on outputs connected to $V_{CC}/2 \pm 0.5$ V. R1 = 220Ω to 47 kΩ.

(b) For static burn-in II, all inputs shall be connected through the R1 resistors to V_{CC}. Outputs may be open or connected to $V_{CC}/2 \pm 0.5$ V. Resistors R1 are optional on open outputs, and required on outputs connected to $V_{CC}/2 \pm 0.5$ V. R1 = 220Ω to 47 kΩ.

(c) V_{CC} = 5.5 V ± 0.5 V.

(6) Dynamic burn-in, device classes B and S, test condition D, method 1015 of MIL-STD-883,

(a) Input resistors = 220Ω to 2 kΩ ± 20 percent.

(b) Output resistors = 220Ω ± 20 percent.

(c) V_{CC} = 5.5 V ± 0.5 V.

(d) The $\overline{SDn}$ and $\overline{CDn}$ pins shall be connected through the resistors in parallel to V_{CC}. The clock inputs (CPn) shall be connected through resistors to a clock pulse (CP1). The data pins (D_n) shall be connected through resistors to a clock pulse (CP2). Outputs shall be connected through the resistors to $V_{CC}/2 \pm 0.5$ V.

(e) CP1, CP2 = 25 kHz to 1 MHz square wave; $f_{CP2} = f_{CP1}/2$; duty cycle = 50 percent ± 15 percent; V_{IH} = 4.5 V to V_{CC}, V_{IL} = 0 V ± 0.5 V; t_r, $t_f \leq 100$ ns.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. For class S devices, post dynamic burn-in, or class B devices, post static burn-in, electrical parameter measurements may, at the manufacturer's option, be performed separately or included in the final electrical parameter requirements.

4.2.2 Additional criteria for device classes Q, and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.2.3 Percent defective allowable (PDA).

a. The PDA for class S devices shall be 5 percent for static burn-in and 5 percent for dynamic burn-in, based on the exact number of devices submitted to each separate burn-in.

b. Static burn-in I and II failures shall be cumulative for determining the PDA.

c. The PDA for class B devices shall be in accordance with MIL-PRF-38535, appendix A for static burn-in. Dynamic burn-in is not required.

d. The PDA for class M devices shall be in accordance with MIL-PRF-38535 for static burn-in and dynamic burn-in.

e. Those devices whose measured characteristics, after burn-in, exceed the specified delta limits or electrical parameter limits specified in table I, subgroup 1, are defective and shall be removed from the lot. The verified number of failed devices times 100 divided by the total number of devices in the lot initially submitted to burn-in shall be used to determine the percent defective for the lot and the lot shall be accepted or rejected based on the specified PDA.

4.3 Qualification inspection.

4.3.1 Qualification inspection for device classes B and S. Qualification inspection for device classes B and S shall be in accordance with MIL-PRF-38535, appendix A. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.3.2 Qualification inspection for device classes Q, and V. Qualification inspection for device classes Q, and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.3.3 Electrostatic discharge sensitivity (ESDS) qualification inspection. ESDS testing shall be performed in accordance with MIL-STD-883, method 3015. ESDS testing shall be measured only for initial qualification and after process or design changes which may affect ESDS classification. For device classes B, S, Q, and V only, those device types that pass ESDS testing at 2,000 volts or greater shall be considered as conforming to the requirements of this specification.

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TABLE II. Electrical test requirements.

Test requirements	Subgroups 1/ (in accordance with MIL-STD-883, method 5005, table I)			Subgroups 1/ (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device 2/ class B	Device 2/ class S	Device class Q	Device class V
Interim electrical parameters, method 5004 (see 4.2)		1	1	1	1
Static burn-in I, method 1015 (see 4.2.1a)	3/	Not required	Required 4/	Not required	Required 4/
Interim electrical parameters, method 5004 (see 4.2.1b)			1 5/		1 5/
Static burn-in II, method 1015 (see 4.2.1a)	3/	Required 6/	Required 4/	Required 6/	Required 4/
Interim electrical parameters, method 5004 (see 4.2.1b)		1 2/ 5/	1 2/ 5/	1 2/ 5/	1 2/ 5/
Dynamic burn-in I, method 1015 (see 4.2.1a)	3/	Not required	Required 4/	Not required	Required 4/
Interim electrical parameters, method 5004 (see 4.2.1b)			1 5/		1 5/
Final electrical parameters, method 5004 (see 4.2)	1,2,3, 2/ 7,8,9	1,2, 2/ 6/ 7,9	1,2,7,9 2/	1,2,3, 2/ 6/ 7,8,9,10,11	1,2,3, 2/ 7,8,9,10,11
Group A test requirements method 5005 (see 4.4.1)	1,2,3,4,7, 8,9,10,11	1,2,3,4,7, 8,9,10,11	1,2,3,4,7, 8,9,10,11	1,2,3,4,7, 8,9,10,11	1,2,3,4,7, 8,9,10,11
Group B end point electrical parameters, method 5005 (see 4.4.2)			1,2,3,7, 5/ 8,9,10,11		
Group C end-point electrical parameters, method 5005 (see 4.4.3)	1,2,3	1,2 5/		1,2,3 5/	1,2,3,7 5/ 8,9,10,11
Group D end-point electrical parameters, method 5005 (see 4.4.4)	1,2,3	1,2	1,2,3	1,2,3	1,2,3
Group E end-point electrical parameters, method 5005 (see 4.4.5)	1,7,9	1,7,9	1,7,9	1,7,9	1,7,9

1/ Blank spaces indicate tests are not applicable.
2/ PDA applies to subgroup 1 (see 4.2.3). For device classes S and V, PDA applies to subgroups 1 and 7 (see 4.2.3).
3/ The burn-in shall meet the requirements of 4.2.1a herein.
4/ On all class S lots, the device manufacturer shall maintain read-and-record data (as a minimum on disk) for burn-in electrical parameters (group A, subgroup 1), in accordance with test method 5004 of MIL-STD-883. For pre-burn-in and interim electrical parameters the read-and-record requirements are for delta measurements only.
5/ Delta limits shall be required only on table I, subgroup 1. The delta values shall be computed with reference to the previous interim electrical parameters. The delta limits are specified in table III.
6/ The device manufacturer may at his option either complete subgroup 1 electrical parameter measurements, including delta measurements, within 96 hours after burn-in completion (removal of bias) or may complete subgroup 1 electrical measurements without delta measurements within 24 hours after burn-in completion (removal of bias). When the manufacturer elects to perform the subgroup 1 electrical parameter measurements without delta measurements, there is no requirement to perform the pre-burn-in electrical tests (first interim electrical parameters test in table II).

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TABLE III. Delta limits at +25°C

Parameters 1/	Device types	Limits
I_{CCH}, I_{CCL}	All	±100 nA

1/ These parameters shall be recorded before and after the required burn-in and life tests to determine delta limits.

4.4 Conformance inspection. Technology conformance inspection for classes Q, and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Technology conformance inspection for device classes M, B, and S shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device classes M, B, and S shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Latch-up and ground bounce tests are required for device classes B, S, Q, and V. These tests shall be performed only for initial qualification and after process or design changes which may affect the performance of the device. Latch-up tests shall be considered destructive. For latch-up and ground-bounce tests, test all applicable pins on five devices with zero failures.

c. C_{IN} and C_{PD} shall be measured only for initial qualification and after process or design changes which may affect capacitance. C_{IN} shall be measured between the designated terminal and GND at a frequency of 1 MHz. C_{PD} shall be tested in accordance with the latest revision of JEDEC Standard No. 20 and table I herein. For C_{IN} and C_{PD}, test all applicable pins on five devices with zero failures.

d. For device classes B and S, subgroups 9 and 11 tests shall be measured only for initial qualification and after process or design changes which may affect dynamic performance.

e. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes B and S, subgroups 7 and 8 tests shall be sufficient to verify the truth table as approved by the qualifying activity. For device classes Q, and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

f. For device classes M, B and S, f_{MAX} shall be measured only for initial qualification and after process or design changes which may affect the device frequency. Test all applicable pins on 22 devices with zero failures.

g. For device classes M, B and S, t_s, t_h, t_{rec}, and t_w shall be guaranteed, if not tested, to the limits specified in table I.

4.4.2 Group B inspection. The group B inspection end-point electrical parameters shall be as specified in table II herein. For device class S steady-state life tests, the test circuit shall be submitted to the qualifying activity.

4.4.3 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.3.1 Additional criteria for device class M and B. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C or D. For device class M, the test circuit shall maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device class B, the test circuit shall be submitted to the qualifying activity. For device classes M and B, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

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b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

d. End-point electrical parameters shall be as specified in table II herein. Delta limits shall apply only to subgroup 1 of group C inspection and shall consist of tests specified in table III herein.

e. For device class M, unless otherwise noted, the requirements for device class B in method 1005 of MIL-STD-883 shall be followed.

4.4.3.2 Additional criteria for device classes Q, and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-PRF-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.4 Group D inspection. Group D inspection shall be in accordance with table IV of method 5005 of MIL-STD-883. End-point electrical parameters shall be as specified in table II herein.

4.4.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. For device classes B and S, subgroups 1 and 2 in table V, method 5005 of MIL-STD-883 shall be tested as appropriate for device construction.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

d. RHA tests for device classes M, B and S for levels M, D, L, R, F, G, and H shall be performed through each level to determine at what levels the devices meet the RHA requirements. These RHA tests shall be performed for initial qualification and after design or process changes which may affect the RHA performance of the device.

e. Prior to irradiation, each selected sample shall be assembled in its qualified package. It shall pass the specified group A electrical parameters in table I for subgroups specified in table II herein.

f. For device classes Q, and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device classes M, B, and S, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

4.4.5.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883, method 1019, and as specified herein:

Prior to and during total dose irradiation characterization and testing, the devices for characterization shall be biased so that 50 percent are at inputs high and 50 percent are at inputs low, and the devices for testing shall be biased to the worst case condition established during characterization. Devices shall be biased as follows:

1. Inputs tested high, V_{CC} = 5.5 V dc +5%, R_{CC} = 10Ω +20%, V_{IN} = 5.0 V dc +5%, R_{IN} = 1 kΩ +20%, and all outputs are open.

2. Inputs tested low, V_{CC} = 5.5 V dc +5%, R_{CC} = 10Ω +20%, V_{IN} = 0.0 V dc, R_{IN} = 1 kΩ +20%, and all outputs are open.

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4.4.5.1.1 Accelerated aging test. Accelerated aging shall be performed on class M, B, S, Q, and V devices requiring an RHA level greater than 5K rads (Si). The post-anneal end point electrical parameter limits shall be as specified in table I herein and shall be the preirradiation end point electrical parameter limit at 25°C ± 5°C. Testing shall be performed at initial qualification and after any design or process changes which may effect the RHA response of the device.

4.5 Methods of inspection. Methods of inspection shall be specified as follows.

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit GND terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q, and V or MIL-PRF-38535, appendix A for device classes M, B, and S.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device classes B and Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q, and V. Sources of supply for device classes Q, and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device classes M, B and S. Approved sources of supply for classes M, B and S are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

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APPENDIX

10. SCOPE

10.1 Scope. This appendix contains the PIN substitution information to support the one part-one part number system. For new designs, after the date of this document the new PIN shall be used in lieu of the old PIN. For existing designs prior to the date of this document the new PIN can be used in lieu of the old PIN. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance. The PIN substitution data shall be as follows.

20. APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

30. SUBSTITUTION DATA

New PIN	Old PIN
5962-8752501MCX	5962-8752501CX
5962-8752501MDX	5962-8752501DX
5962-8752501M2X	5962-87525012X
5962-8752502MCX	5962-8752502CX
5962-8752502MDX	5962-8752502DX
5962-8752502M2X	5962-87525022X

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 97-10-16

Approved sources of supply for SMD 5962-87525 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 during the next revision. MIL-HDBK-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8752501MCX	01295 27014	SNJ54ACT74J 54ACT74DMQB
5962-8752501MDX	01295 27014	SNJ54ACT74W 54ACT74FMQB
5962-8752501M2X	01295 27014	SNJ54ACT74FK 54ACT74LMQB
5962-8752502MCX	3/	SNJ54ACT11074J
5962-8752502M2X	3/	SNJ54ACT11074FK
5962R8752501SCA	27014	JM54ACT74SCA-RH
5962R8752501SDA	27014	JM54ACT74SDA-RH
5962R8752501S2A	27014	JM54ACT74S2A-RH
5962R8752501BCA	27014	JM54ACT74BCA-RH
5962R8752501BDA	27014	JM54ACT74BDA-RH
5962R8752501B2A	27014	JM54ACT74B2A-RH

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ No longer available from an approved supplier.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Incorporated 17500 N. Central Expressway P.O. Box 655303 Dallas, TX 75265 Point-of-contact: I-20 at FM 1788 Midland, TX 79711-0448
27014	National Semiconductor 2900 Semiconductor Drive P.O. Box 58090 Santa Clara, CA 95052-8090 Point-of-contact: 5 Foden Road South Portland, ME 04106

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.