REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																								
SHEET																								
REV																								
SHEET																								
REV STATUS OF SHEETS	REV																							
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20			

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE: 22 September 1988

REVISION LEVEL:

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, DIGITAL, CMOS, 2K x 8
REGISTERED UVEPROM, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-87529

SHEET 1 OF 20

DESC FORM 193
SEP 87

* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60911

5962-E289

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

5962-87529	01	L	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Setup time
01	See 6.4	2K x 8 registered UVEPROM	45 ns
02	See 6.4	2K x 8 registered UVEPROM	35 ns

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
K	F-6 (24-lead, .640" x .420" x .90" max), flat package 1/
L	D-9 (24-lead, 1.280" x .310" x .200"), dual in-line package 1/
3	C-4 (28-terminal, .460" x .460" x .100" max), square chip carrier package 1/

1.3 Absolute maximum ratings. 2/

Supply voltage range (V_{CC})	-0.5 V dc to +7 V dc
DC voltage applied to outputs in high Z state	-0.5 V dc to +7 V dc
DC program voltage	14.0 V dc
DC input voltage	-3.0 V dc to +7 V dc
Maximum power dissipation (P_D) 3/	1.0 W
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Junction temperature (T_J) 4/	+150°C
Thermal resistance, junction to case (θ_{JC})	See MIL-M-38510, appendix C

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	+4.5 V dc to 5.5 V dc
Case operating temperature range (T_C)	-55°C to +125°C

1/ Lid shall be transparent to permit ultraviolet erasure.
2/ Unless otherwise specified, all voltages are referenced to ground.
3/ Must withstand the add P_D due to short circuit test, e.g., I_{OS}.
4/ Maximum junction temperature may be increased to +175°C during burn-in and steady-state life.

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table. The truth table shall be as specified on figure 2.

3.2.2.1 Unprogrammed or erased devices. The truth table for unprogrammed devices shall be as specified on figure 2.

3.2.2.2 Programmed devices. The requirements for supplying programmed devices are not part of this drawing.

3.2.3 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C < T_C < +125°C$, GND = 0 V, $4.5 V < V_{CC} < 5.5 V$ unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Input leakage current	I_{IX}	V_{IN} = 5.5 V and GND	1,2,3	All	-10	+10	µA
Output leakage current 1/	I_{LO}	V_{OUT} = 5.5 V and GND output disabled	1,2,3	All		±40	µA
Operating supply current (active)	I_{CC}	$\overline{E}/E_S = V_{IL}$, $\overline{INIT} = V_{IH}$, addresses cycling between 0 V and 3 V. $f = 1/2t_{pwc}$	1,2,3	All		120	mA
Input low voltage 2/	V_{IL}	V_{CC} = 4.5 V and 5.5 V	1,2,3	All		0.8	V
Input high voltage 2/	V_{IH}	V_{CC} = 4.5 V and 5.5 V	1,2,3	All	2.0		V
Output low voltage	V_{OL}	I_{OL} = 16 mA, V_{IH} = 2.0 V, V_{CC} = 4.5 V, V_{IL} = 0.8 V	1,2,3	All		0.4	V
Output high voltage	V_{OH}	I_{OH} = -4 mA, V_{IH} = 2.0 V, V_{CC} = 4.5 V, V_{IL} = 0.8 V	1,2,3	All	2.4		V
Output short circuit current 3/ 4/	I_{OS}	V_O = GND	1,2,3	All	-20	-90	mA
Input capacitance 4/	C_{IN}	f = 1.0 MHz, T_C = +25°C, see 4.3.1d, V_{CC} = 5.5 V; V_{IN} = 0 V	4	All		5	pF
Output capacitance 4/	C_{OUT}	f = 1.0 MHz, T_C = +25°C, see 4.3.1d, V_{CC} = 5.5 V; V_{OUT} = 0 V	4	All		8	pF
Address setup to clock high	t_{SA}	See figures 3 and 4 as applicable	9,10,11	01	45		ns
			9,10,11	02	35		ns
Address hold from clock high	t_{HA}		9,10,11	01,02	0		ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ GND = 0 V $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Clock high to valid output	t_{CO}	See figures 3 and 4 as applicable	9,10,11	01		25	ns
				02		15	
Clock pulse width 4/	t_{PWC}		9,10,11	01, 02	20		ns
($\overline{E}_S$) setup to clock high 4/	t_{SE_S}		9,10,11	01, 02	15		ns
($\overline{E}_S$) hold from clock high 4/	t_{HE_S}		9,10,11	01, 02	5		ns
Delay from $\overline{INIT}$ to valid output 4/	t_{DI}		9,10,11	01		35	ns
				02		20	
$\overline{INIT}$ recovery to clock high 4/	t_{RI}		9,10,11	01,02	20		ns
$\overline{INIT}$ pulse width 4/	t_{PWI}		9,10,11	01	25		ns
				02	20		
Valid output from clock high 4/ 5/	t_{COS}		9,10,11	01		30	ns
				02		20	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ GND = 0 V 4.5 V $\le V_{CC} \le$ 5.5 V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Inactive output from clock high 4/ 5/ 6/	t_{HZC}	See figures 3 and 4 as applicable	9,10,11	01		30	ns
				02		20	
Valid output from $\overline{E}$ low 4/ 7/	t_{DOE}		9,10,11	01		30	ns
				02		20	
Inactive output from $\overline{E}$ high 4/ 6/ 7/	t_{HZE}		9,10,11	01		30	ns
				02		20	

1/ For devices using the synchronous enable, the device must be clocked after applying these voltages to perform this measurement.
2/ These are absolute voltages with respect to device ground pin and include all overshoots due to system or tester noise.
3/ For test purposes, not more than one output at a time should be shorted. Short-circuit test duration should not exceed 30 seconds.
4/ This parameter tested initially and after any design or process changes which could affect this parameter, therefore, shall be guaranteed to the limits specified in table I.
5/ Applies only when the synchronous (E_S) function is used.
6/ Transition is measured at steady-state high level -500 mV or steady-state low level +500 mV on the output from the 1.5 V level on the input with loads shown on figure 3B.
7/ Applies only when the asynchronous ($\overline{E}$) function is used.

3.5 Processing EPROMS. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.5.1 Erasure of EPROMS. When specified, devices shall be erased in accordance with the procedures and characteristics specified in 4.5.

3.5.2 Programmability of EPROMS. When specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified in 4.6.

3.5.3 Verification of erasure of programmed EPROMS. When specified, devices shall be verified as either programmed to a specified program, or erased. As a minimum, verification shall consist of performing a functional test (subgroup 7) to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure, and shall be removed from the lot.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition C or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

c. The percent defective allowable (PDA) shall be as specified in MIL-M-38510.

d. A data retention stress shall be included as part of the screening procedure and shall consist of the following steps:

Margin test method A.

(1) At +25°C, program greater than 95 percent of the bit locations, including the slowest programming cell. The remaining bits shall provide a worse case speed pattern.

(2) Bake, unbiased, for 72 hours at +140°C, for 32 hours at +150°C, or for 8 hours at +200°C.

(3) At +25°C, perform a margin test using V_m = +4.0 V to loose timing (i.e., T_{AA} = 1 µs).

(4) Perform dynamic burn-in in accordance with 4.2a.

(5) At +25°C, perform a margin test using V_m = +4.0 V.

(6) Perform electrical test in accordance with 4.2b.

(7) Erase in accordance with 3.5.1. Devices may be submitted to quality conformance inspection.

(8) Verify erasure in accordance with 3.5.3.

TABLE II. Electrical test requirements. 1/ 2/ 3/ 4/ 5/

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*,2,3,7*,8,9, 10,11
Group A test requirements (method 5005)	1,2,3,4**,7***, 8***,9,10,11
Groups C and D end-point electrical parameters (method 5005)	2,3,7,8

1/ * PDA applies to subgroups 1, 7, and 9 (see 4.2c).
2/ ** See 4.3.1d.
3/ ***See 4.3.1e.
4/ Any subgroups at the same temperature may be combined when using a multifunction tester.
5/ For all electrical tests, the device shall be programmed to the pattern specified.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. All devices selected for testing shall be programmed with a checkerboard pattern, or equivalent. After completion of all testing, the devices shall be erased and verified except devices being submitted to groups B, C, and D testing.

d. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance.

e. As a minimum, subgroups 7 and 8 shall consist of verifying the EPROM pattern specified.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition C or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

c. All devices submitted for testing shall be programmed with a checkerboard pattern, or equivalent. After completion of all testing, the devices shall be erased and verified.

4.4 Electrostatic discharge sensitivity inspection. Electrostatic discharge sensitivity (ESDS) testing shall be performed in accordance with MIL-STD-883, method 3015 and MIL-M-38510. The option to categorize devices as ESD sensitive without performing the test is not allowed. Only those device types that pass ESDS testing at 1,000 volts or greater shall be considered as conforming to the requirements of this drawing. ESDS testing shall be measured only for initial inspection and after process or design changes which may affect ESDS classification.

4.5 Erasing procedure. The recommended erasure procedure for the device is exposure to shortwave ultraviolet light which has a wavelength of 2537 angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 25 Ws/cm^2. The erasure time with this dosage is approximately 35 minutes using an ultraviolet lamp with a 12000 $\mu W/cm^2$ power rating. The device should be placed within one inch of the lamp tubes during erasure. The maximum integrated dose the device can be exposed to without damage is 7258 Ws/cm^2 (1 week at 12000 $\mu W/cm^2$). Exposure of device to high intensity UV light for long periods may cause permanent damage.

4.6 Programming procedure method A. The programming characteristics in table III and the following procedures shall be used for programming the device:

a. An unprogrammed device contains neither ones nor zeros because of the differential cell used for high speed. To verify that a PROM is unprogrammed, use the two blank check modes provided on figure 2, method A. As the unprogrammed device contains neither ones nor zeros, it is neccessary to program both ones and zeros.

b. Programming is accomplished by applying power to the device with pins CP, $\overline{E}/\overline{E_S}$, and $\overline{INIT}$ at V_{IHP}.

c. In accordance with figure 4A, method A, take pin $\overline{INIT}$ to V_{PP}. The device is now in the program inhibit mode of operation with the output lines in a high impedance state.

d. In accordance with figure 4A, method A, address, program, and verify one byte of data.

e. Repeat this procedure for each location to be programmed.

f. If the "brute force" programming method is used, the pulse width of the program pulse should be 10 ms, and each location is programmed with a single pulse. Any location that fails to verify causes the device to be rejected.

g. If the intelligent programming technique is used (figure 5, method A), the program pulse width should be 100 µs. Each location is ultimately programmed and verified until it verifies correctly up to and including 4 times. When the location verifies, one or more additional programming pulses should be applied of duration equal to 24 times the sum of the previous programming pulses before advancing to the next address to repeat the process.

4.6.1 Programming the initialize byte. The initialize byte in the erased state is "0" or low. This byte is programmed (figure 4B) by the addition of V_{PP} to A_1, and V_{ILP} on A_2. Verification of the initialize byte is accomplished by performing an initialize function.

4.6.2 Programming synchronous enable.

a. The device is delivered in an asynchronous mode of operation and requires programming for synchronous operation only.

b. In accordance with figure 4C address the synchronous enable byte by applying V_{PP} to A_1, and V_{IHP} on A_2.

c. Programming the cell is accomplished with a 10 ms program pulse on pin CP but does not require any data as there is no choice as to how synchronous enable may be programmed, only if it is to be programmed.

Terminal connections		
Device	01-02	
Case	L, K	3
Terminal number		
1	A_7	NC
2	A_6	A_7
3	A_5	A_6
4	A_4	A_5
5	A_3	A_4
6	A_2	A_3
7	A_1	A_2
8	A_0	A_1
9	O_0	A_0
10	O_1	NC
11	O_2	O_0
12	GND	O_1
13	O_3	O_2
14	O_4	GND
15	O_5	NC
16	O_6	O_3
17	O_7	O_4
18	CP	O_5
19	$\overline{E}/\overline{E}_S$	O_6
20	$\overline{INIT}$	O_7
21	A_{10}	NC
22	A_9	CP
23	A_8	$\overline{E}/\overline{E}_S$
24	V_{CC}	$\overline{INIT}$
25	---	A_{10}
26	---	A_9
27	---	A_8
28	---	V_{CC}

FIGURE 1. Terminal connections.

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Mode	Pin function						
	Read or output disable	A_2	CP	$\overline{E}/\overline{E_S}$	$\overline{INIT}$	A_1	Outputs
	Other	A_2	$\overline{PGM}$	$\overline{VFY}$	Vpp	A_1	Outputs
Read 2/ 3/		X	X	V_{IL}	V_{IH}	X	Data out
Output disable 5/		X	X	V_{IH}	V_{IH}	X	High Z
Program 1/ 4/		X	V_{ILP}	V_{IHP}	Vpp	X	Data in
Program verify 1/ 4/		X	V_{IHP}	V_{ILP}	Vpp	X	Data out
Program inhibit 1/ 4/		X	V_{IHP}	V_{IHP}	Vpp	X	High Z
Intelligent program 1/ 4/		X	V_{ILP}	V_{IHP}	Vpp	X	Data in
Program synch enable 4/		V_{IHP}	V_{ILP}	V_{IHP}	Vpp	Vpp	High Z
Program initial byte 4/		V_{ILP}	V_{ILP}	V_{IHP}	Vpp	Vpp	Data in
Blank check ones 1/ 4/		X	Vpp	V_{ILP}	V_{ILP}	X	Ones
Blank check zeros 1/ 4/		X	Vpp	V_{IHP}	V_{ILP}	X	Zeros

1/ X = Don't care, but not to exceed V_{PP}.

2/ During read operation, the output latches are loaded on a "0" to "1" transition of CP.

3/ In the synchronous mode, pin $\overline{E}_S$ must be low prior to the "0" to "1" transition on CP that loads the register.

4/ During programming and verification, all unspecified pins to be at V_{ILP}.

5/ In the synchronous mode, pin $\overline{E}_S$ must be high prior to the "0" to "1" transition on CP that loads the register.

FIGURE 2. Truth table.

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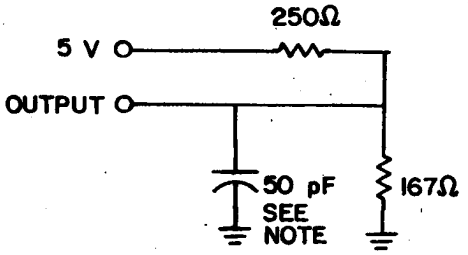
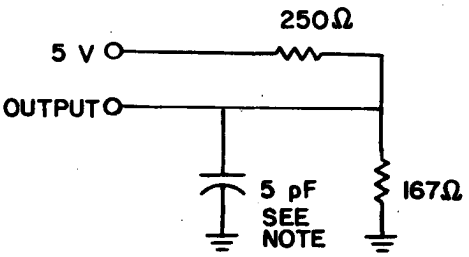


NOTE: (Minimum) including jig and scope

FIGURE 3A. Output load circuit (C_L = 50 pF) or equivalent.



NOTE: (Minimum) including jig and scope

FIGURE 3B. Output load circuit (C_L = 5 pF) or equivalent.

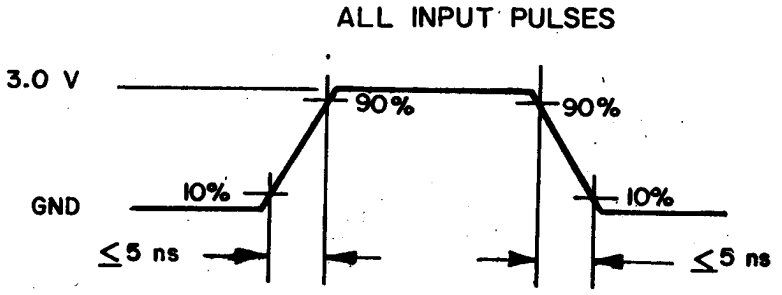
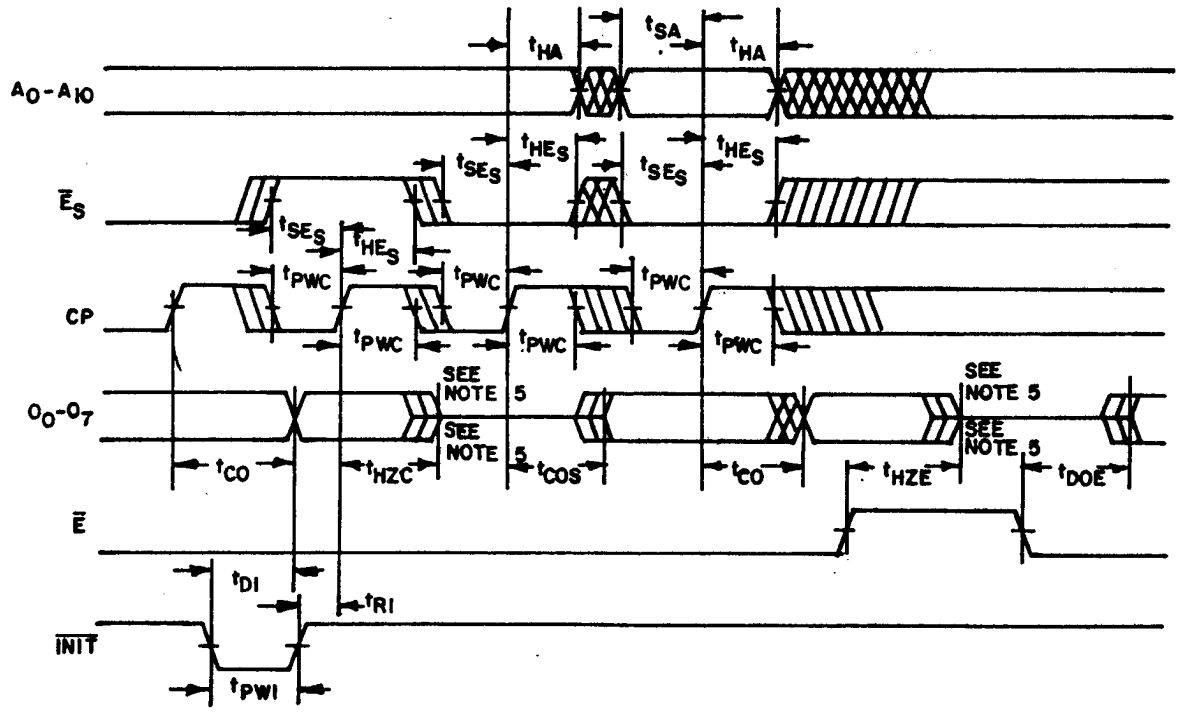


FIGURE 4. Switching waveforms.



NOTES:
1. Ensure that adequate decoupling capacitance is employed accross the device V_{CC} and ground terminals. Multiple capacitors are recommended, including a 0.1 µF or larger capacitor and a 0.01 µF or smaller capacitor, placed as close to the device terminals as possible. Inadequate decoupling may result in large variations of power supply voltage, creating erroneous function or transient performance failures.
2. Do not leave any inputs disconnected (floating) during any tests.
3. Do not attempt to perform threshold tests under ac conditions. Large amplitude fast ground current transients normally occur as the device outputs discharge the load capacitances. These transients flowing through the parasitic inductance between the device ground pin and the test system ground can create significant reductions in observable input noise immunity.
4. Output levels are measured at 1.5 V reference levels.
5. Transition is measured at steady-state HIGH level -500 mV or steady-state LOW level +500 mV on output from the 1.5 V level on inputs with load shown on figure 3B.
6. Tests are performed with rise and fall times of 5 ns or less.
7. See figure 3A for all switching characteristics except t_{HZC} and t_{HZE}.
8. See figure 3B for t_{HZC} and t_{HZE}.
9. All device test loads should be located within 2 inches of device outputs.

FIGURE 4. Switching waveforms - Continued.

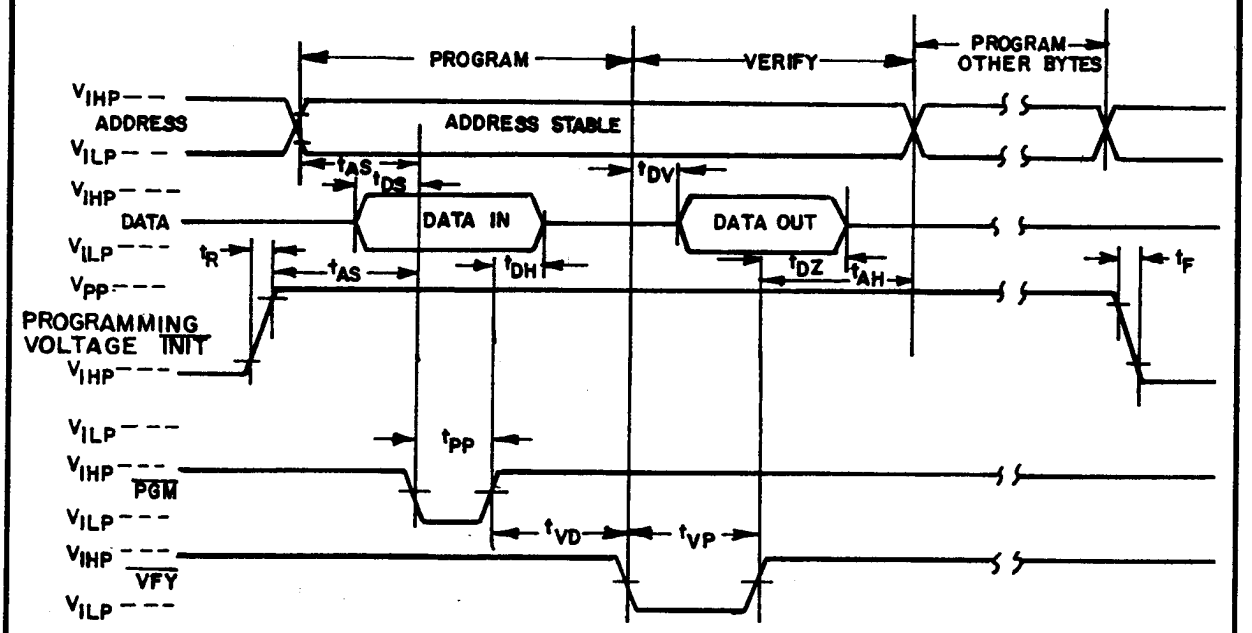


FIGURE 4A. PROM programming waveforms.

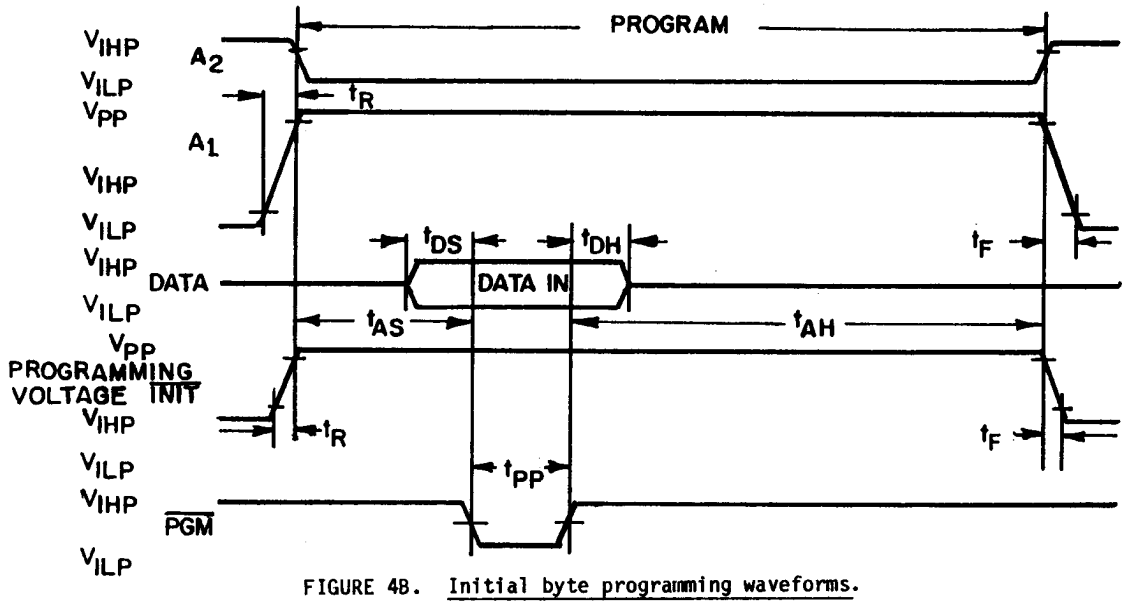


FIGURE 4B. Initial byte programming waveforms.

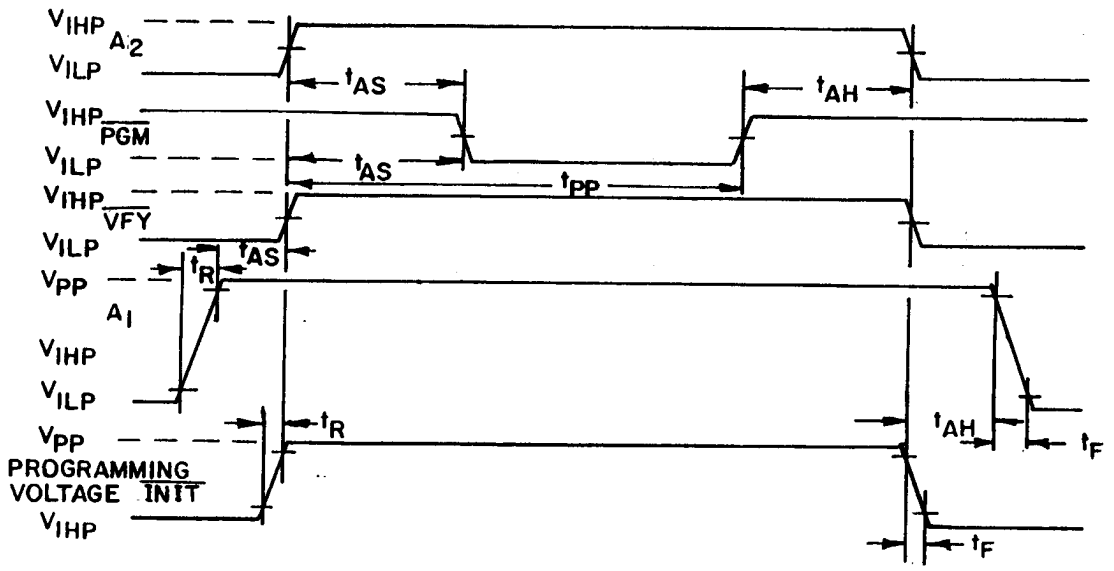


FIGURE 4C. Program synchronous enable.

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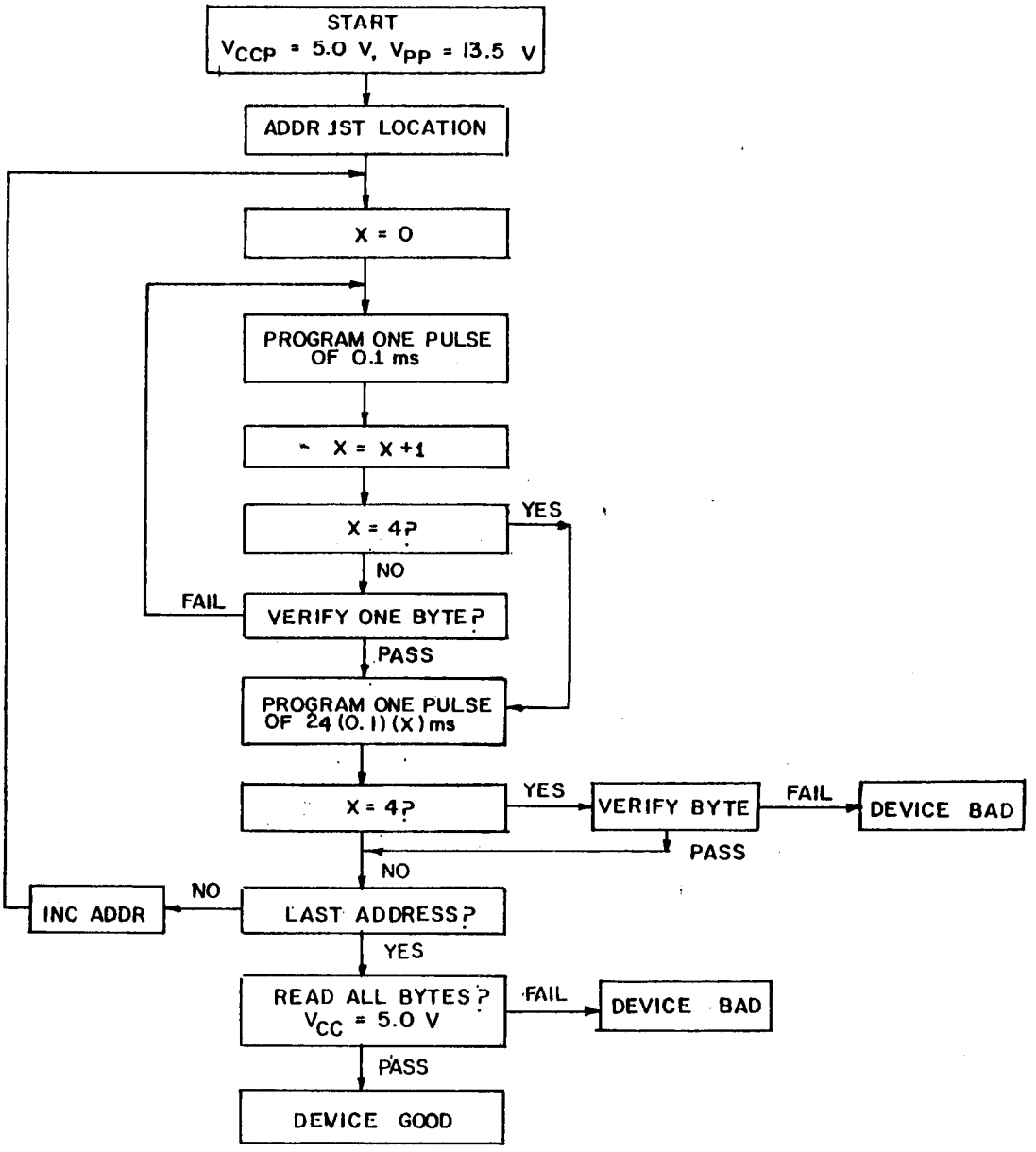

FIGURE 5. Fast programming flowchart, method A.

TABLE III. Programming characteristics for method A.

Parameter	Symbol	Conditions T_C = +25°C ±5°C, V_{CC} = 5.0 V ±0.5 V, V_{PP} = 13.5 V ±0.5 V	Limits		Unit
			Min	Max	
Programming voltage 1/	V_{PP}		13.0	14.0	V
Supply voltage	V_{CCP}		4.75	5.25	V
Input high voltage	V_{IHP}		3.0		V
Input low voltage	V_{ILP}			0.4	V
Output high voltage	V_{OH}	2/	2.4		V
Output low voltage	V_{OL}	2/		0.4	V
Programming supply current	I_{PP}			50.0	mA
Programming pulse width 3/	t_{PP}		100	10,000	µs
Address setup time	t_{AS}		1.0		ns
Data setup time	t_{DS}		1.0		µs
Address hold time	t_{AH}		1.0		µs
Data hold time	t_{DH}		1.0		µs
V_{PP} rise and fall time 3/	t_R, t_F		1.0		µs
Delay to verify	t_{VD}		1.0		ns
Verify pulse width	t_{VP}		2.0		µs

See footnotes at end of table.

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TABLE III. Programming characteristics for method A - Continued.

Parameter	Symbol	Conditions T_C = 25°C ±5°C, V_{CC} = 5.0 V ±0.5 V, V_{PP} = 13.5 V ±0.5 V	Limits		Unit
			Min	Max	
Verify data valid	t_{DV}			1.0	µs
Verify high to high Z	t_{DZ}			1.0	ns

1/ V_{CCP} must be applied prior to V_{PP}.
2/ During verify operation.
3/ Measured at 10 percent and 90 percent points.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.4 Approved source of supply. An approved source of supply is listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/
5962-8752901LX	65786 66579	CY7C245-45WMB WS57C45-45TMB
5962-8752901KX	65786 66579	CY7C245-45TMB WS57C45-45FMB
5962-87529013X	65786 66579	CY7C245-45QMB WS57C45-45CMB
5962-8752902LX	65786 66579	CY7C245-35WMB WS57C45-35TMB
5962-8752902KX	65786 66579	CY7C245-35TMB WS57C45-35FMB
5962-87529023X	65786 66579	CY7C245-35QMB WS57C45-35CMB

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
65786	Cypress Semiconductor Corporation 3901 North First Street San Jose, CA 95134
66579	WaferScale Intetration Incorporated 47280 Kato Road Freemont, CA 94538

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