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LTR	DESCRIPTION	DATE	APPROVED

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Defense Electronics Supply Center
Dayton, Ohio

Original date of drawing:

26 August 1987

AMSC N/A

PREPARED BY
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CHECKED BY
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APPROVED BY
MC Leach

SIZE
A

CODE IDENT. NO.
67268

REV

MILITARY DRAWING

This drawing is available for use by all Departments and Agencies of the Department of Defense

TITLE: MICROCIRCUITS, PROGRAMMABLE COMMUNICATION INTERFACE, MONOLITHIC SILICON

DWG NO. 5962-87548

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5962-E372

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

DESC FORM 193
MAY 86

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

5962-87548	01	X	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	8251A	Programmable communication interface
02	8251A	Programmable communication interface

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
X	D-10 (28-lead, 1/2" x 1 3/8"), dual-in-line package
3	C-4 (28-terminal, .450" x .450"), square chip carrier package

1.3 Absolute maximum ratings.

Supply voltage range	-0.5 V dc to +7.0 V dc
Input voltage range	-0.5 V dc to +7.0 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D)	1.0 W
Lead temperature (soldering, 5 seconds)	+270°C
Thermal resistance, junction-to-case (θ_{JC}):	
Case X 1/	15°C/W
Case 3 1/	60°C/W
Junction temperature (T_J)	+150°C
V_{CC} with respect to V_{SS}	-0.5 V dc to +7.0 V dc
All signal voltages with respect to V_{SS}	-0.5 V dc to +7.0 V dc

1.4 Recommended operation conditions.

Supply voltage (V_{CC}):	
Device type 01	4.5 V dc to 5.5 V dc
Device type 02	4.75 V dc to 5.25 V dc
Minimum high level input voltage (V_{IH})	2.2 V dc
Maximum high level input voltage (V_{IH})	V_{CC}
Maximum low level input voltage (V_{IL})	0.8 V dc
Minimum low level input voltage (V_{IL})	-0.5 V dc
Case operating temperature range (T_C)	-55°C to +125°C

1/ When a thermal resistance value for this case is included in MIL-M-38510, appendix C, that value shall supersede the value indicated herein.

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table. The truth table shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

3.2.4 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full recommended case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C < T_C < +125°C$ V_{CC} = 5 V ±10% for device type 01 V_{CC} = 5 V ±5% for device type 02	Group A subgroups	Limits		Unit
				Min	Max	
Input low voltage	V_{IL}		1, 2, 3		.8	V
Input high voltage	V_{IH}		1, 2, 3	2.2		V
Output low voltage	V_{OL}	I_{OL} = 2.2 mA	1, 2, 3		.45	V
Output high voltage	V_{OH}	I_{OH} = -400 µA	1, 2, 3	2.4		V
Output float leakage current	I_{OFL}	V_{OUT} = 5.5 V and 0.45 V	1, 2, 3		+10 -10 1/	µA
Input leakage current	I_{IL}	V_{IN} = 5.5 V and 0.45 V	1, 2, 3		+10 -10 1/	µA
Power supply current	I_{CC}	Outputs unloaded static 2/	1, 2, 3		120	mA
Input capacitance	C_{IN}	F_C = 1 MHz See 4.3.1c	4		10	pF
I/O capacitance	$C_{I/O}$	Unmeasured pins returned to GND See 4.3.1c	4		20	pF
Functional tests		See 4.3.1d	7, 8			
READ CYCLE						
Address stable before $\overline{READ}$	t_{AR}	See figure 4 3/ 4/ 5/	9, 10, 11	0		ns
Address hold time to $\overline{READ}$	t_{RA}	See figure 4 3/ 4/ 5/	9, 10, 11	0		ns
$\overline{READ}$ pulse width	t_{RR}	See figure 4 3/ 4/	9, 10, 11	250		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = 5 V ±10% for device type 01 V_{CC} = 5 V ±5% for device type 02	Group A subgroups	Limits Min	Limits Max	Unit
Data delay from $\overline{READ}$	t_{RD}	See figure 4 3/ 4/ 6/ 7/	9, 10, 11		200	ns
$\overline{READ}$ to data floating	t_{DF}	See figure 4 3/ 4/	9, 10, 11	10 1/	250	ns
WRITE CYCLE						
Address stable before $\overline{WRITE}$	t_{AW}	See figure 4 3/ 4/	9, 10, 11	0		ns
Address hold time to $\overline{WRITE}$	t_{WA}	See figure 4 3/ 4/	9, 10, 11	20		ns
$\overline{WRITE}$ pulse width	t_{WW}	See figure 4 3/ 4/	9, 10, 11	250		ns
Data setup for $\overline{WRITE}$	t_{DW}	See figure 4 3/ 4/	9, 10, 11	150		ns
Data hold for $\overline{WRITE}$	t_{WD}	See figure 4 3/ 4/	9, 10, 11	20		ns
Recovery time between $\overline{WRITE}$	t_{RV}	See figure 4 3/ 4/ 8/	9, 10, 11	6 1/		t_{CY}
OTHER TIMINGS						
Clock period 9/	t_{CY}	See figure 4 3/ 4/ 10/ 11/	9, 10, 11	320	1350	ns
Clock high pulse width	t_{HO}	See figure 4 3/ 4/	9, 10, 11	140	t_{CY} -90 12/	ns
Clock low pulse width	t_{LO}	See figure 4 3/ 4/	9, 10, 11	90		ns
TxD delay from falling edge of TxC	t_{DTX}	See figure 4 3/ 4/	9, 10, 11		1	µs
Transmitter input clock frequency	f_{TX}	1 x Baud rate 3/ 4/	9, 10, 11	1/ dc	64	kHz
		16 x Baud rate		1/ dc	310	kHz
		64 x Baud rate		1/ dc	615	kHz

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C < T_C < +125°C$ V_{CC} = 5 V ±10% for device type 01 V_{CC} = 5 V ±5% for device type 02		Group A subgroups	Limits		Unit
					Min	Max	
Transmitter input clock pulse width	t_{TPW}	1 x Baud rate	3/ 4/	9, 10, 11	12		t_{CY}
		16 x Baud rate	See figure 4		1		
		64 x Baud rate			1		
Transmitter input clock pulse delay	t_{TPD}	1 x Baud rate	3/ 4/	9, 10, 11	15		t_{CY}
		16 x Baud rate	See figure 4		3		
		64 x Baud rate			3		
Receiver input clock frequency	f_{RX}	1 x Baud rate	3/ 4/	9, 10, 11	1/ dc	64	kHz
		16 x Baud rate			1/ dc	310	
		64 x Baud rate			1/ dc	615	
Receiver input clock pulse width	t_{RPW}	1 x Baud rate	3/ 4/	9, 10, 11	12		t_{CY}
		16 x Baud rate	See figure 4		1		
		64 x Baud rate			1		
Receiver input clock pulse delay	t_{RPD}	1 x Baud rate	3/ 4/	9, 10, 11	15		t_{CY}
		16 x Baud rate	See figure 4		3		
		64 x Baud rate			3		
TxRDY delay from center of last bit	t_{TxRDY}	See figure 4	3/ 4/ 13/	9, 10, 11		12	t_{CY}
TxRDY fall from leading edge of $\overline{WR}$	$t_{TxRDY\ CLEAR}$		3/ 4/ 13/	9, 10, 11		400	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C < T_C < +125°C$ V_{CC} = 5 V ±10% for device type 01 V_{CC} = 5 V ±5% for device type 02	Group A subgroups	Limits Min	Limits Max	Unit
RxRDY delay from center of last bit	t_{RXRDY}	See figure 4 3/ 4/ 13/	9, 10, 11		26	t_{CY}
RxRDY fall from leading edge of $\overline{WR}$	$t_{RXRDY\ CLEAR}$	3/ 4/ 13/	9, 10, 11		400	ns
Internal SYNDET delay from rising edge of RxC	t_{IS}	See figure 4 3/ 4/ 13/	9, 10, 11		26	t_{CY}
External SYNDET setup after rising edge of RxC	t_{ES}	See figure 4 3/ 4/ 13/	9, 10, 11	16		t_{CY}
TxEMPTY delay from center of last bit	$t_{TX\ EMPTY}$	See figure 4 3/ 4/ 13/	9, 10, 11		20	t_{CY}
Control delay from rising edge of WRITE	t_{WC}	See figure 4 3/ 4/ 13/	9, 10, 11		8	t_{CY}
Control to READ setup time	t_{CR}	3/ 4/ 13/	9, 10, 11	20		t_{CY}

1/ Guaranteed if not tested.
2/ I_{CC} is measured in a static condition with outputs in the worst condition with all outputs unloaded.
3/ Test conditions: V_{CC} = 5 V ±10% for device type 01 V_{CC} = 5 V ±5% for device type 02 (See figure 5) V_{IL} = 0.45 V V_{IH} = 2.4 V V_{OL} = 0.8 V V_{OH} = 2.0 V I_{OL} = 2.2 mA I_{OH} = -400 µA
4/ Clock rise and fall times are controlled by the test equipment. Measurement of typical generated signal are $t_R = t_F$ = 5 ns.
5/ Chip Select ($\overline{CS}$) and Command/Data (C/$\overline{D}$) are considered as addresses.
6/ Test condition: C_L = 100 pF (see figure 6).
7/ Assumes that address is valid before $\overline{RD}$ ↑.
8/ This recovery time is for after a mode instruction only. Write data is allowed only when TxRDY = 1. Recovery time between writes for asynchronous mode is 8 t_{CY} and for synchronous mode is 16 t_{CY}.
9/ Due to test equipment limitations, actual tested values may differ from those specified but specified values are guaranteed.
10/ The TxC and RxC frequencies have the following limitations with respect to CLK: For 1 x Baud rate, f_{TX} or $f_{RX} \leq 1/(30\ t_{CY})$: For 16 x and 64 x Baud rate, f_{TX} or $f_{RX} \leq 1/(4.5\ t_{CY})$.
11/ Reset pulse width = 6 t_{CY} minimum; system clock must be running during reset.
12/ Limit may be guaranteed by indirect testing if not tested directly.
13/ Status update can have a maximum delay of 28 clock periods from the event affecting the status.

Case outline 3

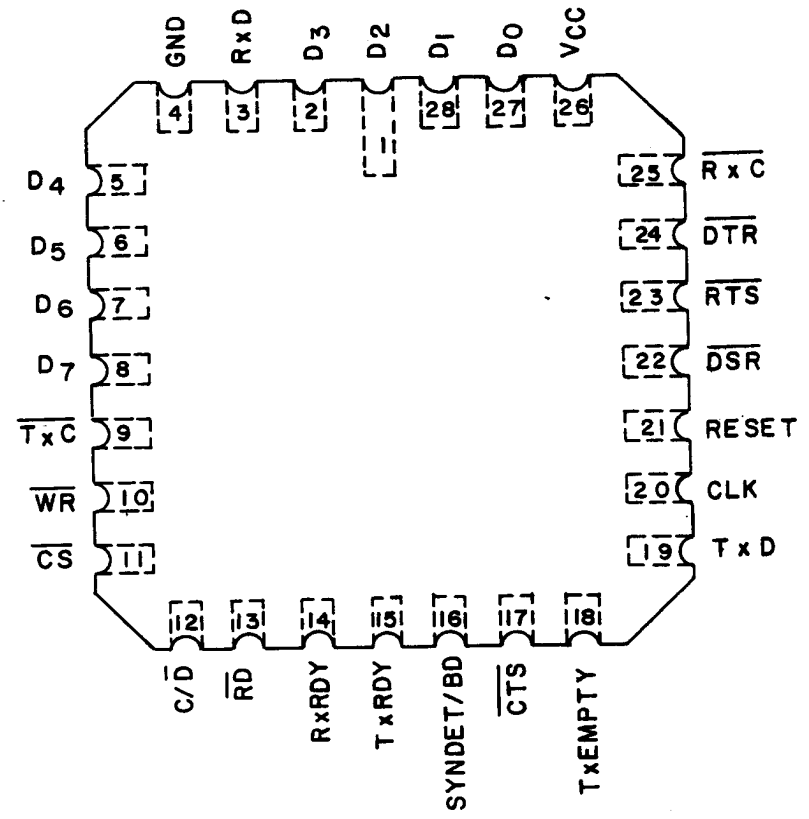

FIGURE 1. Terminal connections.

MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO	SIZE A	CODE IDENT. NO. 67268	DWG NO. 5962-87548
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Case outline X

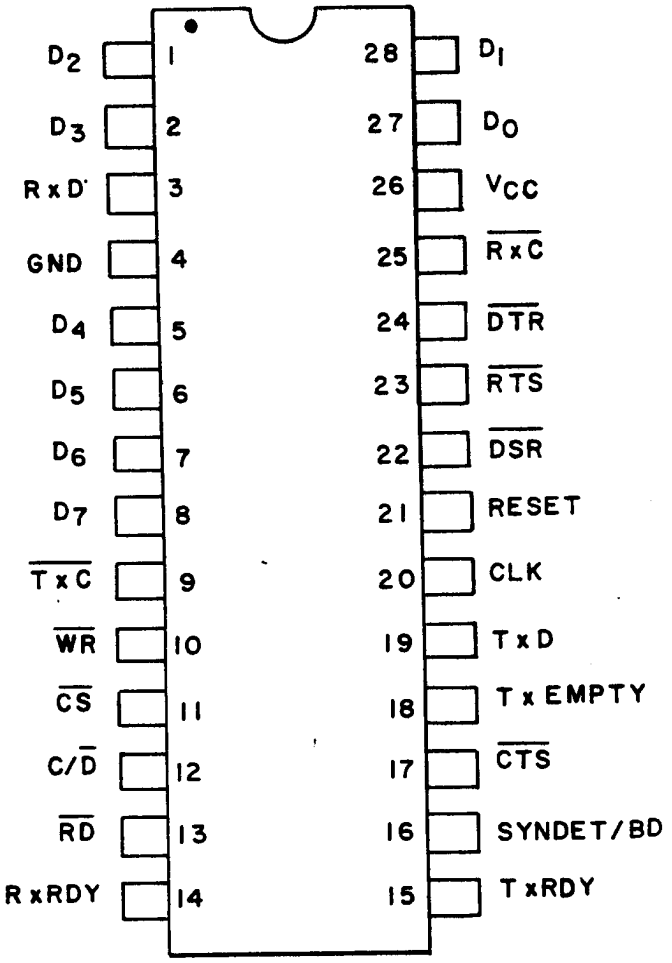

FIGURE 1. Terminal connections - Continued.

READ/WRITE LOGIC FUNCTION

C/$\overline{D}$	$\overline{RD}$	$\overline{W}$	$\overline{CS}$	
0	0	1	0	DEVICE DATA → DATA BUS
0	1	0	0	DATA BUS → DEVICE DATA
1	0	1	0	STATUS → DATA BUS
1	1	0	0	DATA BUS → CONTROL
X	1	1	0	DATA BUS → THREE-STATE
X	X	X	1	DATA BUS → THREE-STATE

FIGURE 2. Truth table.

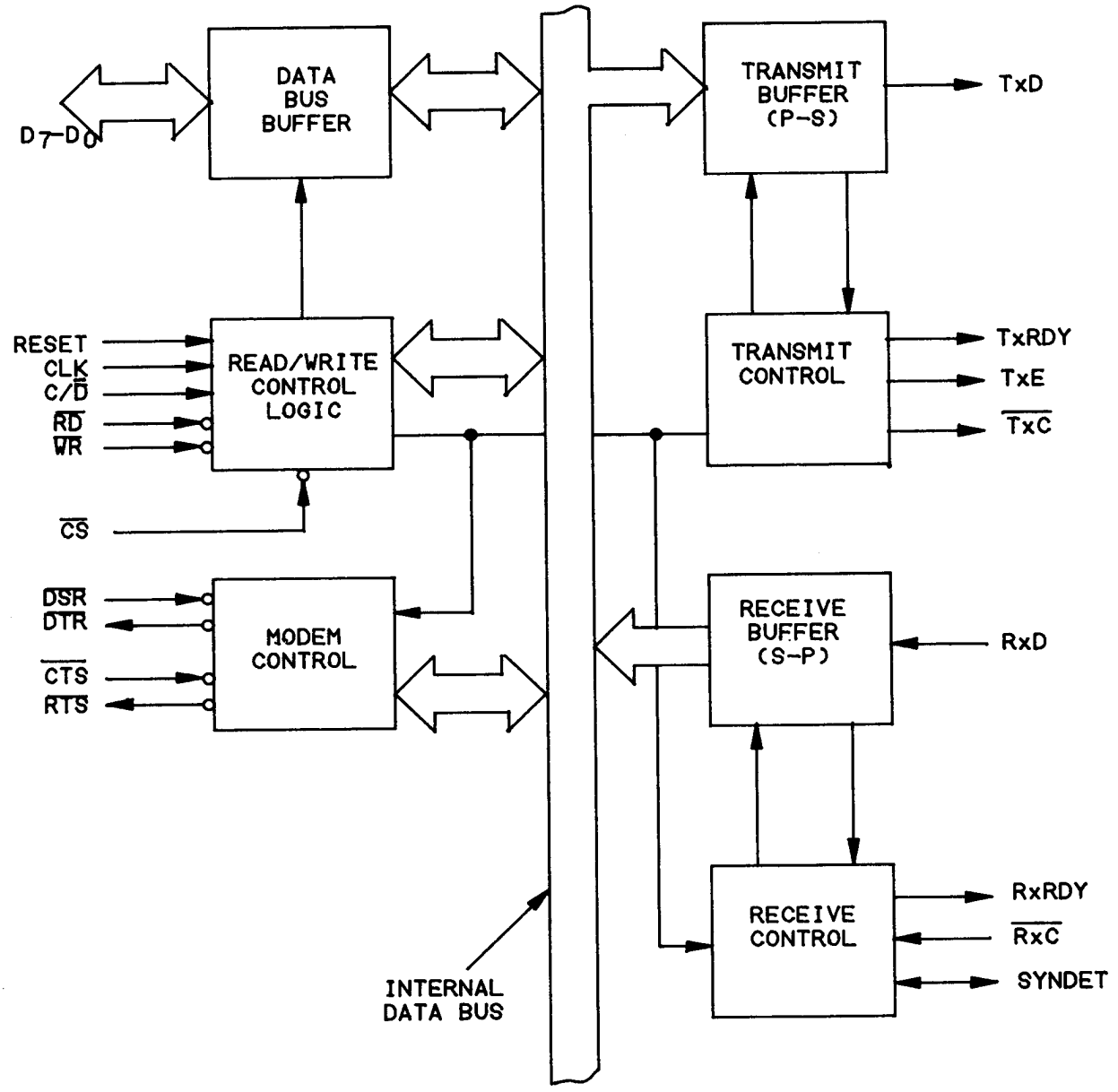

FIGURE 3. Block diagram.

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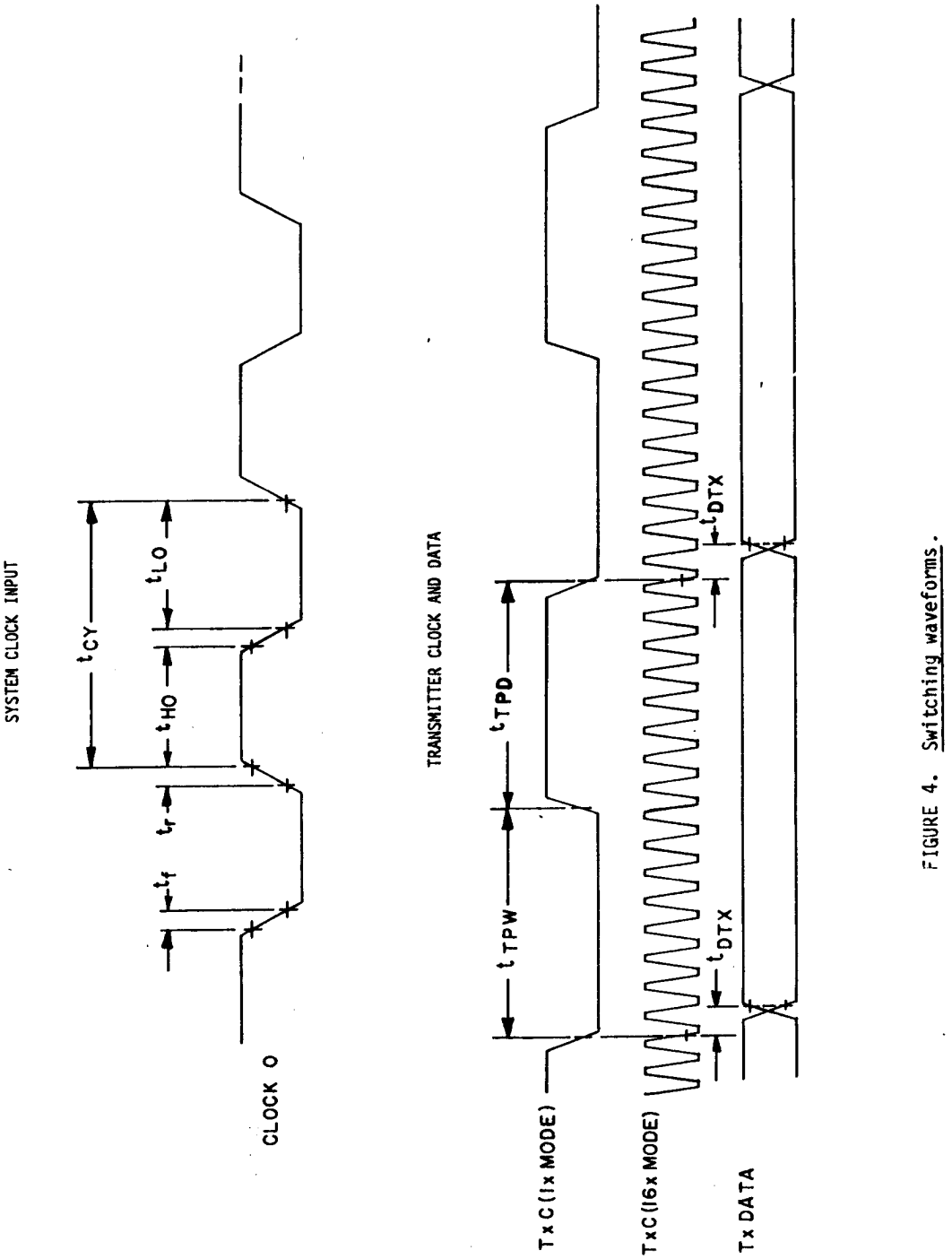

FIGURE 4. Switching waveforms.

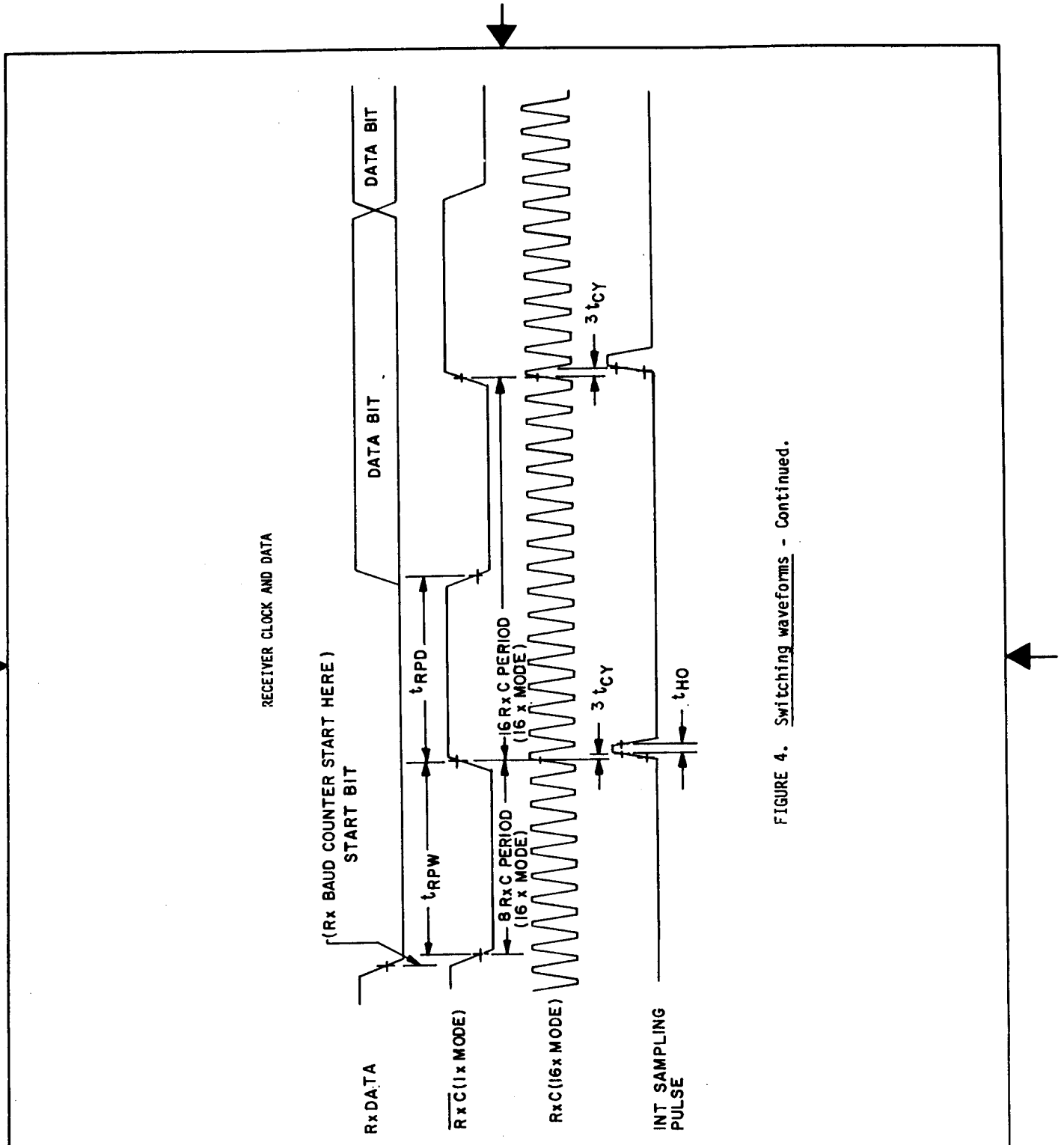

FIGURE 4. Switching waveforms - Continued.

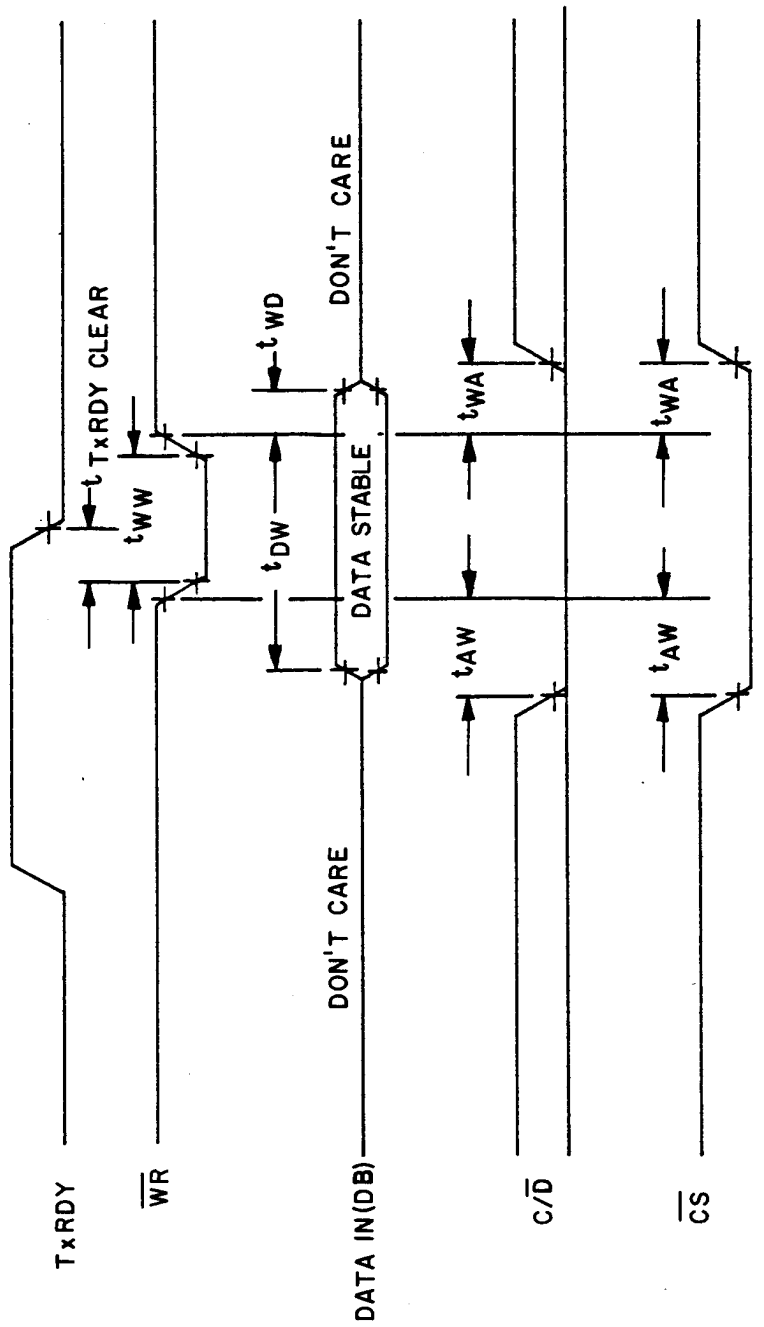

FIGURE 4. Switching waveforms - Continued.

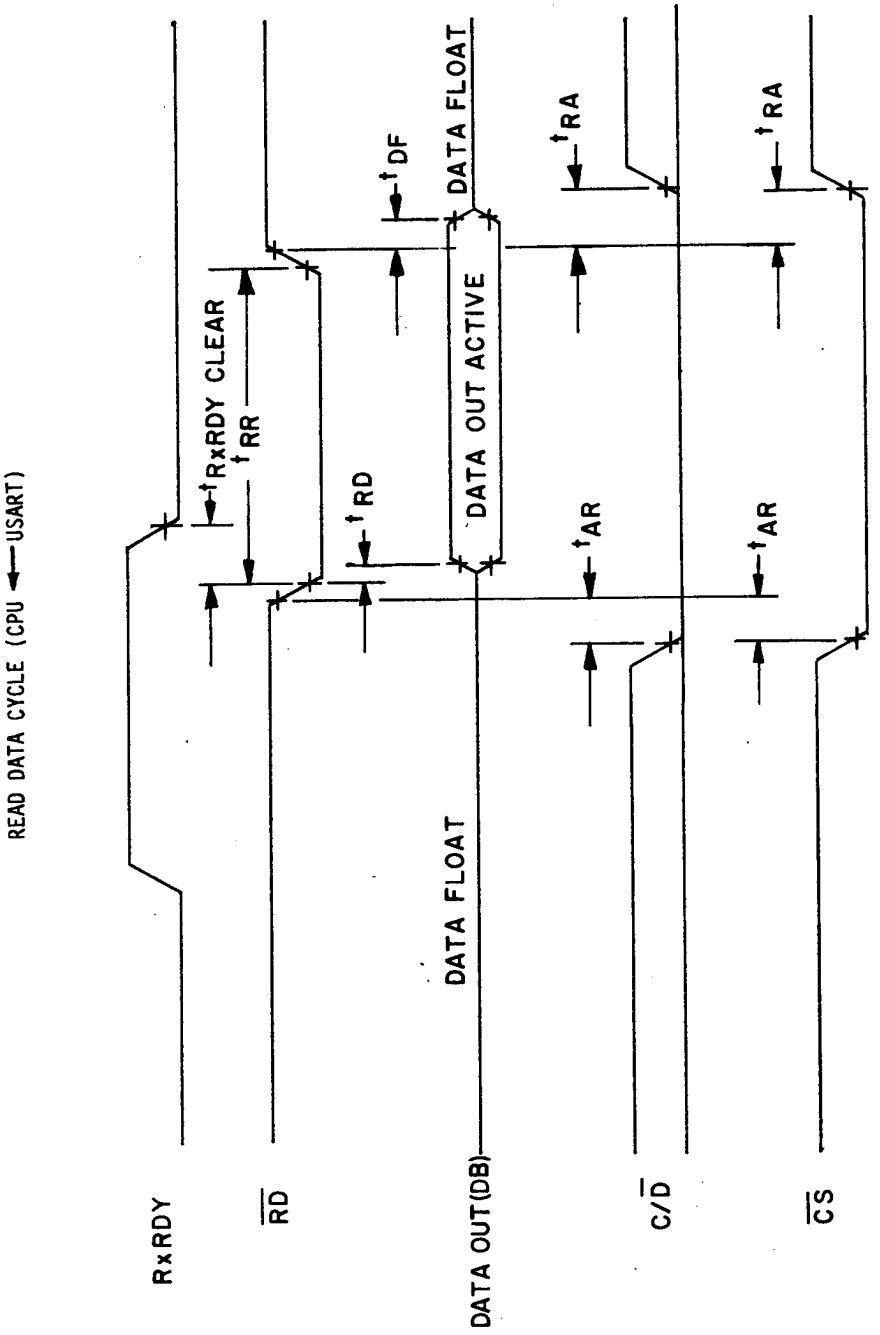

FIGURE 4. Switching waveforms - Continued.

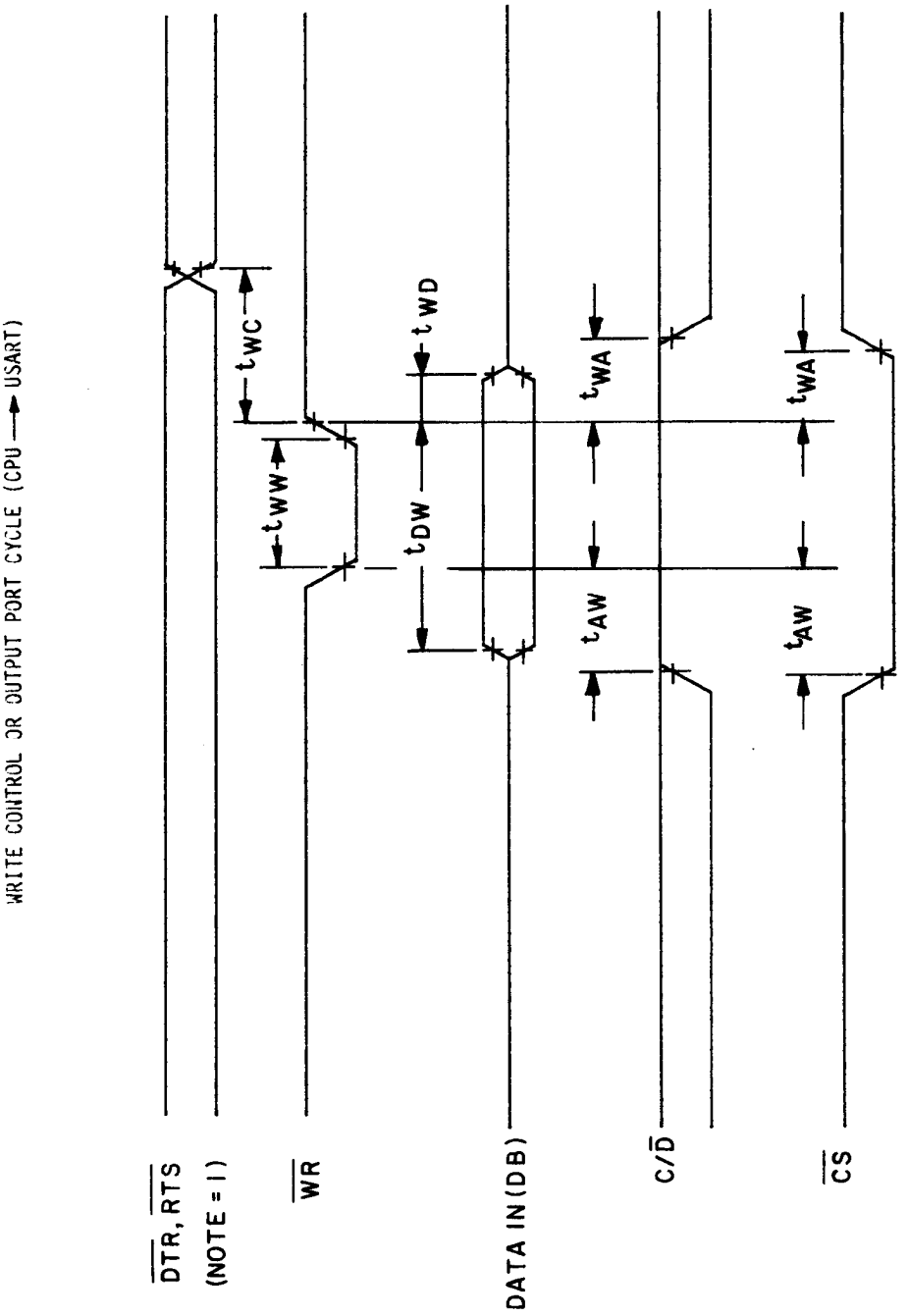

FIGURE 4. Switching waveforms - Continued.

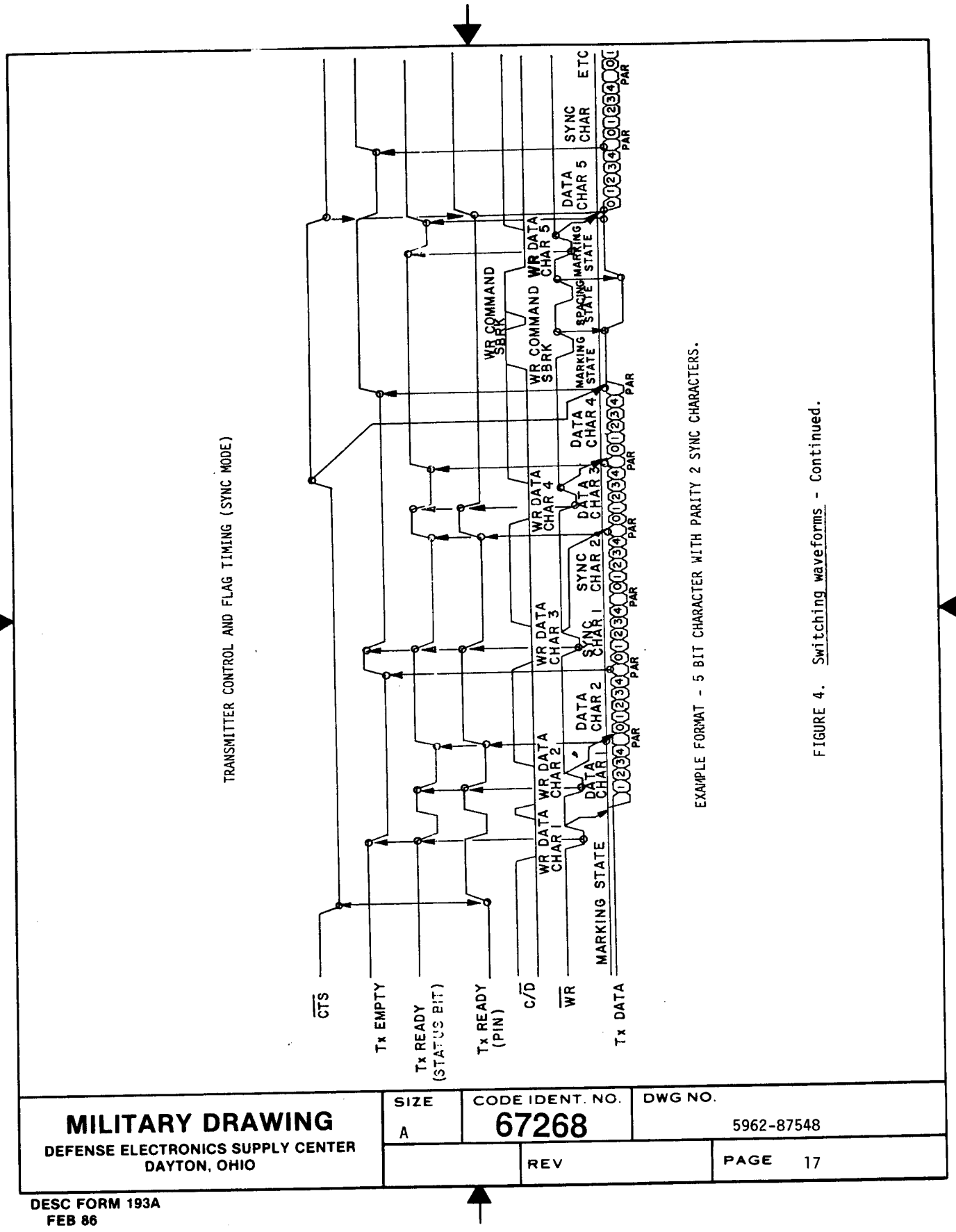

FIGURE 4. Switching waveforms - Continued.

MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO	SIZE A	CODE IDENT. NO. 67268	DWG NO. 5962-87548
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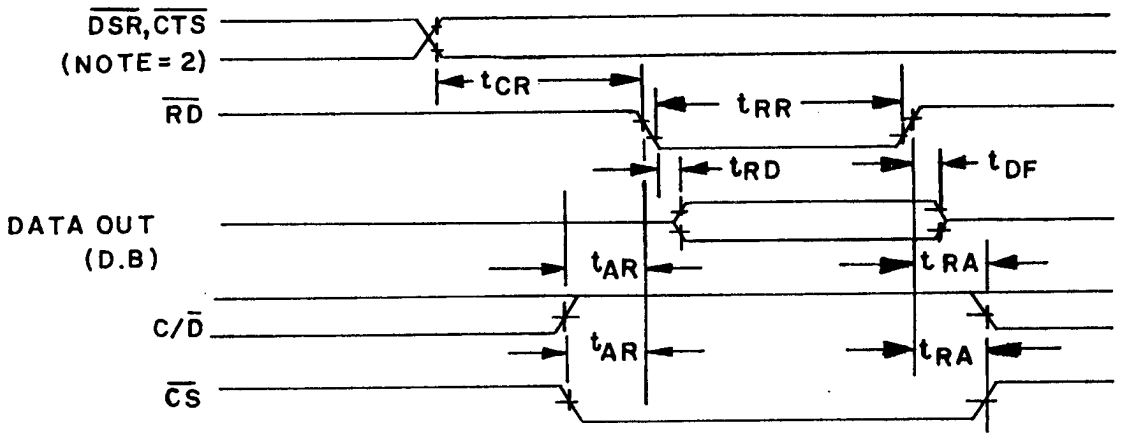
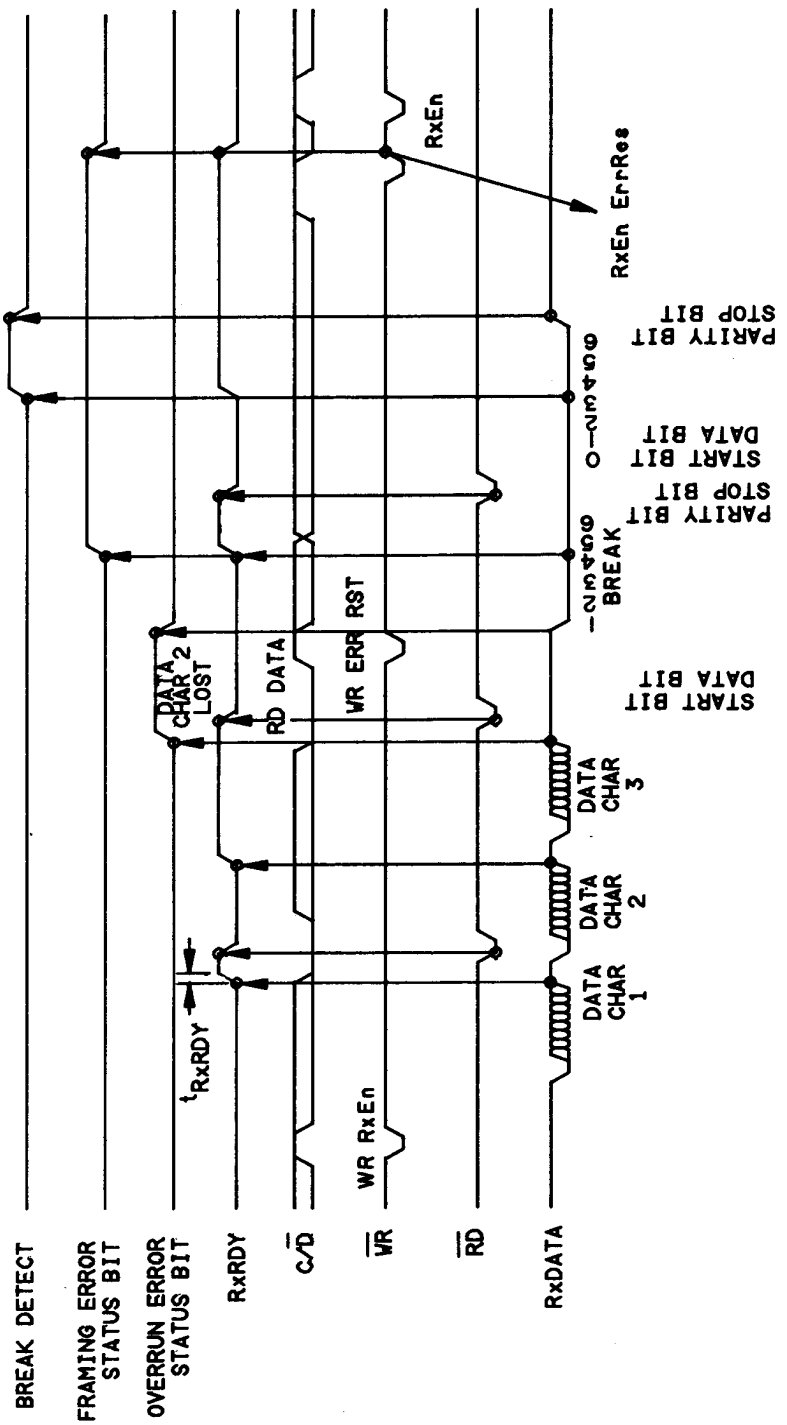
READ CONTROL OR INPUT PORT (CPU←USART)



NOTES:
1. t_{WC} includes the response timing of a control byte.
2. t_{CR} includes the effect of CTS on the TxENBL circuitry.

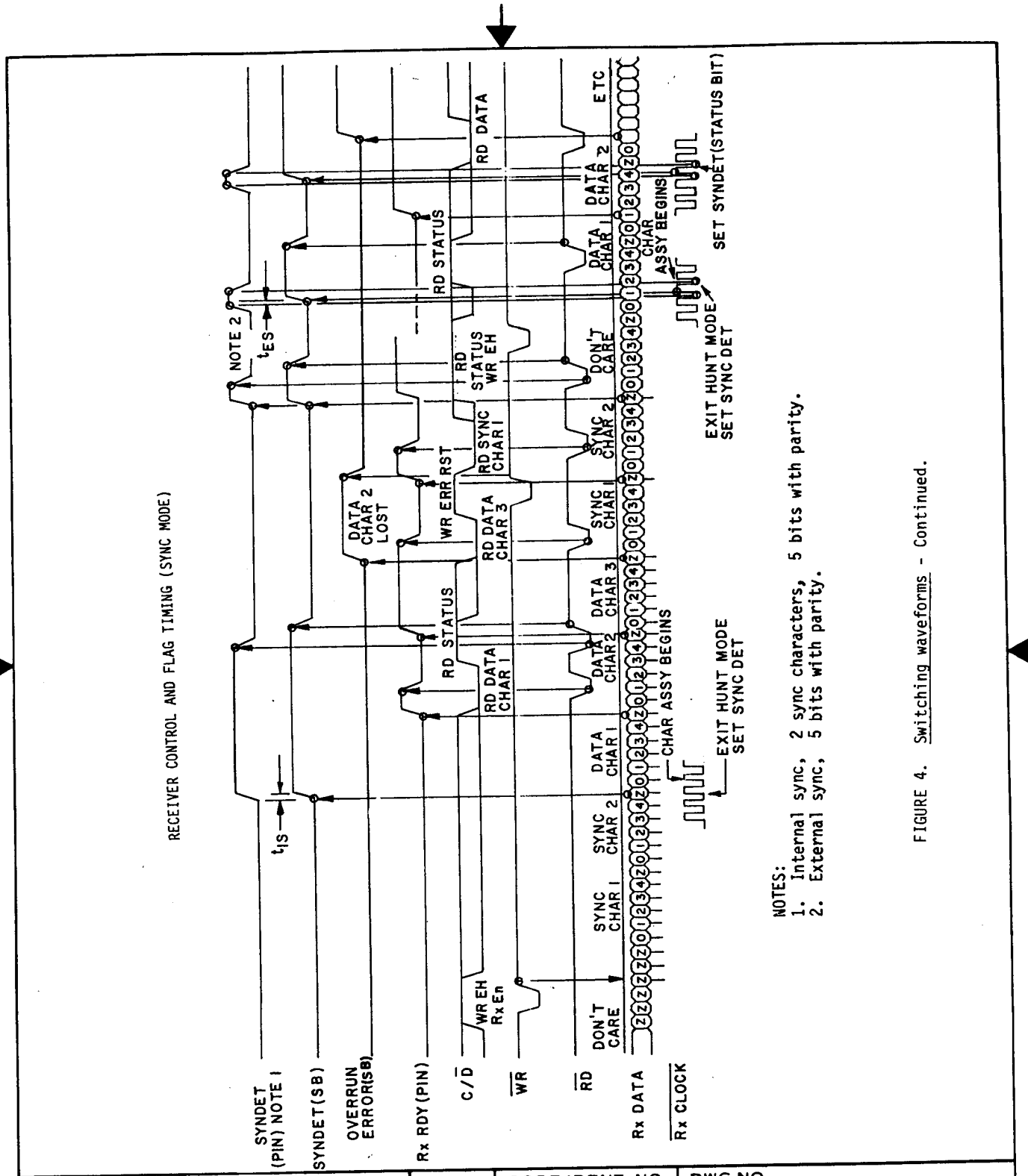
FIGURE 4. Switching waveforms - Continued.

FIGURE 4. Switching waveforms - Continued.



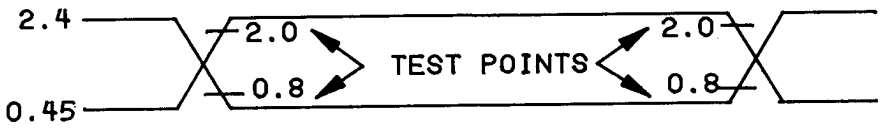
EXAMPLE FORMAT - 7 BIT CHARACTER WITH PARITY 2 and STOP BITS.

FIGURE 4. Switching waveforms - Continued.



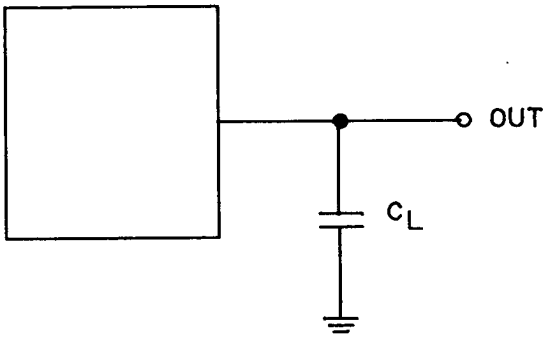
NOTES:
1. Internal sync, 2 sync characters, 5 bits with parity.
2. External sync, 5 bits with parity.

FIGURE 4. Switching waveforms - Continued.



NOTE:
AC testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Timing measurements are made at 2.0 V for a logic "1" and 0.8 V for a logic "0".

FIGURE 5. Switching test input/output waveform.



C_L=100 pF

FIGURE 6. Switching load circuit.

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test (method 1015 of MIL-STD-883).

(1) Test condition C or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and $C_{I/O}$ measurements) shall be measured initially and after process or design changes which may affect capacitance.

d. Subgroup 7 and 8 tests shall verify the truth table.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3 or 2, 8 (hot), 10
Additional electrical subgroups for group C periodic inspections	---

*PDA applies to subgroup 1.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test (method 1005 of MIL-STD-883) conditions:

(1) Test condition C or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by appendix B of MIL-M-38510 and method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.4 Approved sources of supply. Approved sources of supply are listed herein. Additional sources will be added as they become available. The vendors listed herein have agreed to this drawing and a certificate of compliance (see 3.5 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/	Replacement military specification part number
5962-8754801XX	34335	8251A/BXA	
5962-8754802XX	34649	MD8251A/B	
5962-87548023X	34649	MR8251A/B	

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34335	Advanced Micro Devices, Incorporated 901 Thompson Place P.O. Box 3453 Sunnyvale, CA 94088
34649	Intel Corporation 5000 W. Williams Field Road Chandler, AZ 85224

☆ U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-073/60058