REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Convert to new boilerplate format. Added device types 06, 07, and 08 for vendor CAGE code 01295. Added technical changes to sections 1.3 and 1.4. Technical changes to table I. Added device types 06, 07, and 08 to figure 1. Technical change to figure 2. Editorial changes throughout.	1990 JULY 25	Weckman

REV																								
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REV	A	A																						
SHEET	22	23																						
REV STATUS OF SHEETS	REV	A	A	A	A	A	A	A	A	A										A	A	A		
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21		

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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APPROVED BY: Michael A. Frye

DRAWING APPROVAL DATE: 27 SEPTEMBER 1988

REVISION LEVEL: A

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL, CMOS, SIGNAL PROCESSOR, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-87633

SHEET 1 OF 23 1

DESC FORM 193
SEP 87

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

5962-87633	01	Q	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Frequency
01	320C10	Digital signal processor	20 MHz
02	320C10-25	Digital signal processor	25 MHz
03	320CM10	Digital signal processor with mask programmable ROM	20 MHz
04	320CM10-25	Digital signal processor with mask programmable ROM	25 MHz
05	320CF10-25	Digital signal processor	6.7 - 25 MHz
06	320E15	Digital signal processor with EPROM	20 MHz
07	320C15	Digital signal processor	6.7 - 20 MHz
08	320C15-25	Digital signal processor	6.7 - 25 MHz

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
Q	D-5 (40-lead, 2.096" x .620" x .225"), dual in-line package
X	C-5 (44-terminal, .662" x .662" x .120"), square chip carrier package

1.3 Absolute maximum ratings.

Supply voltage range	-0.3 V dc to +7.0 V dc
Input/output voltage range	-0.3 V dc to V_{CC} +0.3 V dc
Input voltage range for device type 06	-0.3 V dc to +15.0 V dc
Storage temperature range	-65° C to 150° C
Power dissipation for 01-05, 07,08	0.4 W
Power dissipation for device type 06	0.495 W
Lead temperature (soldering, 10 seconds)	+300°C
Junction temperature (T_J)	+150°C
Thermal resistance (θ_{JC})	See MIL-M-38510, appendix C

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	4.5 V dc to 5.5 V dc
Supply voltage (V_{SS})	0.0 V
Minimum high-level input voltage (V_{IH}):	
All inputs except CLKIN	2.0 V dc
CLKIN	3.0 V dc
Maximum low-level input voltage (V_{IL}):	
Device types 01-08 (all other)	0.8 V dc
Device types 06-08 (MC/$\overline{MP}$)	0.6 V dc
High-level output current (I_{OH})	-300 µA
Low-level output current (I_{OL})	2.0 mA
Master clock cycle time	
Device types 01, 03, 06, 07	48.78 ns to 150 ns
Device types 02, 04	39.06 ns to 66.67 ns
Device types 05, 08	39.06 ns to 150 ns
Rise time master clock input	10 ns maximum
Fall time master clock input	10 ns maximum
Case operating temperature range (T_C)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Device types	Group A subgroups	Limits Min	Limits Max	Unit
High level output voltage	V_{OH}	I_{OH} = -300 µA	All	1,2,3	2.4		V
		I_{OH} = -20 µA 1/ 2/			V_{CC} -0.4		
Low level output voltage	V_{OL}	I_{OL} = 2.0 mA	All	1,2,3		0.5	V
Off-state output current	I_{OZ}	V_{CC} = 5.5 V, V_O = 2.4 V	All	1,2,3		20	µA
		V_{CC} = 5.5 V, V_O = 0.4 V				-20	
Input current	I_I	V_I = 0 V to 5.5 V	All	1,2,3		±50	µA
Supply current	I_{CC}	f = 20.5 MHz	01,03	1,2,3		65	mA
			06,07			90	
		f = 25.6 MHz	02,04, 05,08			75	
Input capacitance	C_{IN}	See 4.3.1c	All	4		25	pF
Output capacitance	C_{OUT}		All	4		25	pF
Input/output capacitance	$C_{I/O}$		All	4		35	pF
Functional tests		See 4.3.1d	All	7,8			
Crystal frequency 1/	f_X	See figure 3.	01,03 06,07	9,10,11	6.7	20.5	MHz
			02,04		15.0	25.6	
			05,08		6.7	25.6	
Master clock cycle time	$t_{C(MC)}$		01,03 06,07	9,10,11	48.78	150	ns
			02,04		39.06	66.67	
			05,08		39.06	150	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics.

Parameter	Symbol	Conditions $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$, unless otherwise specified	Device types	Group A subgroups	Limits Min	Limits Max	Unit
Pulse duration master clock 1/	$t_{W(MCP)}$	See figure 3.	All	9,10,11	0.475 $t_{C(MC)}$	0.525 $t_{C(MC)}$	ns
CLKOUT cycle time 3/	$t_{C(C)}$		01,03 06,07	9,10,11	195.12	600	ns
			02,04		156.25	266.67	
			05,08		156.25	600	
Delay time CLKIN ↑ to CLKOUT ↓ 1/	$t_{D(MCC)}$		All	9,10,11	15	60	ns
Delay time CLKOUT ↓ to address bus valid	t_{D1}		All	9,10,11	10 1/	50	ns
Delay time CLKOUT ↓ to $\overline{MEN}$ ↓	t_{D2}		All	9,10,11	1/ $.25t_{C(C)}-5$	$.25t_{C(C)}+15$	ns
Delay time CLKOUT ↓ to $\overline{MEN}$ ↑	t_{D3}		All	9,10,11	1/ -10	15	ns
Delay time CLKOUT ↓ to $\overline{DEN}$ ↓	t_{D4}		All	9,10,11	1/ $.25t_{C(C)}-5$	$.25t_{C(C)}+15$	ns
Delay time CLKOUT ↓ to $\overline{DEN}$ ↑	t_{D5}		All	9,10,11	1/ -10	15	ns
Delay time CLKOUT ↓ to $\overline{WE}$ ↓	t_{D6}		All	9,10,11	1/ $.5t_{C(C)}-5$	$.5t_{C(C)}+15$	ns
Delay time CLKOUT ↓ to $\overline{WE}$ ↑	t_{D7}		All	9,10,11	1/ -10	15	ns
Delay time CLKOUT ↓ to data bus OUT valid	t_{D8}		01,02, 03,04, 05,07, 08	9,10,11		$.25t_{C(C)}+65$	ns
			06	9,10,11		$.25t_{C(C)}+80$	
Time after CLKOUT ↓ that data bus starts to be driven	t_{D9}		All	9,10,11	1/ $.25t_{C(C)}-5$		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics.

Parameter	Symbol	Conditions $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Device types	Group A subgroups	Limits Min	Limits Max	Unit
Time after CLKOUT ↓ that data bus stops being driven	t_{D10}	See figure 3.	01,02, 03,04, 05,07, 08	9,10,11		1/ $.25t_C$ (C)+40	ns
			06			1/ $.25t_C$ (C)+80	
Delay time $\overline{DEN}$ ↑ $\overline{WE}$↑, and $\overline{MEN}$ ↑ from RS 1/	t_{D11}		01,02, 03,04, 05,07, 08	9,10,11		$1.5t_C$ (C)+50	ns
			06			$.5t_C$ (C)+50	
Data bus disable time after $\overline{RS}$ 1/	$t_{DIS(R)}$		01,02, 03,04, 05,07, 08	9,10,11		$1.25t_C$ (C)+50	ns
			06			$.25t_C$ (C)+50	
Data bus OUT valid after CLKOUT ↓	t_V		All	9,10,11	$.25t_C$ (C)-10		ns
Address bus setup time prior to $\overline{MEN}$ ↓ or $\overline{DEN}$ ↓	$t_{SU(A-MD)}$		All	9,10,11	$.25t_C$ (C)-45		ns
Setup time data bus valid prior to CLKOUT ↓	$t_{SU(D)}$		All	9,10,11	50		ns
Hold time data bus held valid after CLKOUT ↓ 4/	$t_{H(D)}$		All	9,10,11	0		ns
$\overline{RS}$ setup time prior to CLKOUT 5/	$t_{SU(R)}$		All	9,10,11	50		ns
$\overline{RS}$ pulse duration 6/	$t_{W(R)}$		All	9,10,11	$5t_{C(C)}$		ns
$\overline{INT}$ pulse duration	$t_{W(INT)}$		All	9,10,11	$t_{C(C)}$		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Parameter	Symbol	Conditions $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$, unless otherwise specified	Device types	Group A subgroups	Limits		Unit
					Min	Max	
Setup time $\overline{INT}$ ↓ before CLKOUT ↓	$t_{SU(INT)}$	See figure 3.	All	9,10,11	50		ns
$\overline{BIO}$ pulse duration	$t_{W(IO)}$		All	9,10,11	$t_{C(C)}$		ns
Setup time $\overline{BIO}$ ↓ before CLKOUT ↓	$t_{SU(IO)}$		All	9,10,11	50		ns

1/ Guaranteed to the limit specified in table I, if not tested.
2/ This voltage specification is included for interface to high speed CMOS logic. Note that all other timing parameters are specified for TTL.
3/ $t_{C(C)}$ is the cycle time of CLKOUT, (i.e., $4t_{C(MC)}$ is 4 times the CLKIN cycle time if an external oscillator is used).
4/ Data may be removed from the bus upon $\overline{MEN}$↑ or $\overline{DEN}$ ↑preceding CLKOUT.
5/ $\overline{RS}$ can occur anytime during a clock cycle. The time specified is the minimum to ensure synchronous operation.
6/ $\overline{RS}$ must not happen until clocks are stabilized, approximately 100 ms after power up.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Functional block diagram. The functional block diagram shall be as specified on figure 2.

3.2.3 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

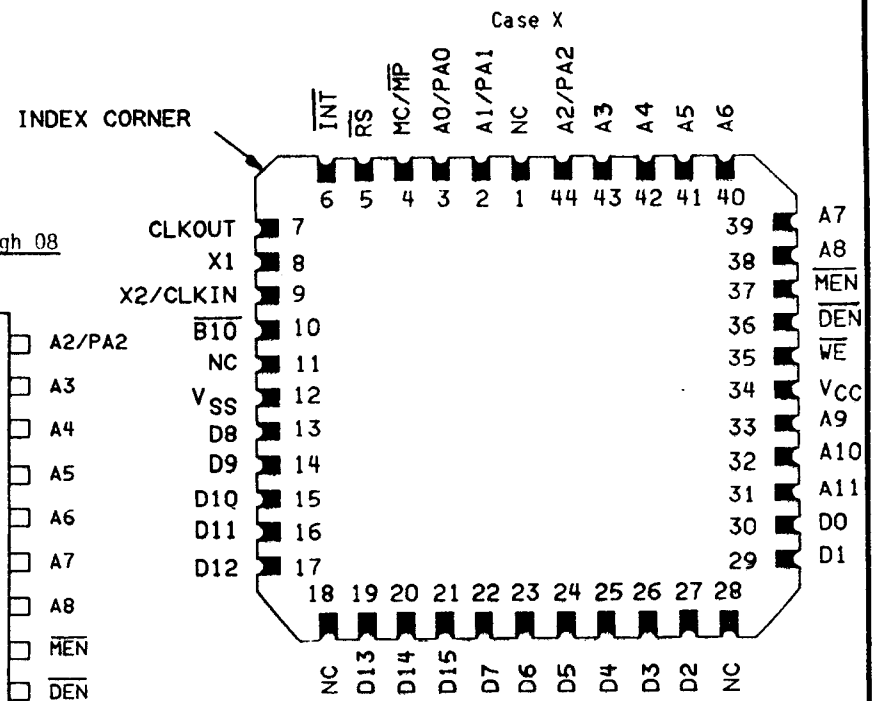
3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-ECC prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

Device types 01 through 08

Case X



Device types 01 through 08

Case Q

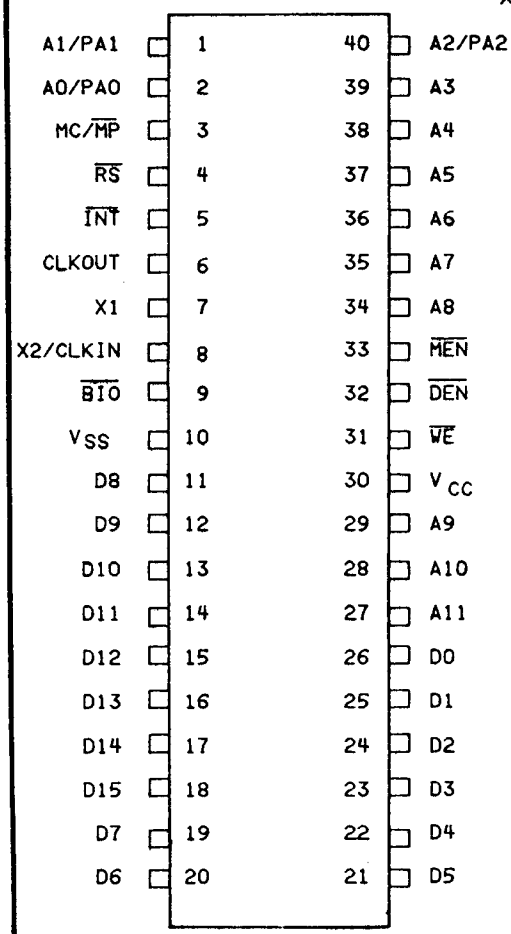
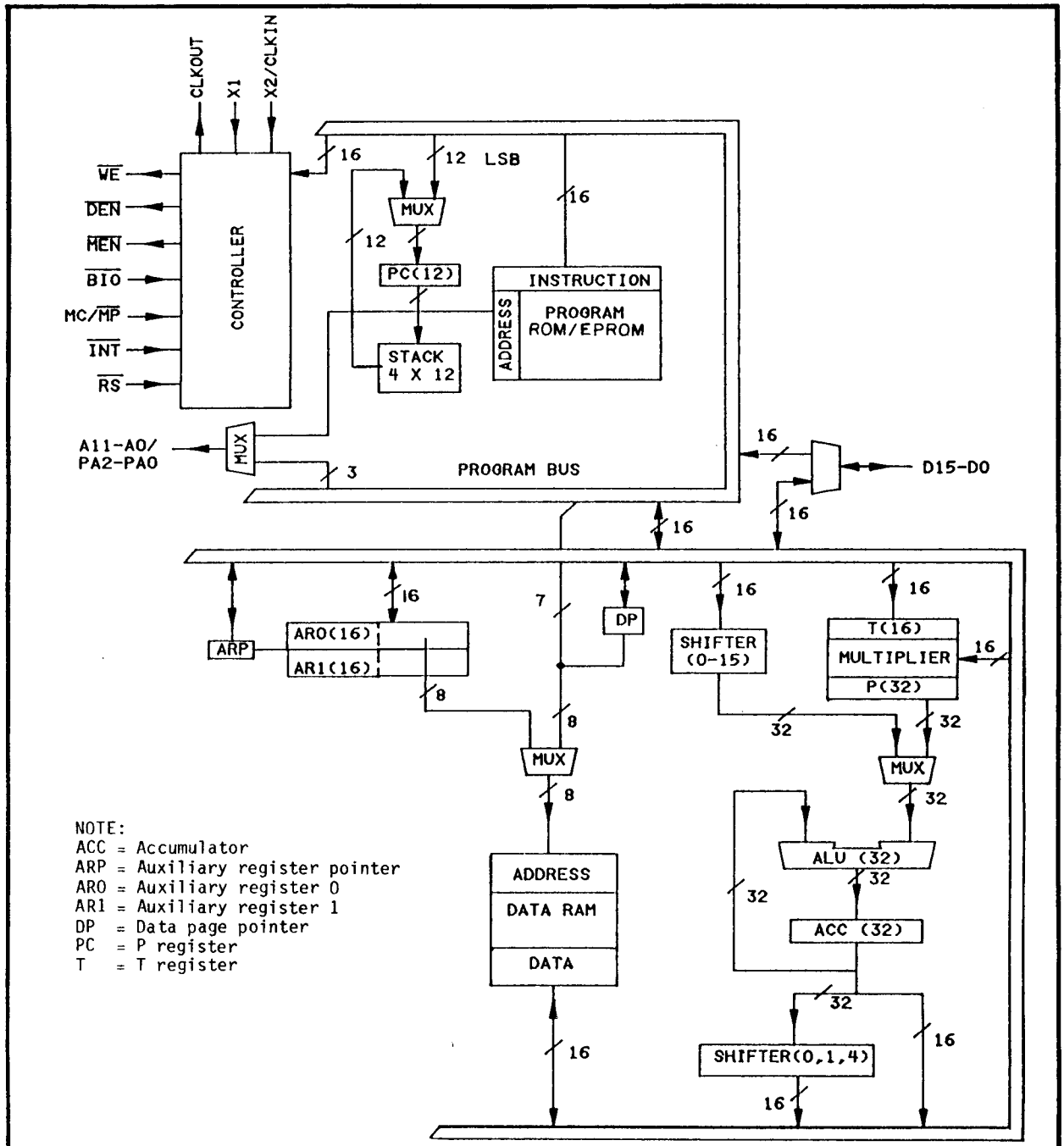


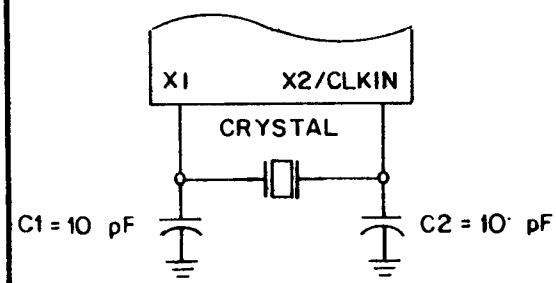
FIGURE 1. Terminal connections, top view.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-87633
		REVISION LEVEL A	SHEET 8

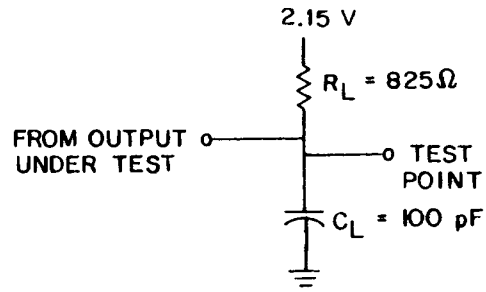


NOTE:
ACC = Accumulator
ARP = Auxiliary register pointer
ARO = Auxiliary register 0
AR1 = Auxiliary register 1
DP = Data page pointer
PC = P register
T = T register

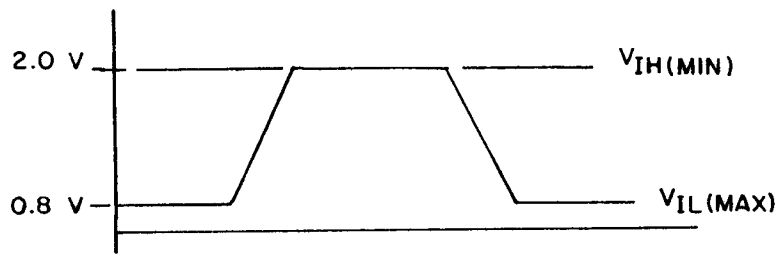
FIGURE 2. Functional block diagram.



INTERNAL CLOCK OPTION



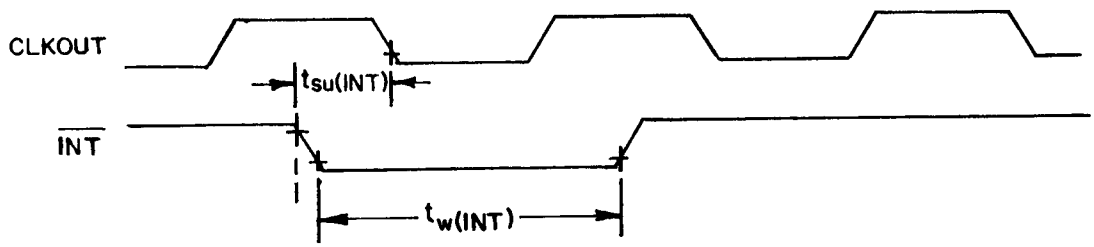
NOTE: Equivalent TTL load may be used.



INPUT VOLTAGE REFERENCE WAVEFORM

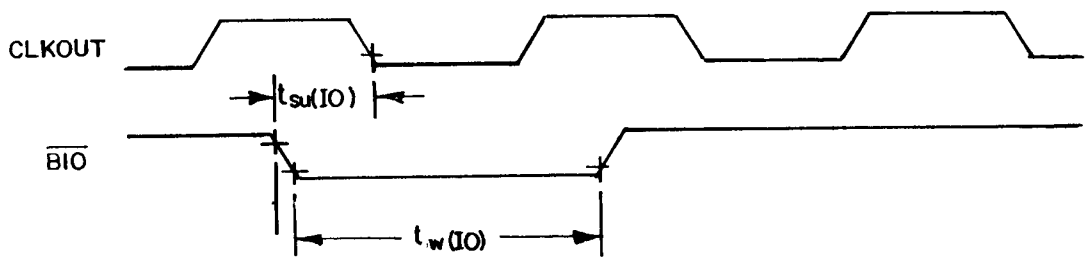
FIGURE 3. AC loading circuits and switching waveforms.

INTERRUPT TIMING



NOTES:
1. Timing measurements are referenced to and from low voltage of 0.8 volt and a high voltage of 2.0 volts, unless otherwise noted.
2. $\overline{INT}$ fall time must be less than 15 ns.

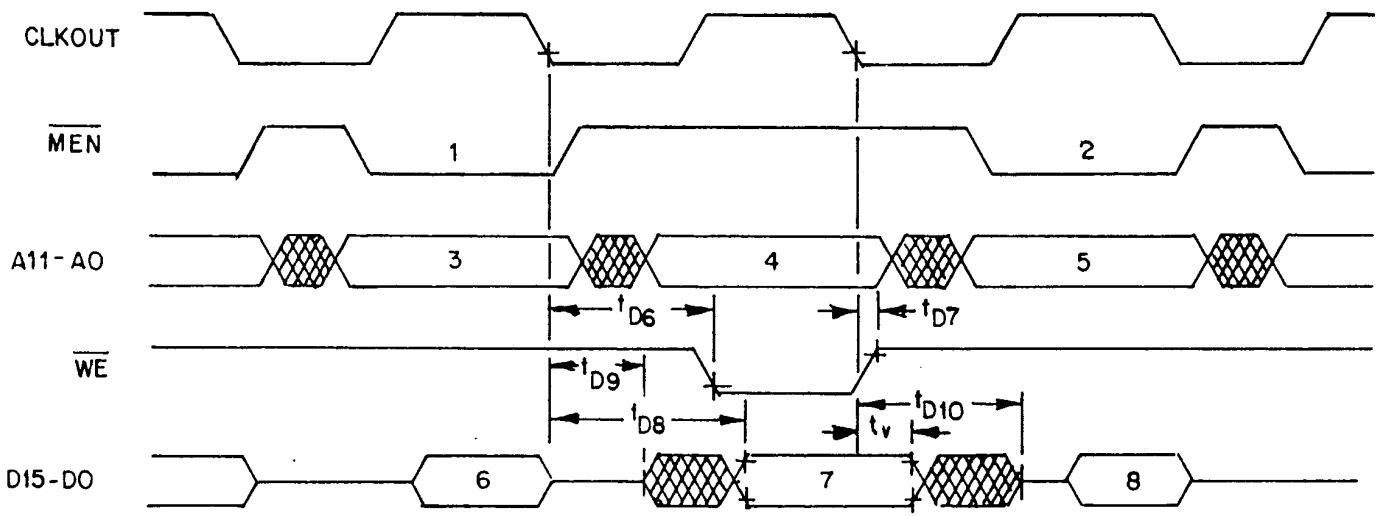
$\overline{BIO}$ TIMING



NOTES:
1. Timing measurements are referenced to and from low voltage of 0.8 volt and a high voltage of 2.0 volts, unless otherwise noted.
2. $\overline{BIO}$ fall time must be less than 15 ns.

FIGURE 3. AC loading circuits and switching waveforms - Continued.

OUT INSTRUCTION TIMING

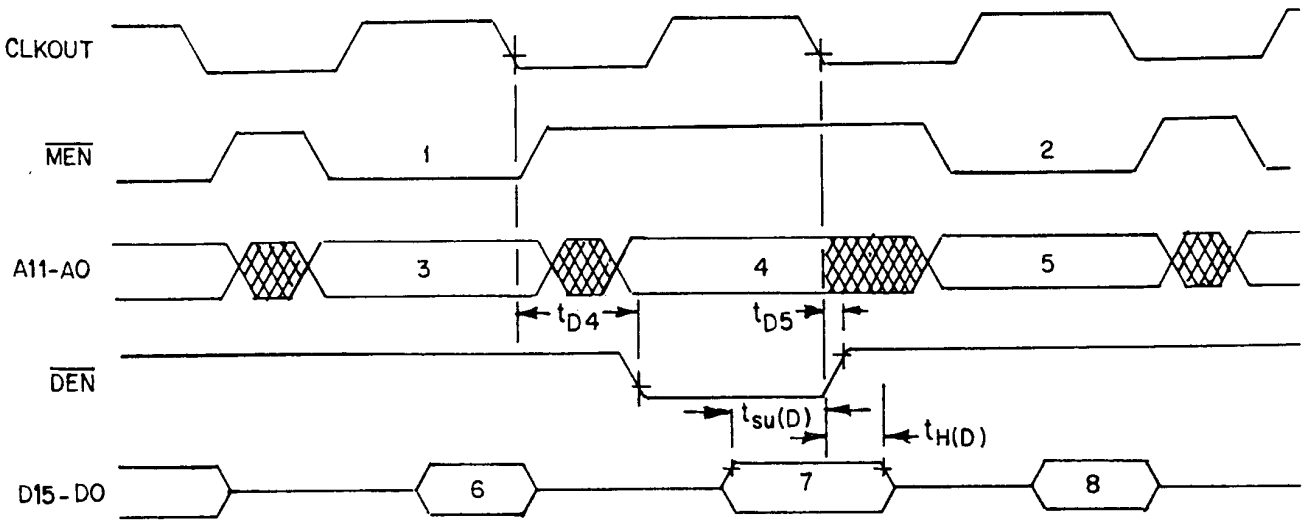


Legend:
1. Out instruction prefetch
2. Next instruction prefetch
3. Address bus valid
4. Peripheral address valid
5. Address bus valid
6. Instruction in valid
7. Data out valid
8. Instruction in valid

NOTE: Timing measurements are referenced to and from low voltage of 0.8 volt and a high voltage of 2.0 volts, unless otherwise noted.

FIGURE 3. AC loading circuits and switching waveforms - Continued.

IN INSTRUCTION TIMING

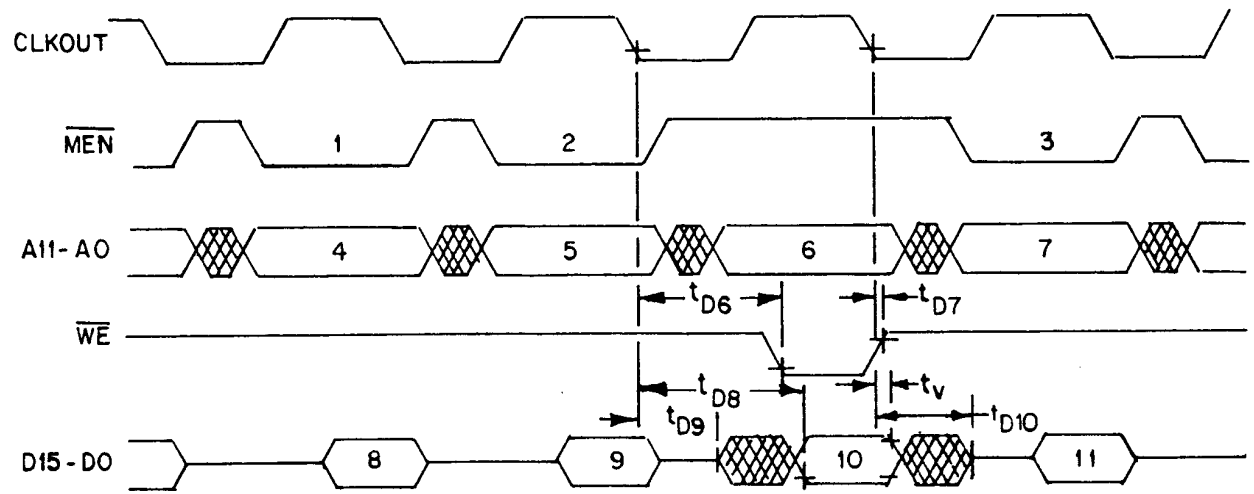


Legend:
1. In instruction prefetch
2. Next instruction prefetch
3. Address bus valid
4. Peripheral address valid
5. Address bus valid
6. Instruction in valid
7. Data out valid
8. Instruction in valid

NOTE: Timing measurements are referenced to and from low voltage of 0.8 volt and a high voltage of 2.0 volts, unless otherwise noted.

FIGURE 3. AC loading circuits and switching waveforms - Continued.

TBLW INSTRUCTION TIMING

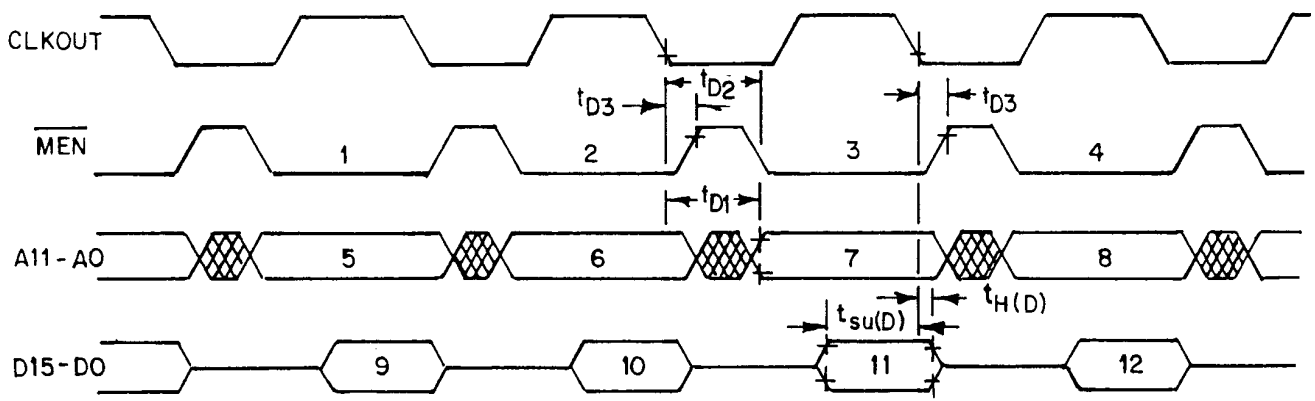


Legend:
1. TBLW instruction prefetch
2. Dummy prefetch
3. Next instruction address valid
4. Address bus valid
5. Address bus valid
6. Address bus valid
7. Address bus valid
8. Instruction in valid
9. Instruction in valid
10. Data out valid
11. Instruction in valid

NOTE: Timing measurements are referenced to and from low voltage of 0.8 volt and a high voltage of 2.0 volts, unless otherwise noted.

FIGURE 3. AC loading circuits and switching waveforms - Continued.

TBLR INSTRUCTION TIMING

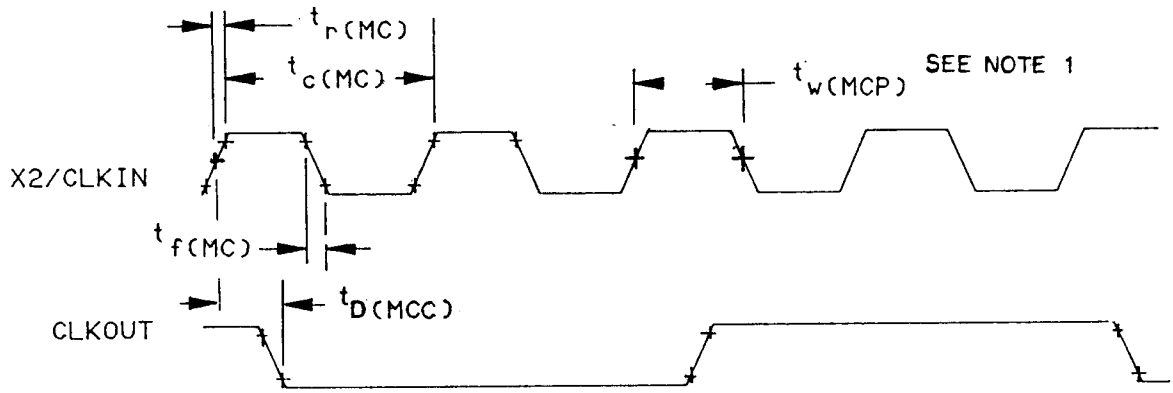


Legend:
1. TBLR instruction prefetch
2. Dummy prefetch
3. Data fetch
4. Next instruction address valid
5. Address bus valid
6. Address bus valid
7. Address bus valid
8. Address bus valid
9. Instruction in valid
10. Instruction in valid
11. Data out valid
12. Instruction in valid

NOTE: Timing measurements are referenced to and from low voltage of 0.8 volt and a high voltage of 2.0 volts, unless otherwise noted.

FIGURE 3. AC loading circuits and switching waveforms - Continued.

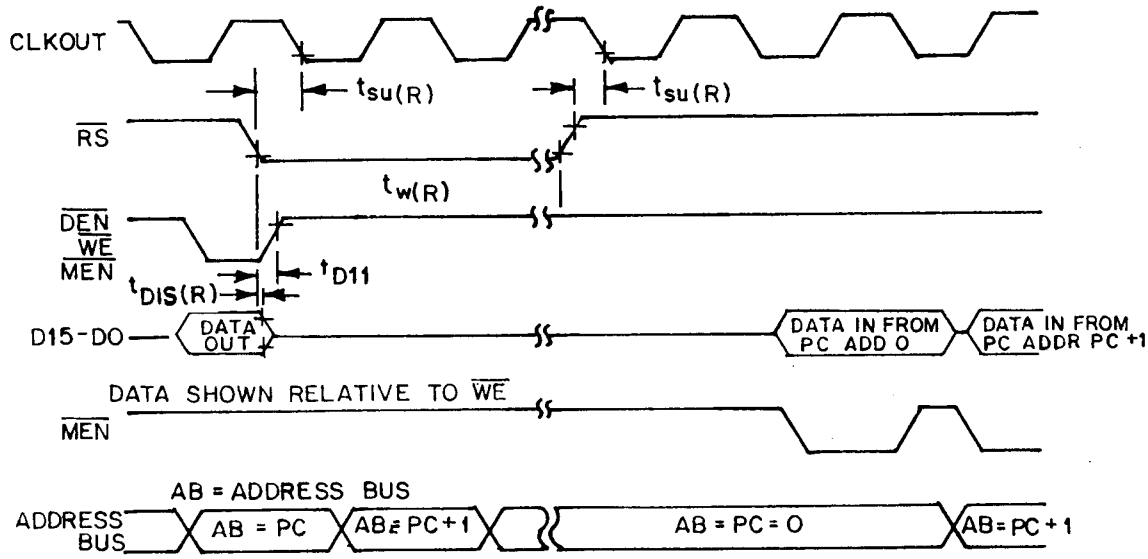
CLOCK TIMING



NOTES:
1. $t_{D(MCC)}$ and $t_{w(MCP)}$ are referenced to an intermediate level of 1.5 volts on the CLKIN waveform.
2. Timing measurements are referenced to and from a low voltage of 0.8 volt and a high voltage of 2.0 volts, unless otherwise noted.

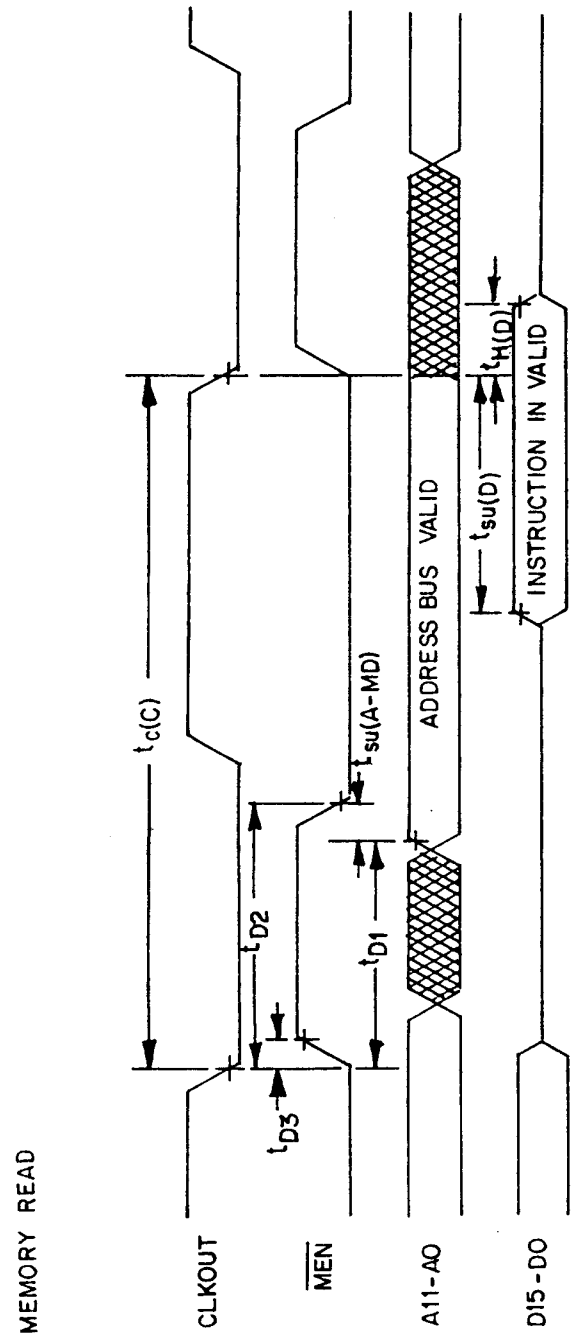
FIGURE 3. AC loading circuits and switching waveforms - Continued.

RESET TIMING



NOTES:
1. Timing measurements are referenced to and from a low voltage of 0.8 volt and a high voltage of 2.0 volts, unless otherwise noted.
2. $\overline{RS}$ forces $\overline{DEN}$, $\overline{WE}$, and $\overline{MEN}$ high and three states data bus DO through D15. AB outputs (and program counter) are synchronously clear to zero after the next complete CLK cycle from + $\overline{RS}$.
3. $\overline{RS}$ must be maintained for a minimum of five clock cycles.
4. Resumption of normal program will commence after one CLK cycle from + $\overline{RS}$.
5. Due to the synchronizing action on $\overline{RS}$, time to execute the function can vary dependent upon when + $\overline{RS}$ or + $\overline{RS}$ occurs in the CLK cycle.
6. Diagram shown is for definition purposes only. $\overline{DEN}$, $\overline{WE}$, and $\overline{MEN}$ are mutually exclusive.
7. During a write cycle, $\overline{RS}$ may produce an invalid write address.

FIGURE 3. AC loading circuits and switching waveforms - Continued.



NOTE: Timing measurements are referenced to and from low voltage of 0.8 volt and a high voltage of 2.0 volts, unless otherwise noted.

FIGURE 3. AC loading circuits and switching waveforms - Continued.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.7 Notification of change. Notification of change to DESC-ECC shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.9 User mask program. For device types 03 and 04, since the ROM is programmed by the manufacturer in a variety of configurations, the contracting activity shall provide an altered item drawing describing the mask program to be used by the manufacturer. This drawing shall consist of the desired mask program supplied on one or more of the following media: Truth table, floppy disk, or EPROM.

3.10 Additional processing for device type 06. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.10.1 Erasure of EPROMS for device type 06. When specified, devices shall be erased in accordance with the procedures and characteristics specified in 4.4.

3.10.2 Programmability of EPROMS for device type 06. When specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified in 4.5.

3.10.3 Verification of erasure or programmability of EPROMS for device type 06. When specified, devices shall be verified as either programmed to the specified pattern or erased. As a minimum, verification shall consist of performing a functional test (subgroup) to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a failure, and shall be removed from the lot.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

c. For device type 06 a data retention stress test shall be included as part of the screening procedure and shall consist of the following steps:

(1) Erase (see 3.10.1).

(2) Program all 0's (see 3.10.2).

(3) Test at +25°C. Measure V_{CC} max and store this value in the signature row (see 3.10.3).

(4) Unbiased bake 72 hours at +165°C ±5°C.

(5) Margin test at +25°C. Measure V_{CC} max and compare with the value stored in the signature row. Any part with a delta greater than 0.66 V or with V_{CC} max less than 6.0 V constitute a failure. Also program and verify the r bit.

(6) Erase (see 3.10.1).

(7) Program with ramdom code. Verify this at 6.0 V (see 3.10.2).

(8) Burn-in (see 4.2a).

(9) Verify EPROM array, program and verify r bit at 6.0 V and +25°C (see 3.10.3).

(10) Erase (see 3.10.1).

(11) Program with random code (see 3.10.2).

(12) Test at +125°C and 6.0 V. Verify EPROM array. Program and verify r bit (see 3.10.3).

(13) Erase (see 3.10.1).

(14) Program with random code (see 3.10.2).

(15) Test at -55°C and 6.0 V. Verify EPROM array. Program and verify r bit (see 3.10.3).

(16) Erase (see 3.10.1).

(17) Verify erasure at +25°C (see 3.10.3).

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I) 1/
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 4, 7, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5008)	2, 8A, 10

1/ Any subgroups at the same temperature may be combined when using a multifunction tester.
* PDA applies to subgroup 1.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 ($C_{IN}/C_{OUT}/C_{I/O}$ measurement) shall be measured only for the initial test and after process or design changes which may affect capacitance. A minimum sample size of five devices with zero rejects shall be required.

d. Subgroups 7 and 8 shall verify the instruction set. The instruction set forms a part of the vendor's test tape and shall be maintained and available from the approved sources of supply.

e. All device type 06 devices selected for testing shall have the EPROM programmed with a checkerboard pattern or equivalent. After completion of all testing, the devices shall be erased and verified (except devices submitted for groups C and D testing).

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

(4) All device type 06 devices selected for testing shall be programmed with a checkerboard pattern or equivalent. After completion of all testing, the devices shall be erased and verified.

4.4 Erasing procedure for device type 06. The recommended erasure procedure for the device is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., ultraviolet intensity times exposure time) for exposure should be a minimum of 15 ws/cm^2. The erasure time with this dosage is approximately 25 minutes using an ultraviolet lamp with a 12000 µW/cm^2 power rating. The device should be placed within one inch of the lamp tubes during erasure. The maximum integrated dose the device can be exposed to without damage is 7258 ws/cm^2 (1 week at 12000 µW/cm^2). Exposure of EPROMS to high intensity ultraviolet light for long periods may cause permanent damage.

4.5 Programming procedures for device type 06. The programming procedures shall be as specified by the device manufacturer.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECC, telephone (513) 296-8528.

6.5 Comments. Comments on this drawing should be directed to DESC-ECC, Dayton, Ohio 45444, or telephone 513-296-8528.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. Additional sources will be added as they become available. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECC. The approved sources of supply listed below are for information purposes only and are current only to the date of the last action of this document.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/
5962-8763301QX	01295	SMJ320C10JDM
5962-8763301QX	60991	DSP320C10BQX
5962-8763301XX	01295	SMJ320C10FDM
5962-8763301XX	60991	DSP320C10BUX
5962-8763302QX	60991	DSP320C10-25BQX
5962-8763302QX	01295	SMJ320C10-25JDM
5962-8763302XX	60991	DSP320C10-25BUX
5962-8763302XX	01295	SMJ320C10-25FDM
5962-8763303QX	60991	DSP320CM10BQX
5962-8763303QX	01295	SMJ320CM10JDM
5962-8763303XX	60991	DSP320CM10BUX
5962-8763303XX	01295	SMJ320CM10FDM
5962-8763304QX	60991	DSP320CM10-25BQX
5962-8763304QX	01295	SMJ320CM10-25JDM
5962-8763304XX	60991	DSP320CM10-25BUX
5962-8763304XX	01295	SMJ320CM10-25FDM
5962-8763305QX	60991	DSP320CF10-25BQX
5962-8763305QX	01295	SMJ320C10-25JDM
5962-8763305XX	60991	DSP320CF10-25BUX
5962-8763305XX	01295	SMJ320C10-25FDM
5962-87633060X	01295	SMJ320E15JDM
5962-87633070X	01295	SMJ320C15JDM
5962-8763307XX	01295	SMJ320C15FDM
5962-87633080X	01295	SMJ320C15-25JDM
5962-8763308XX	01295	SMJ320C15-25FDM

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Incorporated 13500 N. Central Expressway P.O. Box 655303 Dallas, TX 75265 Point of contact: I-20 at FM 1788 Midland, TX 79711-0448
60991	Microchip Technology 2355 W. Chandler Boulevard Chandler, AZ 85224-6199