

REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Added device type 04. Technical changes were implemented. Editorial changes throughout.	92-05-06	Monica L. Poelking
B	Added device types 05, 06, and 07. Technical changes to table I. Editorial changes throughout.	94-03-03	Monica L. Poelking

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

REV	B																			
SHEET	55																			
REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B
SHEET	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54
REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34
REV STATUS OF SHEETS				REV		B	B	B	B	B	B	B	B	B	B	B	B	B	B	B
				SHEET		1	2	3	4	5	6	7	8	9	10	11	12	13	14	
PMIC N/A				PREPARED BY Todd D. Creek						DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444										
STANDARDIZED MILITARY DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A				CHECKED BY Ray Monnin						MICROCIRCUIT, DIGITAL, CMOS, 16-BIT, MIL-STD-1750 MICROPROCESSOR, MONOLITHIC SILICON										
				APPROVED BY Michael A. Frye																
				DRAWING APPROVAL DATE 89-03-01						SIZE A	CAGE CODE 67268	5962-87665								
				REVISION LEVEL B						SHEET	1	OF	55							

DESC FORM 193
JUL 91

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

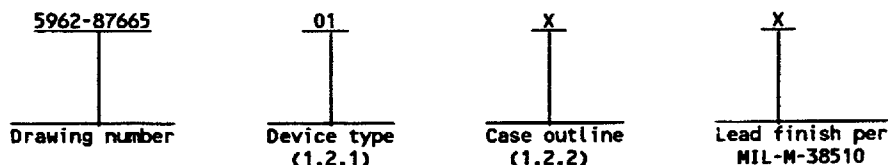
5962-E052-94

74E ■ 9004708 0000096 131 ■

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:



1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Speed
01	P1750A-15	16-bit microprocessor	15 MHz
02	P1750A-20	16-bit microprocessor	20 MHz
03	P1750A-30	16-bit microprocessor	30 MHz
04	P1750A-40	16-bit microprocessor	40 MHz
05	P1750AE-20	16-bit microprocessor	20 MHz
06	P1750AE-30	16-bit microprocessor	30 MHz
07	P1750AE-40	16-bit microprocessor	40 MHz

1.2.2 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
T	See figure 1	64	Dual-in-line with gull-wing leads
U	See figure 2	68	Leaded chip carrier with unformed leads
X	See figure 3	64	Dual-in-line
Y	See figure 4	68	Leaded chip carrier with gull-wing leads
Z	See figure 5	68	Pin grid array

1.3 Absolute maximum ratings.

Supply voltage range (V_{CC})	-0.5 V dc to +7.0 V dc
Input voltage range	-0.5 V dc to $V_{CC} + 0.5$ V dc
Storage temperature range	-65°C to +150°C
Input current range	-30 mA to +5 mA
Voltage applied to inputs range	-0.5 V dc to $V_{CC} + 0.5$ V dc
Current applied to any output	100 mA
Maximum power dissipation (P_D)	1.5 W ^{1/}
Lead temperature range (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (Θ_{JC}):	
Cases T and X	8°C/W
Cases U and Y	5°C/W
Case Z	6°C/W

1.4 Recommended operating conditions.

Supply voltage range	4.5 V dc to 5.5 V dc
Case operating temperature range (T_C)	-55°C to +125°C
Operating worst case power dissipation (outputs open):	
Device type 01	0.25 W at 15 MHz
Device type 02	0.30 W at 20 MHz
Device type 03	0.35 W at 30 MHz
Device type 04	0.40 W at 40 MHz
Device type 05	0.40 W at 20 MHz
Device type 06	0.50 W at 30 MHz
Device type 07	0.60 W at 40 MHz

^{1/} Must withstand the added P_D due to short circuit test; e.g., I_{OS} .

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-87665
		REVISION LEVEL B	SHEET 2

DESC FORM 193A
JUL 91

74E 9004708 0000097 078

2. APPLICABLE DOCUMENTS

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-1835 - Microcircuit Case Outlines.
MIL-STD-1750 - 16 Bit Instruction Set Architecture

BULLETIN MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 6.

3.2.3 Functional block diagram. The functional block diagram shall be as specified on figure 7.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-EC shall be required in accordance with MIL-STD-883 (see 3.1 herein).

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-87665
		REVISION LEVEL B	SHEET 3

DESC FORM 193A
JUL 91

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $4.5 \text{ V} \leq V_{CC} \leq 5.5 \text{ V}$ $-55^\circ\text{C} \leq T_C \leq +125^\circ\text{C}$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Input high level voltage	V_{IH}		1, 2, 3	ALL	2.0	$V_{CC} + 0.5 \text{ V}$	V
Input low level voltage	V_{IL}		1, 2, 3	ALL	-0.5	0.8	V
Input clamp diode voltage	V_{CD}	$V_{CC} = 4.5 \text{ V}$, $I_{IN} = -18 \text{ mA}$	1, 2, 3	ALL		-1.2	V
High level output voltage	V_{OH}	$I_{OH} = -8.0 \text{ mA}$, $V_{CC} = 4.5 \text{ V}$	1, 2, 3	ALL	2.4		V
		$I_{OH} = -300 \mu\text{A}$, $V_{CC} = 4.5 \text{ V}$	1, 2, 3	ALL	$V_{CC} - 0.2$		V
Low level output voltage	V_{OL}	$I_{OL} = 8.0 \text{ mA}$, $V_{CC} = 4.5 \text{ V}$	1, 2, 3	ALL		0.5	V
		$I_{OL} = 300 \mu\text{A}$, $V_{CC} = 4.5 \text{ V}$	1, 2, 3	ALL		0.2	V
High level input current, except IB_0 - IB_{15} , <u>BUS BUSY</u> , <u>BUS LOCK</u>	I_{IH1}	$V_{IN} = V_{CC}$, $V_{CC} = 5.5 \text{ V}$	1, 2, 3	ALL		10	μA
High level input current, IB_0 - IB_{15} , <u>BUS BUSY</u> , <u>BUS LOCK</u>	I_{IH2}	$V_{IN} = V_{CC}$, $V_{CC} = 5.5 \text{ V}$	1, 2, 3	ALL		50	μA
Low level input current, except IB_0 - IB_{15} , <u>BUS BUSY</u> , <u>BUS LOCK</u>	I_{IL1}	$V_{IN} = \text{GND}$, $V_{CC} = 5.5 \text{ V}$	1, 2, 3	ALL		-10	μA
Low level input current, IB_0 - IB_{15} , parity/ IB_{16} , <u>BUS BUSY</u> , <u>BUS LOCK</u>	I_{IL2}	$V_{IN} = \text{GND}$, $V_{CC} = 5.5 \text{ V}$	1, 2, 3	ALL		-50	μA
Output three-state current	I_{OZH}	$V_{OUT} = 2.4 \text{ V}$, $V_{CC} = 5.5 \text{ V}$	1, 2, 3	ALL		50	μA

See footnotes at end of table.

STANDARDIZED
MILITARY DRAWING
DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

SIZE
A

5962-87665

REVISION LEVEL
B

SHEET

4

DESC FORM 193A
JUL 91

74E ■ 9004708 0000099 940 ■

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 4.5 V ≤ V _{CC} ≤ 5.5 V -55°C ≤ T _C ≤ +125°C unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Output three-state current	I _{OZL}	V _{OUT} = 0.5 V, V _{CC} = 5.5 V	1, 2, 3	All		-50	μA
Quiescent power supply current (CMOS input levels)	I _{CCQC}	V _{IN} < 0.2 V or V _{IN} > V _{CC} - 0.2 V, f = 0 MHz, outputs open, V _{CC} = 5.5 V	1, 2, 3	01,02 03,04		10	mA
				05, 06,07		20	
Quiescent power supply current (TTL input levels)	I _{CCQT}	V _{IN} = 3.4 V, f = 0 MHz, outputs open, V _{CC} = 5.5 V	1, 2, 3	All		50	mA
Dynamic power supply current	I _{CCD}	V _{IN} = 0 V to V _{CC} , t _r = t _f = 2.5 ns nominal, Outputs open, V _{CC} = 5.5 V	1, 2, 3	01		40	mA
				02		50	
				03		60	
				04		70	
				05		70	
				06		85	
				07		100	
Output short circuit current	I _{OS}	V _{OUT} = GND, 1/ V _{CC} = 5.5 V	1, 2, 3	All	-25		mA
Input capacitance	C _{IN}	See 4.3.1c	4	All		10	pF
Output capacitance	C _{OUT}		4	All		15	pF
Bidirectional capacitance	C _{I/O}		4	All		15	pF
Functional tests		See 4.3.1d	7, 8				
BUS REQ	t _{C(BR)L}	See figure 8 2/ V _{CC} = 4.5 V	9, 10, 11	01		45	ns
				02		33	
				03			
				05,06		25	
				04,07		22	
BUS REQ	t _{C(BR)H}		9, 10, 11	01		45	
				02		33	
				03			
				05,06		25	
				04,07		22	

See footnotes at end of table.

STANDARDIZED
MILITARY DRAWING
DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

SIZE
A

5962-87665

REVISION LEVEL
B

SHEET
5

TABLE 1. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 4.5 V $\leq$ V _{CC} $\leq$ 5.5 V -55°C $\leq$ T _C $\leq$ +125°C unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
BUS GNT setup	t _{BGy(C)}	See figure 8 2/ V _{CC} = 4.5 V	9, 10, 11	01	5		ns
				02	5		
				03			
				05,06	5		
				04,07	5		
BUS GNT hold	t _{C(BG)X}		9, 10, 11	01	5		
				02	5		
				03			
				05,06	5		
				04,07	5		
BUS BUSY low	t _{C(BB)L}		9, 10, 11	01		35	
				02		25	
				03			
				05,06		24	
				04,07		20	
BUS BUSY high	t _{C(BB)H}		9, 10, 11	01		35	
				02		25	
				03			
				05,06		20	
				04,07		15	
BUS BUSY setup	t _{BBV(C)}		9, 10, 11	01	5		
				02	5		
				03			
				05,06	5		
				04,07	5		
BUS BUSY hold	t _{C(BB)X}		9, 10, 11	01	5		
				02	5		
				03			
				05,06	5		
				04,07	5		
BUS LOCK low	t _{C(BL)L}		9, 10, 11	01		50	
				02		30	
				03			
				05,06		25	
				04,07		21	

See footnotes at end of table.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-87665
		REVISION LEVEL B	SHEET 6

DESC FORM 193A
JUL 91

74E ■ 9004708 0000101 329 ■

TABLE 1. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $4.5 \text{ V} \leq V_{CC} \leq 5.5 \text{ V}$ $-55^\circ\text{C} \leq T_C \leq +125^\circ\text{C}$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
BUS LOCK high	$t_{C(BL)H}$	See figure 8 2/ $V_{CC} = 4.5 \text{ V}$	9, 10, 11	01		50	ns
				02		30	
				03		20	
				05,06		20	
				04,07		17	
BUS LOCK setup	$t_{BLV(C)}$		9, 10, 11	01	5		
				02	5		
				03			
				05,06	5		
				04,07	5		
BUS LOCK hold	$t_{C(BL)X(IN)}$		9, 10, 11	01	5		
				02	5		
				03			
				05,06	5		
				04,07	5		
M/ $\overline{IO}$, R/ $\overline{W}$ status	$t_{C(ST)V}$		9, 10, 11	01		45	
				02		30	
				03			
				05,06		25	
				04,07		20	
AS ₀ -AS ₃ , AK ₀ -AK ₃ , D/ $\overline{I}$ status	$t_{C(ST)V}$		9, 10, 11	01		40	
				02		25	
				03			
				05,06		20	
				04,07		20	
STRBA high	$t_{C(SA)H}$		9, 10, 11	01		25	
				02		22	
				03			
				05,06		17	
				04,07		16	
STRBA low	$t_{C(SA)L}$		9, 10, 11	01		25	
				02		22	
				03			
				05,06		17	
				04,07		16	

See footnotes at end of table.

STANDARDIZED
MILITARY DRAWING
DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

SIZE
A

5962-87665

REVISION LEVEL
B

SHEET

7

DESC FORM 193A
JUL 91

74E ■ 9004708 0000102 265 ■

TABLE 1. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$ $-55^\circ\text{C} \leq T_C \leq +125^\circ\text{C}$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Address hold from STRBA low	$t_{SAL(1BA)X}$	See figure 8 2/ $V_{CC} = 4.5\text{ V}$	9, 10, 11	01	5		ns
				02	5		
				03			
				05,06	5		
				04,07	5		
RDYA setup	$t_{RAV(C)}$		9, 10, 11	01	5		
				02	5		
				03			
				05,06	5		
				04,07	5		
RDYA hold	$t_{C(RA)X}$		9, 10, 11	01	5		
				02	5		
				03			
				05,06	5		
				04,07	5		
STRBD low write	$t_{C(SDW)L}$		9, 10, 11	01		25	
				02		22	
				03			
				05,06		17	
				04,07		14	
STRBD high	$t_{C(SD)H}$		9, 10, 11	01		25	
				02		22	
				03			
				05,06		17	
				04,07		14	
STRBD low read	$t_{C(SDR)L}$		9, 10, 11	01		25	
				02		22	
				03			
				05,06		17	
				04,07		14	
STRBD high	$t_{(SDR)HIBDX}$		9, 10, 11	01	0		
				02	0		
				03			
				05,06	0		
				04,07	0		

See footnotes at end of table.

STANDARDIZED
MILITARY DRAWING
DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

SIZE
A

5962-87665

REVISION LEVEL
B

SHEET
8

DESC FORM 193A
JUL 91

74E ■ 9004708 0000103 1T1 ■

TABLE 1. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$ $-55^{\circ}\text{C} \leq T_C \leq +125^{\circ}\text{C}$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
STRBD high	$t_{SDWH(1BD)X}$	See figure 8 2/ $V_{CC} = 4.5\text{ V}$	9, 10, 11	01	45		ns
				02	30		
				03			
				05,06	25		
				04,07	17		
STRBD write	$t_{SDL(SDH)}$		9, 10, 11	01	50		
				02	40		
				03			
				05,06	26		
				04,07	20		
RDYD setup	$t_{RDV(C)}$		9, 10, 11	01	5		
				02	5		
				03			
				05,06	5		
				04,07	5		
RDYD hold	$t_{C(RD)X}$		9, 10, 11	01	5		
				02	5		
				03			
				05,06	5		
				04,07	5		
IB_0 - IB_{15}	$t_{C(1BA)V}$		9, 10, 11	01		45	
				02		30	
				03			
				05,06		25	
				04,07		20	
IB_0 - IB_{15}	$t_{FC(1BA)X}$		9, 10, 11	01	0		
				02	0		
				03			
				05,06	0		
				04,07	0		
IB_0 - IB_{15} setup	$t_{IBDRV(C)}$		9, 10, 11	01	5		
				02	5		
				03			
				05,06	5		
				04,07	5		

See footnotes at end of table.

STANDARDIZED
MILITARY DRAWING
DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

SIZE
A

5962-87665

REVISION LEVEL
B

SHEET

9

DESC FORM 193A
JUL 91

74E ■ 9004708 0000104 038 ■

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$ $-55^{\circ}\text{C} \leq T_C \leq +125^{\circ}\text{C}$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
IB_0 - IB_{15} hold (read)	$t_{C(IBD)X}$	See figure 8 2/ $V_{CC} = 4.5\text{ V}$	9, 10, 11	01	8		ns
				02	7		
				03			
				05,06	6		
				04,07	5		
Data valid out (write)	$t_{C(IBD)X}$		9, 10, 11	01	0		
				02	0		
				03			
				05,06	0		
				04,07	0		
IB_0 - IB_{15}	$t_{FC(IBD)V}$		9, 10, 11	01		45	
				02		30	
				03			
				05,06		25	
				04,07		20	
SNEW	$t_{C(SNW)}$		9, 10, 11	01		45	
				02		30	
				03			
				05,06		26	
				04,07		22	
TRIGO RST	$t_{FC(TGO)}$		9, 10, 11	01		45	
				02		30	
				03			
				05,06		26	
				04,07		22	
DMA enable	$t_{RSTL(DMA ENL)}$		9, 10, 11	01		45	
				02		40	
				03			
				05,06		35	
				04,07		30	
DMA enable	$t_{C(DME)}$		9, 10, 11	01		45	
				02		40	
				03			
				05,06		35	
				04,07		30	

See footnotes at end of table.

STANDARDIZED
MILITARY DRAWING
DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

SIZE
A

5962-87665

REVISION LEVEL
B

SHEET
10

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$ $-55^{\circ}\text{C} \leq T_C \leq +125^{\circ}\text{C}$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Normal power up	$t_{FC(NPU)}$	See figure 8 2/ $V_{CC} = 4.5\text{ V}$	9, 10, 11	01		45	ns
				02		40	
				03			
				05,06		35	
				04,07		30	
Clock to major error unrecoverable	$t_{C(ER)}$		9, 10, 11	01		75	
				02		60	
				03			
				05,06		50	
				04,07		45	
$\overline{\text{RESET}}$	$t_{RSTL(NPU)}$		9, 10, 11	01		65	
				02		50	
				03			
				05,06		40	
				04,07		30	
Console request	$t_{REQV(C)}$		9, 10, 11	01	0		
				02	0		
				03			
				05,06	0		
				04,07	0		
Console request	$t_{C(REQ)X}$		9, 10, 11	01	10		
				02	10		
				03			
				05,06	10		
				04,07	10		
Level sensitive faults	$t_{FV(BB)H}$		9, 10, 11	01	5		
				02	5		
				03			
				05,06	5		
				04,07	5		
Level sensitive faults	$t_{BBH(F)X}$		9, 10, 11	01	5		
				02	5		
				03			
				05,06	5		
				04,07	5		

See footnotes at end of table.

STANDARDIZED
MILITARY DRAWING
DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

SIZE
A

5962-87665

REVISION LEVEL
B

SHEET
11

DESC FORM 193A
JUL 91

74E ■ 9004708 0000106 900 ■

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$ $-55^\circ\text{C} \leq T_C \leq +125^\circ\text{C}$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
IOL ₁₋₂ INT setup user interrupt (0-5)	$t_{IRV(C)}$	See figure 8 2/ $V_{CC} = 4.5\text{ V}$	9, 10, 11	01	0		ns
				02	0		
				03,04	0		
				05			
				06,07	10		
Power down interrupt level sensitive hold	$t_{C(IR)X}$		9, 10, 11	01	10		
				02	10		
				03			
				05,06	10		
				04,07	10		
Reset pulse width	$t_{RSTL}(t_{RSTH})$		9,10,11	01	30		
				02	25		
				03			
				05,06	20		
				04,07	15		
Clock to three- state	$t_{C(XX)Z}$		9, 10, 11	01		30	
				02		22	
				03			
				05,06		17	
				04,07		13	
M/ $\overline{IO}$, R/ $\overline{W}$, AS ₀ -AS ₃ AK ₀ -AK ₃ , D/ $\overline{I}$ status	$t_{C(ST)X}$		9, 10, 11	All	0		
Edge sensitive pulse width	$t_{f(F)}, t_{l(1)}$		9, 10, 11	All	5		
Clock rise and fall	t_r, t_f		9, 10, 11	All		5	

1/ Only one output may be shorted at a time.

2/ All timing parameters are composed of Three elements. The first "t" stands for timing. The second represents the "from" signal. The third in parentheses indicates "to" signal. When the CPU clock is one of the signal elements, either the rising edge "C" or the falling edge "FC" is referenced. When other elements are used, an additional suffix indicates the final logic level of the signal. "L"-low level, "H"-high level, "V"-valid, "Z"-high impedance, "X"-don't care, "LH"-low to high, "ZH"-high impedance to high, "R"-read cycle, and "W"-write cycle.

STANDARDIZED
MILITARY DRAWING
DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

SIZE
A

5962-87665

REVISION LEVEL
B

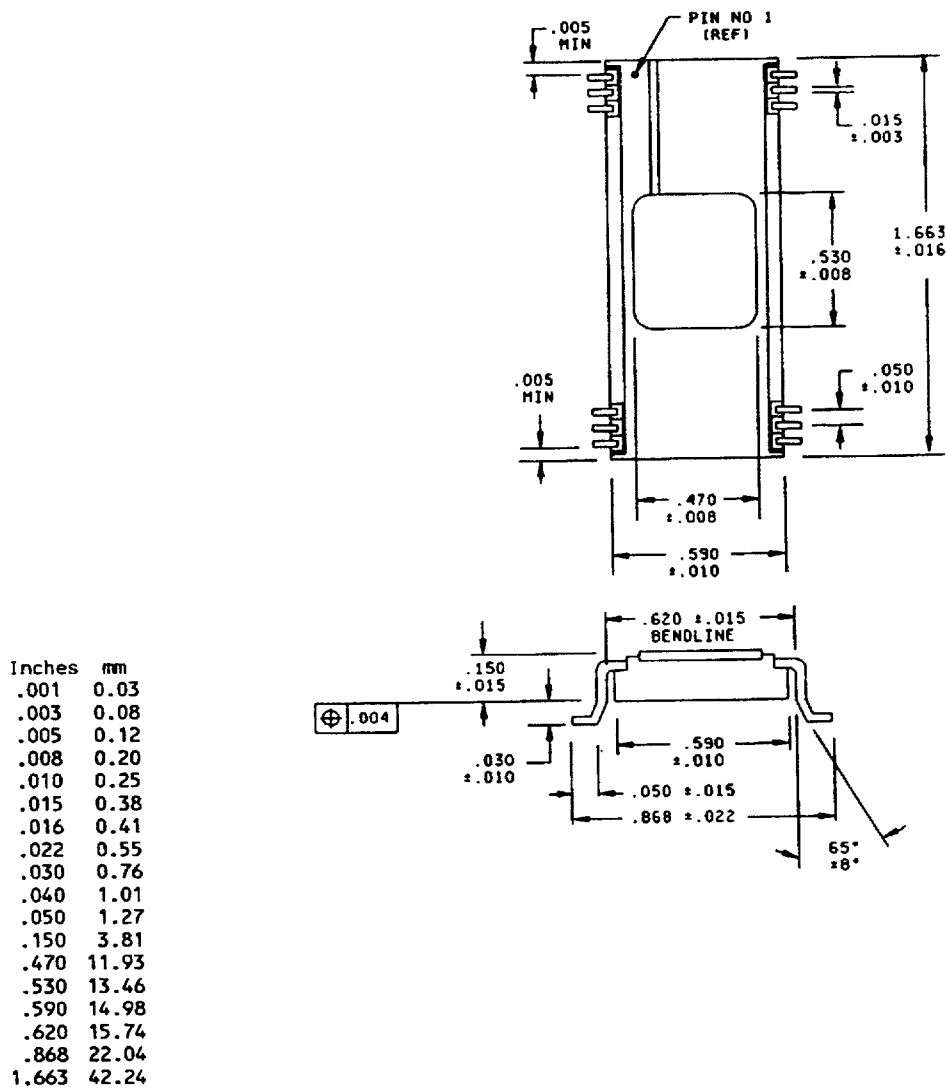
SHEET

12

DESC FORM 193A
JUL 91

74E ■ 9004708 0000107 847 ■

Device types 01, 02, 03, 04 and 05



NOTES:

1. Dimensions are in inches.
2. Metric equivalents are given for general information only.
3. Unless otherwise specified, tolerances are .02 (0.5 mm) for two place decimals and .005 (0.13 mm) for three place decimals.
4. Case T is derived from Case X by forming the leads to the shown gullwing configuration.

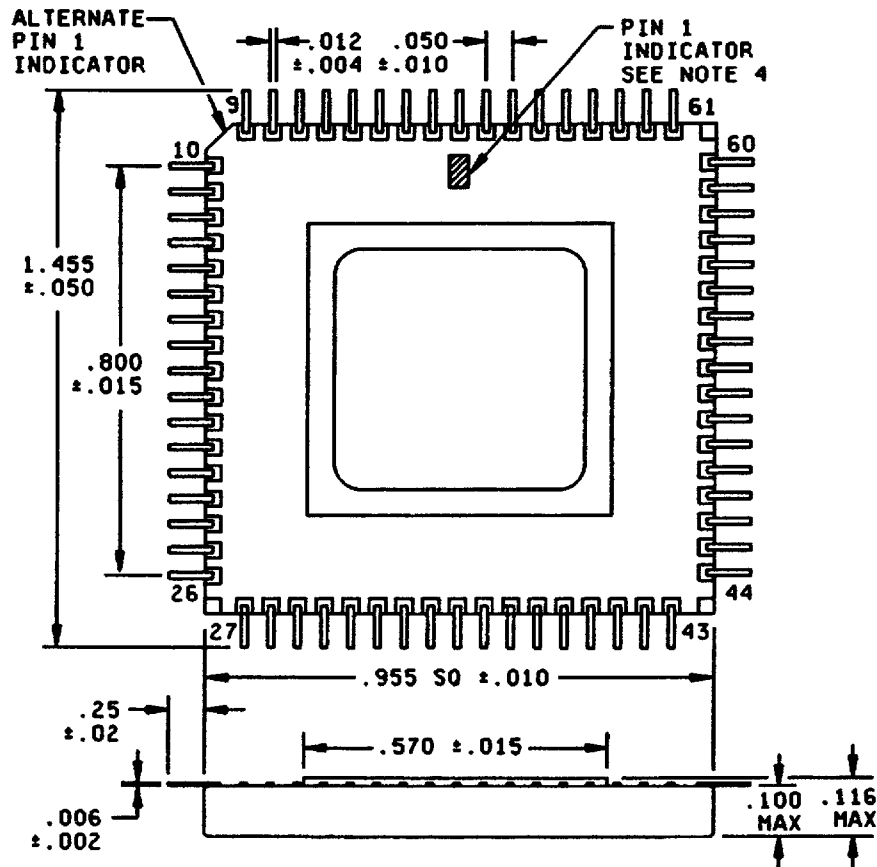
FIGURE 1. Case outline I.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-87665
		REVISION LEVEL B	SHEET 13

DESC FORM 193A
JUL 91

74E ■ 9004708 0000108 783 ■

All device types



Inches	mm
.002	0.05
.004	0.10
.006	0.15
.010	0.25
.012	0.30
.02	0.5
.020	0.51
.050	1.27
.100	2.54
.116	2.95
.25	6.4
.560	14.22
.570	14.48
.800	20.32
.955	24.25
1.090	27.69

NOTES:

1. Dimensions are in inches.
2. Metric equivalents are given for general information only.
3. Unless otherwise specified, tolerances are .02 (0.5 mm) for two place decimals and .005 (0.13 mm) for three place decimals.
4. Pin 1 indicator can be either rectangle, dot, or triangle at specified location or referenced to the uniquely beveled corner.
5. Corners indicated as notched may be either notched or square.

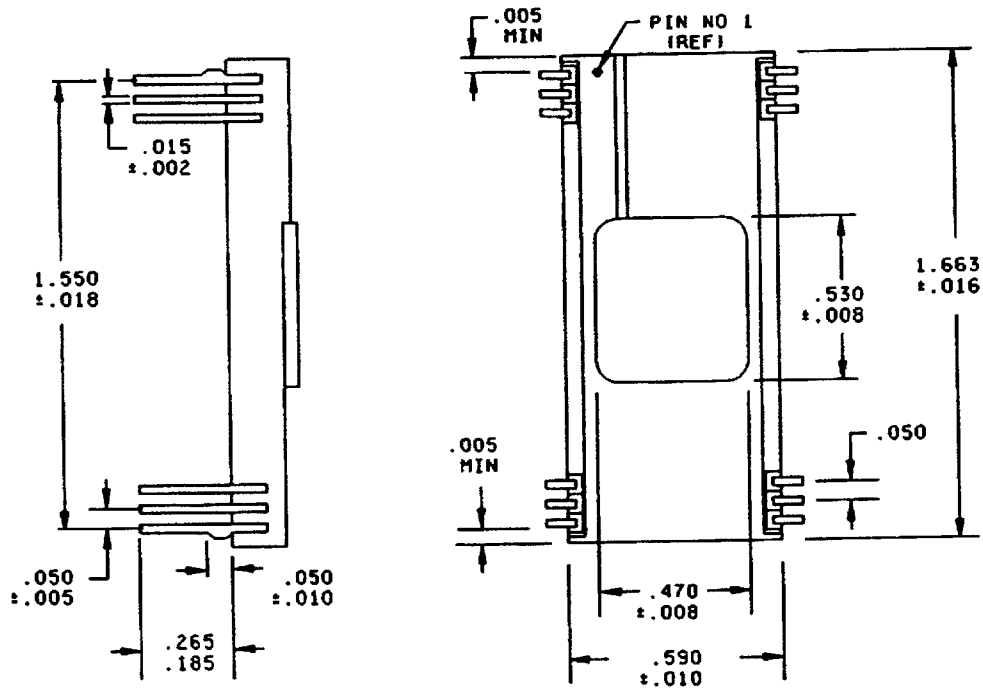
FIGURE 2. Case outline U.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-87665
		REVISION LEVEL B	SHEET 14

DESC FORM 193A
JUL 91

74E ■ 9004708 0000109 61T ■

Device types 01, 02, 03, 04 and 05



Inches	mm
.002	0.05
.005	0.12
.008	0.20
.010	0.25
.015	0.38
.016	0.40
.018	0.45
.025	0.63
.040	1.01
.050	1.27
.185	4.70
.265	6.73
.470	11.93
.530	13.46
.590	14.98
.620	15.74
.645	16.38
1.550	39.37
1.563	39.70

NOTES:

1. Dimensions are in inches.
2. Metric equivalents are given for general information only.
3. Unless otherwise specified, tolerances are .02 (0.5 mm) for two place decimals and .005 (0.13 mm) for three place decimals.

FIGURE 3. Case outline X.

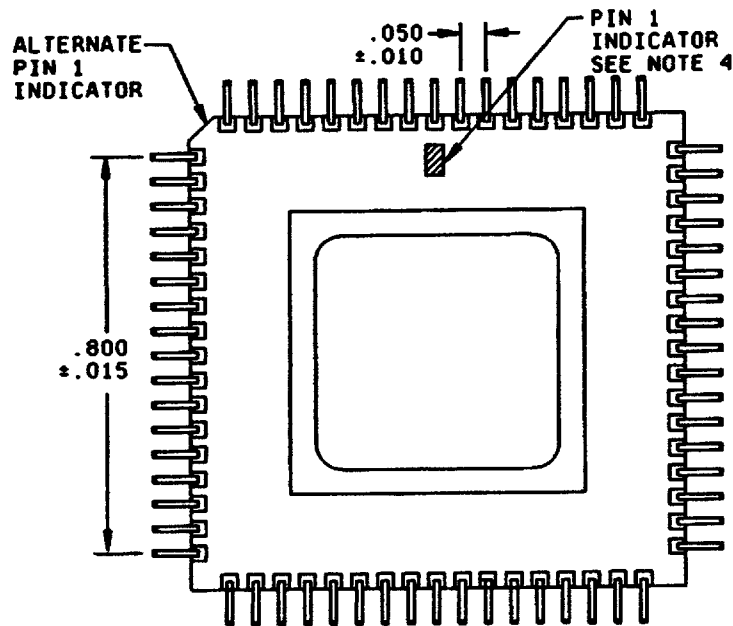
STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-87665
		REVISION LEVEL B	SHEET 15

DESC FORM 193A

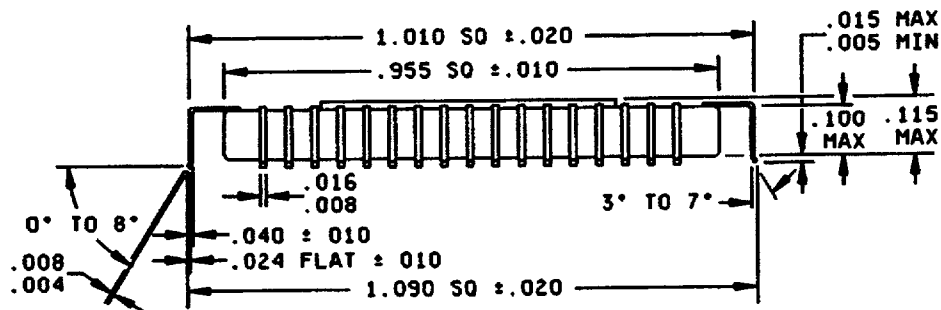
JUL 91

74E ■ 9004708 0000110 331 ■

All device types



Inches	mm
.004	0.10
.005	0.12
.008	0.20
.010	0.25
.012	0.30
.015	0.38
.016	4.06
.020	0.50
.024	0.60
.040	1.02
.050	1.27
.100	2.54
.115	2.92
.570	14.48
.800	20.32
.955	24.25
1.010	25.65
1.090	27.68



NOTES:

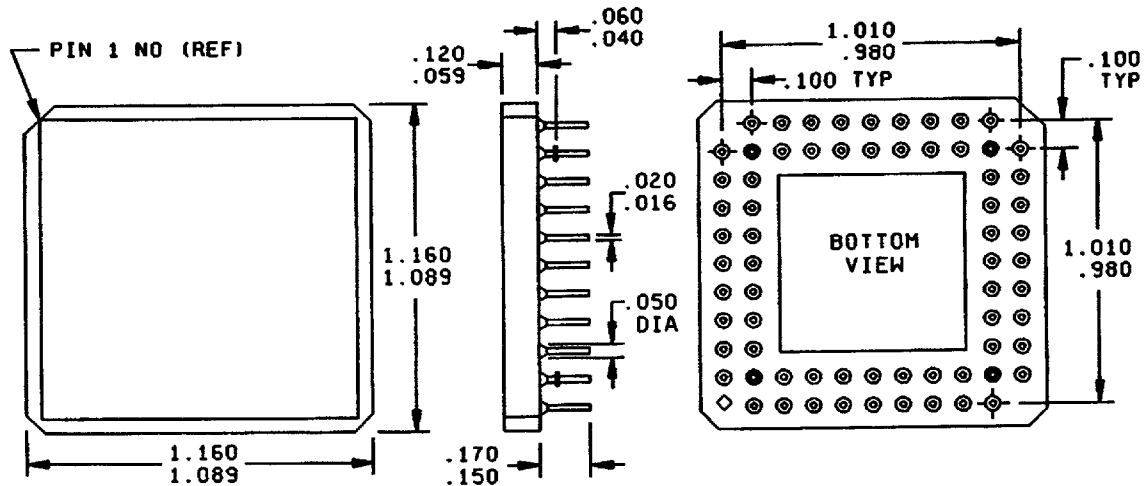
1. Dimensions are in inches.
2. Metric equivalents are given for general information only.
3. Unless otherwise specified, tolerances are .02 (0.5 mm) for two place decimals and .005 (0.13 mm) for three place decimals.
4. Pin 1 indicator can be either rectangle, dot or triangle at specified location or referenced to the uniquely beveled corner.
5. Corners indicated as notched may be either notched or square (with radius).
6. Case Y is derived from Case U by forming the leads to the shown gullwing configuration

FIGURE 4. Case outline Y.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-87665
		REVISION LEVEL B	SHEET 16

DESC FORM 193A
JUL 91

All device types



Inches	mm
.016	4.06
.020	0.50
.040	1.01
.050	1.27
.059	1.49
.060	1.52
.098	2.49
.100	2.54
.120	3.04
.150	3.81
.170	4.32
1.010	25.65
1.089	27.66
1.160	29.46

NOTES:

1. Dimensions are in inches.
2. Metric equivalents are given for general information only.
3. Unless otherwise specified, tolerances are .02 (0.5 mm) for two place decimals and .005 (0.13 mm) for three place decimals.
4. Corners except pin number 1 (ref.) can be either rounded or square.
5. All pins must be on the .100" grid.

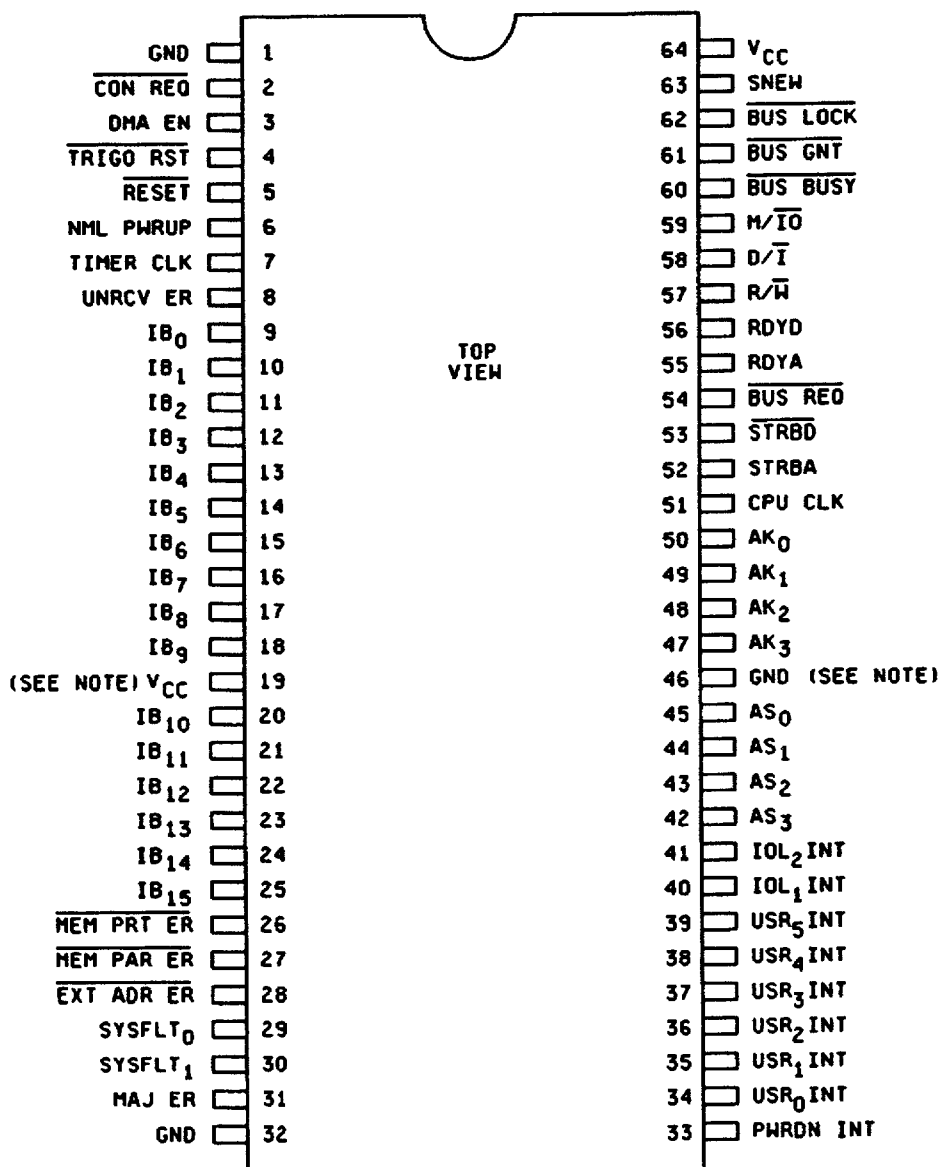
FIGURE 5. Case outline Z.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-87665
		REVISION LEVEL B	SHEET 17

DESC FORM 193A
JUL 91

74E ■ 9004708 0000112 104 ■

Cases X and T



NOTE: For device types 03, 04 and 05, cases X or T, pins 19 and 46 are connected as shown. For device types 01 and 02, cases X or T, these pins are not internally connected to the die.

FIGURE 6. Terminal connections.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-87665
		REVISION LEVEL B	SHEET 18

DESC FORM 193A
JUL 91

Cases U and Y

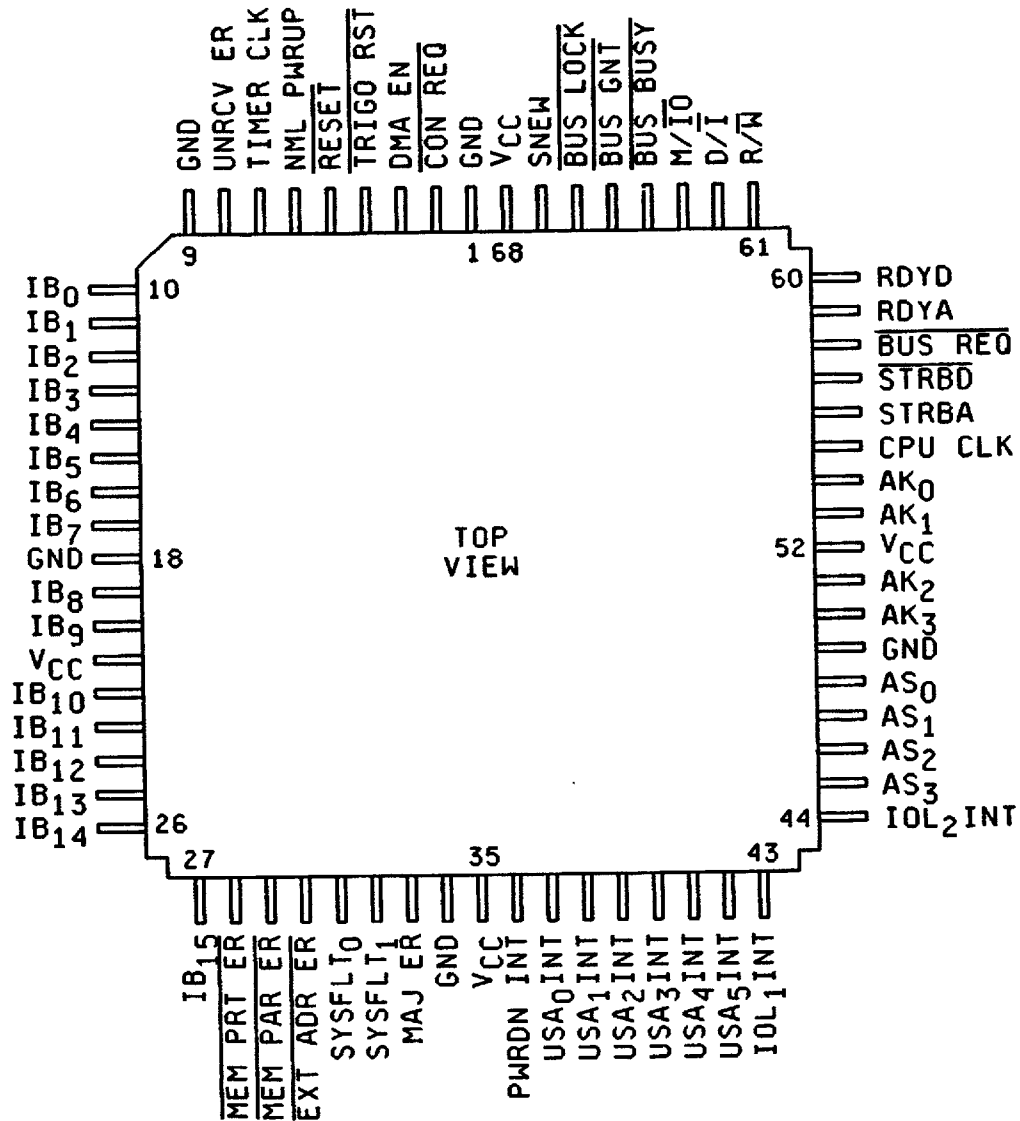


FIGURE 6. Terminal connections - Continued.

STANDARDIZED
MILITARY DRAWING
DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

SIZE
A

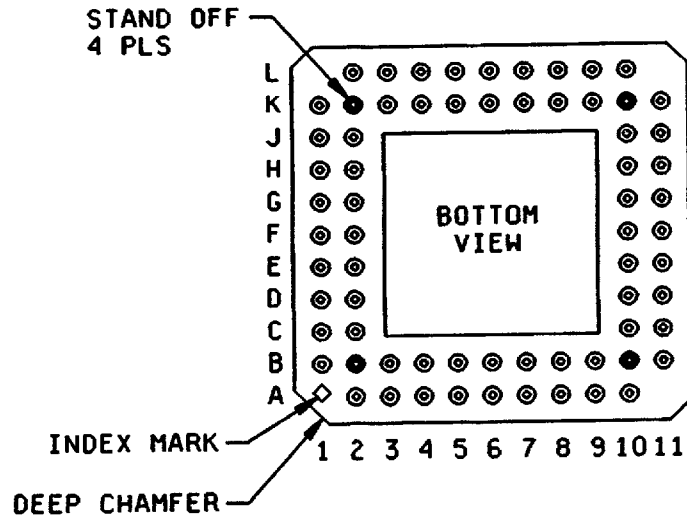
5962-87665

REVISION LEVEL
B

SHEET
19

DESC FORM 193A
JUL 91

74E 9004708 0000114 T87



Pin	Pin name	Pin	Pin name	Pin	Pin name	Pin	Pin name
B1	V _{CC}	L2	GND	K11	RDYD	A10	GND
B2	IB ₁₄	K2	UNRCV ER	K10	RDYA	B10	IOL ₁ INT
C1	IB ₁₃	L3	TIMER CLK	J11	BUS REQ	A9	USR ₅ INT
C2	IB ₁₂	K3	NML PWRUP	J10	STRBD	B9	USR ₄ INT
D1	IB ₁₁	L4	RESET	H11	STRBA	A8	USR ₃ INT
D2	IB ₁₀	K4	TRIGO RST	H10	CPU CLK	B8	USR ₂ INT
E1	IB ₉	L5	DMA EN	G11	AK ₀	A7	USR ₁ INT
E2	IB ₈	K5	CON REQ	G10	AK ₁	B7	USR ₀ INT
F1	GND	L6	V _{CC}	F11	AK ₂	A6	PWRDN INT
F2	IB ₇	K6	SNEW	F10	AK ₃	B6	GND
G1	IB ₆	L7	BUS LOCK	E11	GND	A5	MAJ ER
G2	IB ₅	K7	BUS GNT	E10	AS ₀	B5	SYSFLT ₁
H1	IB ₄	L8	BUS BUSY	D11	AS ₁	A4	SYSFLT ₀
H2	IB ₃	K8	M/I _O	D10	AS ₂	B4	EXT ADR ER
J1	IB ₂	L9	D/I	C11	AS ₃	A3	MEM PAR ER
J2	IB ₁	K9	R/W	C10	IOL ₂ INT	B3	MEM PRT ER
K1	IB ₀	L10	GND	B11	V _{CC}	A2	IB ₁₅

FIGURE 6. Terminal connections - Continued.

STANDARDIZED
MILITARY DRAWING
DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

SIZE
A

5962-87665

REVISION LEVEL
B

SHEET
20

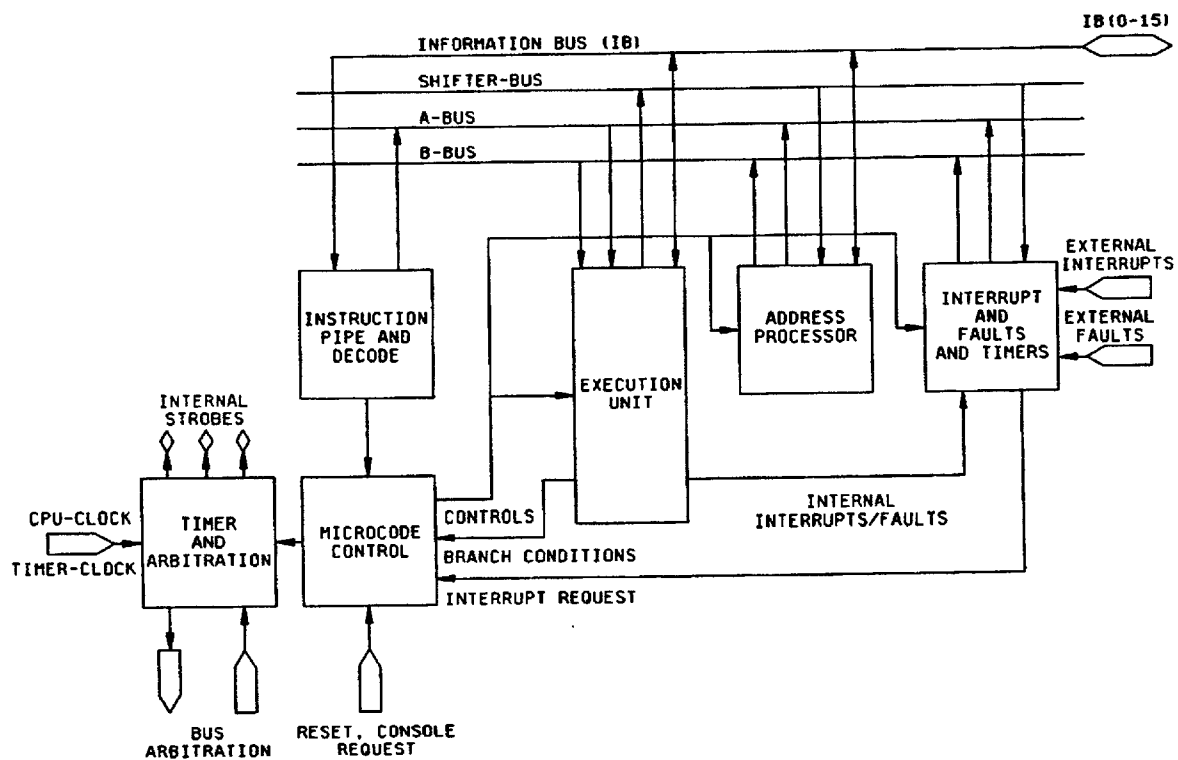


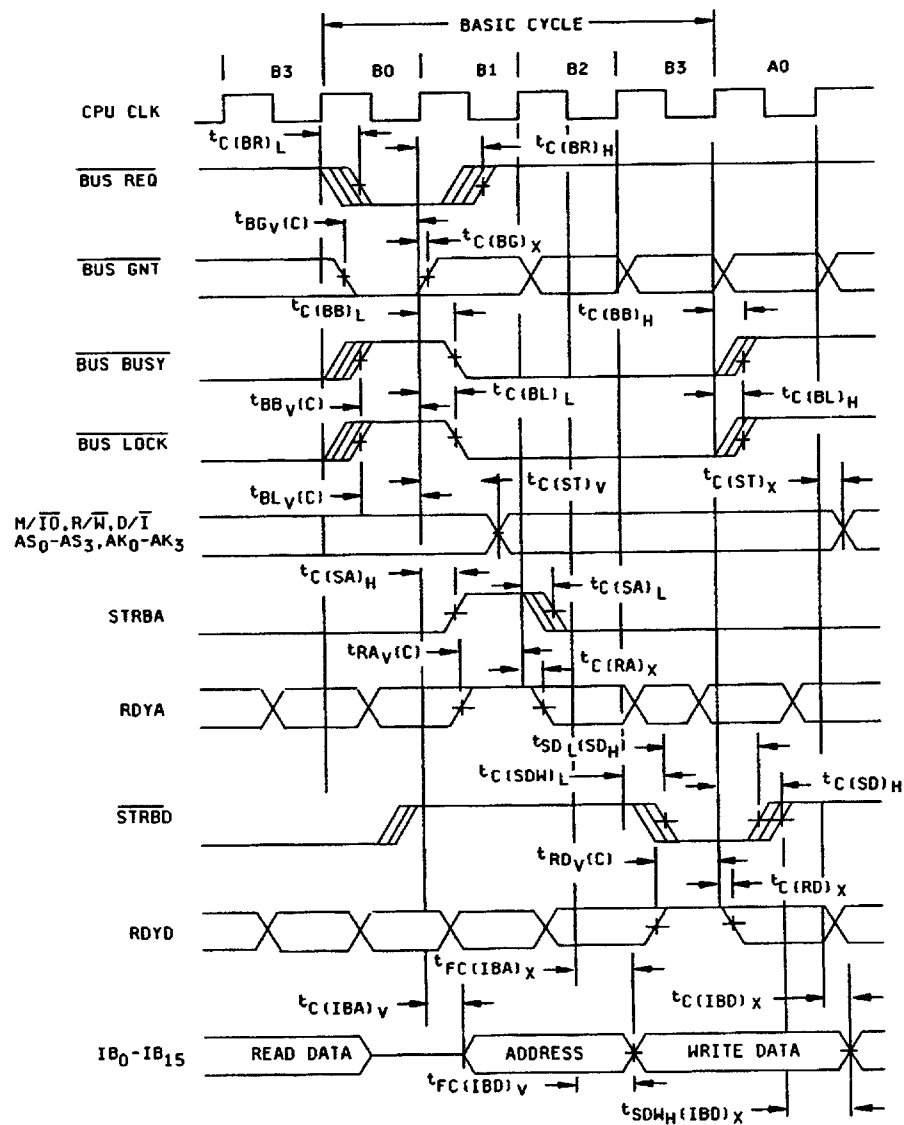
FIGURE 7. Functional block diagram.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-87665
		REVISION LEVEL B	SHEET 21

DESC FORM 193A
JUL 91

74E 9004708 0000116 85T

Minimum write bus cycle timing diagram.



NOTE: ALL time measurements on active signals relate to the 1.5 volt level.

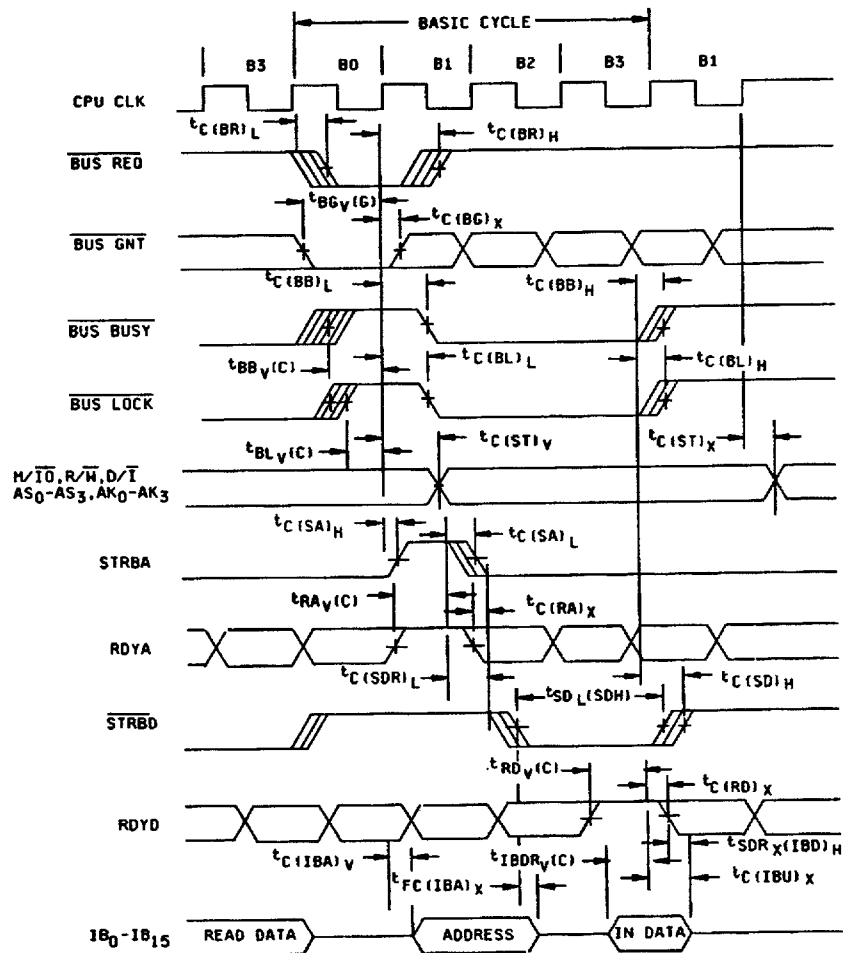
FIGURE 8. Timing diagram and ac test circuits.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-87665
		REVISION LEVEL B	SHEET 22

DESC FORM 193A
JUL 91

74E 9004708 0000117 796

Minimum read bus cycle timing diagram



NOTE: All time measurements on active signals relate to the 1.5 volt level.

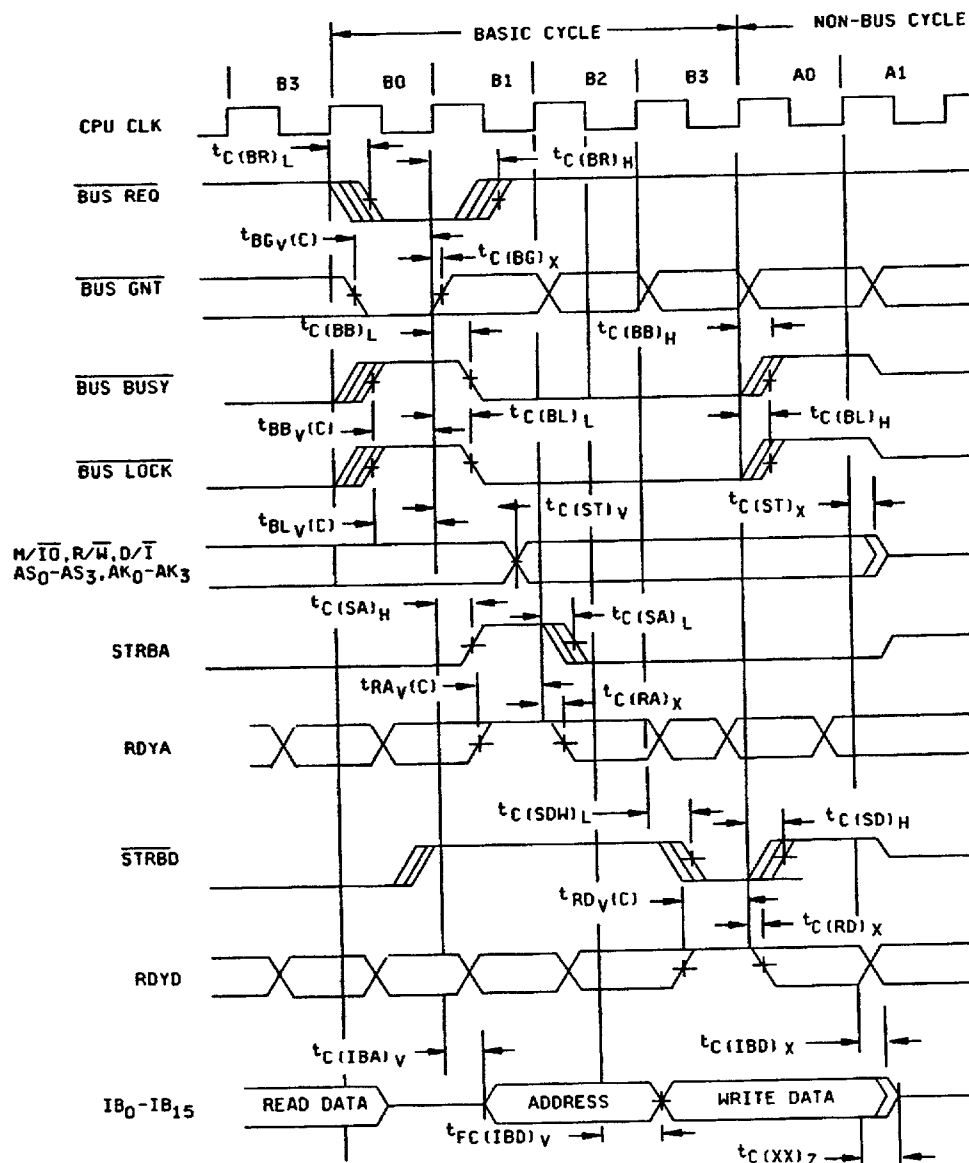
FIGURE 8. Timing diagram and ac test circuits - Continued.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-87665
		REVISION LEVEL B	SHEET 23

DESC FORM 193A
JUL 91

74E 9004708 0000118 622

Minimum write bus cycle, followed by a nonbus cycle, timing diagram.



NOTE: All time measurements on active signals relate to the 1.5 volt level.

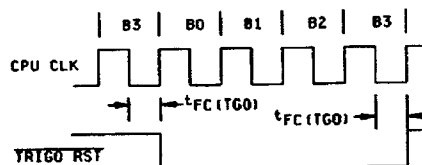
FIGURE 8. Timing diagram and ac test circuits - Continued.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-87665
		REVISION LEVEL B	SHEET 24

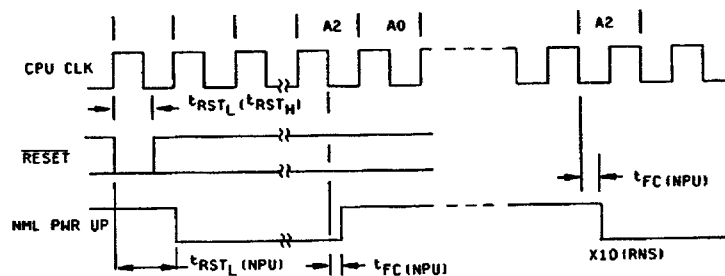
DESC FORM 193A
JUL 91

74E 9004708 0000119 569

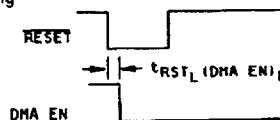
TRIG0 RST discrete timing diagrams



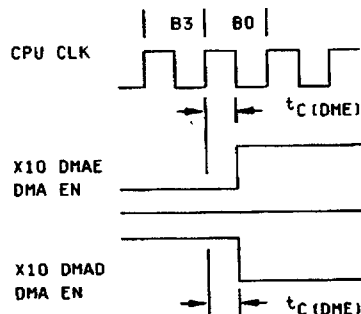
Normal power up discrete timing



DMA EN discrete timing



X10 operations



NOTE: All time measurements on active signals relate to the 1.5 volt level.

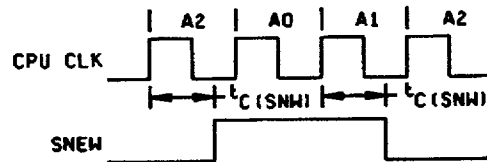
FIGURE 8. Timing diagrams and ac test circuits - Continued.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-87665
		REVISION LEVEL B	SHEET 25

DESC FORM 193A
JUL 91

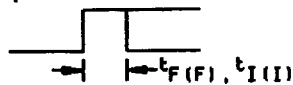
74E ■ 9004708 0000120 280 ■

SNEW discrete timing diagram

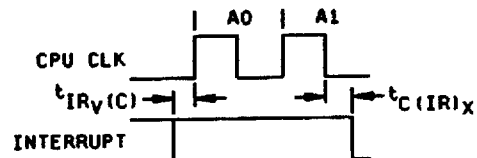


External faults and interrupts timing diagram

Edge-sensitive interrupts and faults (SYSFLT₀, SYSFLT₁) min. pulse width

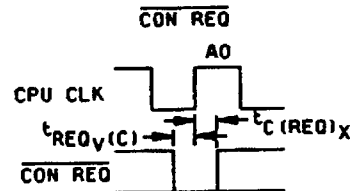
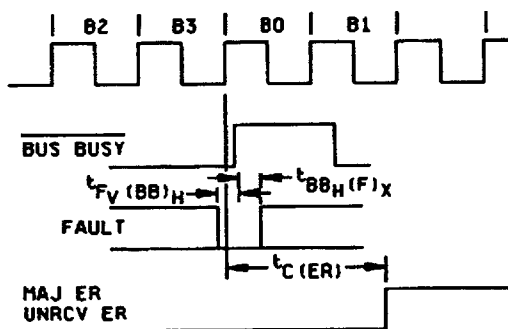


Level-sensitive interrupts



NOTE: $t_{C(IR)_X}$ max = 35 clocks

Level-sensitive faults



NOTE: All time measurements on active signals relate to the 1.5 volt level.

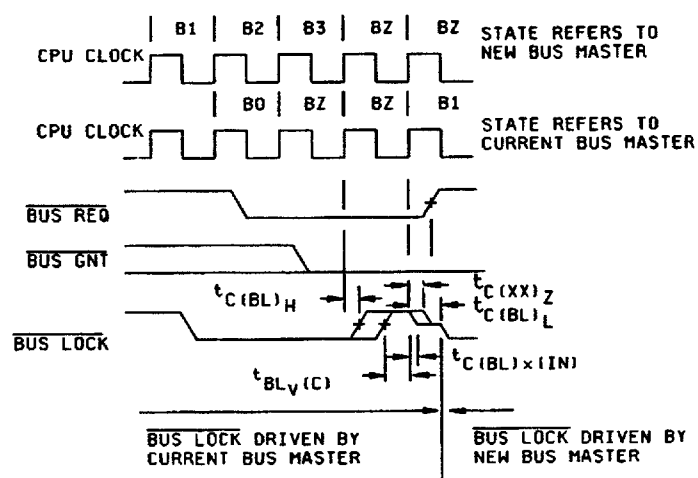
FIGURE 8. Timing diagrams and ac test circuits - Continued.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-87665
		REVISION LEVEL B	SHEET 26

DESC FORM 193A
JUL 91

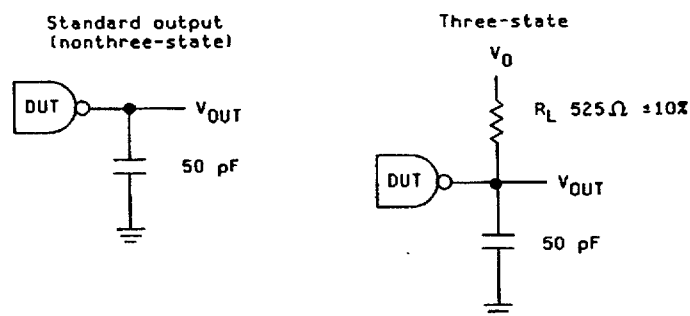
74E 9004708 0000121 117

BUS acquisition



NOTE: A CPU contending for the BUS, will assert the BUS REQ line, and will acquire it when BUS GNT is asserted and the BUS is not locked (BUS LOCK is high).

Switching time test circuits



Parameter	V_0	V_{MEA}
t_{PLZ}	≥ 3 V	.5 V
t_{PHZ}	0 V	$V_{CC} - .5$ V
t_{PXL}	$V_{CC}/2$	1.5 V
t_{PXH}	$V_{CC}/2$	1.5 V

NOTE: All time measurements on active signals relate to the 1.5 volt level.

FIGURE 8. Timing diagrams and ac test circuits - Continued.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-87665
		REVISION LEVEL B	SHEET 27

DESC FORM 193A
JUL 91

74E 74004708 0000122 053

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Certification. Certification to MIL-STD-1750A VSW test version 2.2 shall be required and the manufacturer shall be listed on Air Force VSW Compliant Computer List.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) $T_A = +125^{\circ}\text{C}$, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups in (accordance with method 5005, table)
Interim electrical parameters (method 5004)	1, 2, 7, 8a
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3, 7, 8, 9, 10, 11

* PDA applies to subgroup 1.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} , C_{OUT} , and $C_{I/O}$ measurements) shall be measured only for the initial test and after process or design changes which may affect input capacitance.

d. Subgroups 7 and 8 shall include verifying the functionality of the device. The functional test shall achieve at least 95 percent coverage of all detectable single stuck-at-zero and stuck-at-one logic faults. These tests form a part of the vendors test tape and shall be maintained and available from the approved sources of supply.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-87665
		REVISION LEVEL B	SHEET 28

DESC FORM 193A
JUL 91

74E ■ 9004708 0000123 T9T ■

4.3.2 Groups C and D inspections.

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady-state life test conditions, method 1005 of MIL-STD-883.
 - (1) Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.
 - (2) $T_A = +125^{\circ}\text{C}$, minimum.
 - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.
- c. For group D inspection only, electrical failures from subgroups 9, 10, 11 of Table I can be used for group D subgroups 3 and 4 provided; they have passed subgroups 1, 2, 3, 7, 8, the device built in functional test, been exposed to the full time/temperature exposure of burn-in and operate greater than or equal to 12 MHz. These devices shall be identified as non-shippable through the remainder of testing.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.5 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444, or telephone (513) 296-5377.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-87665
		REVISION LEVEL B	SHEET 29

DESC FORM 193A
JUL 91

74E ■ 9004708 0000124 926 ■

6.6 Pin descriptions.

<u>Mnemonic</u>	<u>Name</u>	<u>Description</u>
CPU CLK	CPU clock	A single phase input clock signal 0-40 MHz, 40 percent to 60 percent duty cycle.
TIMER CLK	Timer clock	A 100 kHz input that, after synchronization with CPU CLK provides the clock for timer A and timer B. If timers are used, the CPU CLK signal frequency must be > 300 kHz.
<u>RESET</u>	Reset	An active low input that initializes the device.
<u>CON REQ</u>	Console request	An active low input that initiates console operations after completion of the current instruction.
PWRDN INT	Power down interrupt	An interrupt request input that cannot be masked or disabled. This signal is active on the positive going edge or the high level, according to the interrupt mode bit in the configuration register.
USR ₀ INT- USR ₅ INT	User interrupt	Interrupt request input signals that are active on positive going edge or the high level, according to the interrupt mode bit in the configuration register
IOL ₁ INT IOL ₂ INT	I/O level interrupts	Active high interrupt request inputs that can be used to expand the number of user interrupts.
<u>MEM PRT ER</u>	Memory protect error	An active low input generated by the MMU or BPU, or both and sampled by the BUS BUSY signal into the Fault Register (bit 0 CPU bus cycle, bit 1 if non-CPU bus cycle).
<u>MEM PAR ER</u>	Memory parity error	An active low input sampled by the BUS BUSY signal into bit 2 of the fault register.
<u>EXT ADR ER</u>	External address error	An active low input sampled by the BUS BUSY signal into the fault register (bit 5 or 8), depending on the cycle (memory or I/O).
SYSFLT ₀ SYSFLT ₁	System fault 0, System fault 1,	Asynchronous, positive edge-sensitive inputs that sets bit 7 (SYSFLT ₀) or bits 13 and 15 (SYSFLT ₁) in the fault register.
UNRCV ER	Unrecoverable error	An active high output that indicates the occurrence of an error classified as unrecoverable.
MAJ ER	Major error	An active high output that indicates the occurrence of an error classified as major.
D/ <u>I</u>	Data or instruction	An output signal that indicates whether the current bus cycle access is for Data (high) or Instruction (low). It is three-state during bus cycles not assigned to this CPU. This line can be used as an additional memory address bit for systems that require separate data and program memory.
<u>BUS REQ</u>	Bus request	An active low output that indicates the CPU requires the bus. It becomes inactive when the CPU has acquired the bus and started the bus cycle.

STANDARDIZED
MILITARY DRAWING
DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

SIZE
A

5962-87665

REVISION LEVEL
B

SHEET
30

DESC FORM 193A
JUL 91

74E ■ 9004708 0000125 862 ■

<u>Mnemonic</u>	<u>Name</u>	<u>Description</u>
<u>BUS GNT</u>	Bus grant	An active low input from an external arbiter that indicates the CPU currently has the highest priority bus request. If the bus is not used and not locked, the CPU may begin a bus cycle, commencing with the next CPU clock. A high level will hold the CPU in Hi-Z state (Bz), three-stating the IB bus status lines (D/I, R/W, M/I/O), strobes (STRBA, STRBD), and all the other lines that go three-state when this CPU does not have the bus.
<u>BUS BUSY</u>	Bus busy	An active low, bidirectional signal used to establish the beginning and end of a bus cycle. The trailing edge (low-to-high transition) is used for sampling bits into the fault register. It is three-state in bus cycles <u>not</u> assigned to this CPU. However, the CPU monitors the <u>BUS BUSY</u> line for latching non-CPU bus cycle faults into the fault register.
<u>BUS LOCK</u>	Bus lock	An active low, bidirectional signal used to lock the bus for successive bus cycles. During <u>nonlocked</u> bus cycles, the <u>BUS LOCK</u> signal mimics the <u>BUS BUSY</u> signal. It is three-state during bus cycles not assigned to this CPU. The following instructions will lock the bus: INCM, DECM, SB, RB, TSB, SRM, STUB and STLB.
DMA EN	Direct memory Access enable	An active high output that indicates the DMA is enabled. It is disabled when the CPU is initialized (reset) and can be enabled or disabled under program control (I/O commands DMAE, DMAD).
NML PWRUP	Normal power up	An active high output that is set when the CPU has successfully completed the built-in self test in the initialization sequence. It can be reset by the I/O command RNS.
SNEW	Start new	An active high output that indicates a new instruction is about to start executing in the next cycle.
<u>TRIGO RST</u>	Trigger-go reset	An active low discrete output. This signal can be pulsed low under program control I/O address 400B (Hex) and is automatically pulsed during processor initialization.
R/ <u>W</u>	Read or write	An output signal that indicates direction of data flow with respect to the current bus master. A high indicates a read or input operation and a low indicates a write or output operation. The signal is three-state during bus cycles not assigned to this CPU.
M/ <u>I</u> O	Memory or I/O	An output signal that indicates whether the current bus cycle is memory (high) or I/O (low). This signal is three-state during bus cycles not assigned to this CPU.
STRBA	Address strobe	An active high output that can be used to externally latch the memory or I/O address at the high-to-low transition of the strobe. The signal is three-state during bus cycles not assigned to this CPU.

STANDARDIZED
MILITARY DRAWING
DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

SIZE
A

5962-87665

REVISION LEVEL
B

SHEET

31

DESC FORM 193A
JUL 91

74E ■ 9004708 0000126 7T9 ■

<u>Mnemonic</u>	<u>Name</u>	<u>Description</u>
RDYA	Address ready	An active high input that can be used to extend the address phase of a bus cycle. When RDYA is not active, wait states are inserted by the device to accommodate slower memory or I/O devices.
STRBD	Data strobe	An active low output that can be used to strobe data in memory and XIO cycles. This signal is three-state during bus cycles not assigned to this CPU.
RDYD	Data ready	An active high input that extends the data phase of a bus cycle. When RDYD is not active, wait states are inserted by the device to accommodate slower memory or I/O devices.
IB ₀ -IB ₁₅	Information bus	A bidirectional time-multiplexed address/data bus that is three-state during bus cycles not assigned to this CPU. IB ₀ is the most significant bit.
AK ₀ -AK ₃	Access key	Outputs used to match the access lock in the MMU for memory accesses (a mismatch will cause the MMU to pull the MEM PRT ER signal low), and also indicates processor state (PS). Privileged instructions can be executed with PS = 0 only. These signals are three-state during bus cycles not assigned to this CPU.
AS ₀ -AS ₃	Address state	Outputs that select the page register group in the MMU. It is three-state during bus cycles not assigned to this CPU. These outputs together with D/I can be used to expand the device direct addressing space to 4 MBytes, in a nonprotected mode (no MMU). However, using this addressing mode may produce situations not specified in MIL-STD-1750.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-87665
		REVISION LEVEL B	SHEET 32

DESC FORM 193A
JUL 91

74E ■ 9004708 0000127 635 ■

6.6.1 Instruction clock cycles - Device types 01, 02, 03, and 04.

Instruction clock cycles - effect of wait states 1/

MIL-STD-1750 implemented instruction	Mnemonic	Address mode	Number of clock cycles								Notes
			WO = Wait states instr. fetch								
			0	1	2	1	2	1	2		
			WA = Wait states data R/W								
			0	0	0	1	1	2	2		
Integer arithmetic and logic											
Single precision add	A	R	4	5	6	5	6	5	6		
	A	B	11	12	13	13	14	14	15		
	A	BX	11	12	13	13	14	14	15		
	A	ISP	7	8	9	8	9	8	9		
	A	D	12	14	16	15	17	16	18		
	A	DX	12	14	16	15	17	16	18		
	A	IM	8	10	12	10	12	10	12		
Double precision add	DA	R	9	9	9	9	9	9	9		
	DA	D	21	22	23	24	25	26	27		
	DA	DX	21	22	23	24	25	26	27		
Single precision subtract	S	R	4	5	6	5	6	5	6		
	S	B	11	12	13	13	14	14	15		
	S	BX	11	12	13	13	14	14	15		
	S	ISP	7	8	9	8	9	8	9		
	S	D	12	14	16	15	17	16	18		
	S	DX	12	14	16	15	17	16	18		
	S	IM	8	10	12	10	12	10	12		
Double precision subtract	DS	R	9	9	9	9	9	9	9		
	DS	D	21	22	23	24	25	26	27		
	DS	DX	21	22	23	24	25	26	27		
Single precision multiply 16-bit product	MS	R	23	23	23	23	23	23	23		
	MS	ISP	26	26	26	26	26	26	26		
	MS	ISN	26	26	26	26	26	26	26		
	MS	D	31	32	33	33	34	34	35		
	MS	DX	31	32	33	33	34	34	35		
	MS	IM	27	28	29	28	29	28	29		
Single precision multiply 32-bit product	M	R	26	26	26	26	26	26	26		
	M	B	33	33	33	34	34	35	35		
	M	BX	33	33	33	34	34	35	35		
	M	D	34	35	36	36	37	37	38		
	M	DX	34	35	36	36	37	37	38		
	M	IM	30	31	32	31	32	31	32		
Double precision multiply	DM	R	69	69	69	69	69	69	69		
	DM	D	81	82	83	84	85	86	87		
	DM	DX	81	82	83	84	85	86	87		

See footnotes at end of list.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-87665
		REVISION LEVEL B	SHEET 33

DESC FORM 193A
JUL 91

74E ■ 9004708 0000128 571 ■

MIL-STD-1750 Implemented Instruction	Mnemonic	Address Mode	Number of clock cycles								Notes
			WD = Wait states instr. fetch								
			0	1	2	1	2	1	2		
			WA = Wait states data R/W								
			0	0	0	1	1	2	2		
Single precision divide 16-bit dividend	DV	R	58	58	58	58	58	58	58		
	DV	ISP	61	61	61	61	61	61	61		
	DV	ISN	61	61	61	61	61	61	61		
	DV	D	66	67	68	68	69	69	70		
	DV	DX	66	67	68	68	69	69	70		
	DV	IM	62	63	64	63	64	63	64		
Single precision divide 32-bit dividend	D	R	73	73	73	73	73	73	73		
	D	B	80	80	80	81	81	82	82		
	D	BX	80	80	80	81	81	82	82		
	D	D	81	82	83	83	84	84	85		
	D	DX	81	82	83	83	84	84	85		
	D	IM	77	78	79	78	79	78	79		
Double precision divide	DD	R	133	133	133	133	133	133	133		
	DD	D	145	146	147	148	149	150	151		
	DD	DX	145	146	147	148	149	150	151		
Increment memory by positive integer	INCM	D	15	16	17	18	19	20	21		
	INCM	DX	15	16	17	18	19	20	21		
Decrement memory by positive integer	DECM	D	16	18	20	20	22	22	24		
	DECM	DX	16	18	20	20	22	22	24		
Single precision absolute value	ABS	R	6	6	6	6	6	6	6	Pos. Number	
	ABS	R	9	9	9	9	9	9	9	Neg. Number	
Double precision absolute value	DABS	R	9	9	9	9	9	9	9	Pos. Number	
	DABS	R	12	12	12	12	12	12	12	Neg. Number	
Single precision negate	NEG	R	4	5	6	5	6	5	6		
Double precision negate	DNEG	R	9	9	9	9	9	9	9		
Single precision compare	C	R	4	5	6	5	6	5	6		
	C	B	11	12	13	13	14	14	15		
	C	BX	11	12	13	13	14	14	15		
	C	ISP	7	8	9	8	9	8	9		
	C	ISN	7	8	9	8	9	8	9		
	C	D	12	14	16	15	17	16	18		
	C	DX	12	14	16	15	17	16	18		
	C	IM	8	10	12	10	12	10	12		

See footnotes at end of list.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-87665
		REVISION LEVEL B	SHEET 34

DESC FORM 193A
JUL 91

74E ■ 9004708 0000129 408 ■

MIL-STD-1750 Implemented instruction	Mnemonic	Address mode	Number of clock cycles								Notes
			WD = Wait states instr. fetch 0 1 2 1 2 1 2								
			WA = Wait states data R/W 0 0 0 1 1 2 2								
Compare between limits	CBL	D	24	25	26	27	28	29	30		
	CBL	DX	24	25	26	27	28	29	30		
Double precision compare	DC	R	6	6	6	6	6	6	6		
	DC	D	18	19	20	21	22	23	24		
	DC	DX	18	19	20	21	22	23	24		
Logical inclusive-OR	OR	R	4	5	6	5	6	5	6		
	OR	B	11	12	13	13	14	14	15		
	OR	BX	11	12	13	13	14	14	15		
	OR	D	12	14	16	15	17	16	18		
	OR	DX	12	14	16	15	17	16	18		
	OR	IM	8	10	12	10	12	10	12		
Logical exclusive-OR	XOR	R	4	5	6	5	6	5	6		
	XOR	D	12	14	16	15	17	16	18		
	XOR	DX	12	14	16	15	17	16	18		
	XOR	IM	8	10	12	10	12	10	12		
Logical AND	AND	R	4	5	6	5	6	5	6		
	AND	B	11	12	13	13	14	14	15		
	AND	BX	11	12	13	13	14	14	15		
	AND	D	12	14	16	15	17	16	18		
	AND	DX	12	14	16	15	17	16	18		
	AND	IM	8	10	12	10	12	10	12		
Logical NAND	NAND	R	4	5	6	5	6	5	6		
	NAND	D	12	14	16	15	17	16	18		
	NAND	DX	12	14	16	15	17	16	18		
	NAND	IM	8	10	12	10	12	10	12		
Floating point arithmetic											
Floating point add	FA	R	28	28	28	28	28	28	28		
	FA	B	39	39	39	41	41	43	43		
	FA	BX	39	39	39	41	41	43	43		
	FA	D	40	41	42	43	44	45	46		
	FA	DX	40	41	42	43	44	45	46		
Floating point add extended precision	EFA	R	50	50	50	50	50	50	50		
	EFA	D	66	67	68	70	71	73	74		
	EFA	DX	66	67	68	70	71	73	74		

See footnotes at end of list.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-87665
		REVISION LEVEL B	SHEET 35

DESC FORM 193A
JUL 91

74E ■ 9004708 0000130 12T ■

MIL-STD-1750 implemented instruction	Mnemonic	Address mode	Number of clock cycles								Notes
			WO = Wait states instr. fetch								
			0	1	2	1	2	1	2		
			WA = Wait states data R/W								
			0	0	0	1	1	2	2		
Floating point subtract	FS	R	28	28	28	28	28	28	28		
	FS	B	39	39	39	41	41	43	43		
	FS	BX	39	39	39	41	41	43	43		
	FS	D	40	41	42	43	44	45	46		
	FS	DX	40	41	42	43	44	45	46		
Floating point subtract extended precision	EFS	R	50	50	50	50	50	50	50		
	EFS	D	66	67	68	70	71	73	74		
	EFS	DX	66	67	68	70	71	73	74		
Floating point multiply	FM	R	43	43	43	43	43	43	43		
	FM	B	54	54	54	56	56	58	58		
	FM	BX	54	54	54	56	56	58	58		
	FM	D	55	56	57	58	59	60	61		
	FM	DX	55	56	57	58	59	60	61		
Floating point multiply extended precision	EFM	R	99	99	99	99	99	99	99		
	EFM	D	112	113	114	116	117	119	120		
	EFM	DX	112	113	114	116	117	119	120		
Floating point divide	FD	R	89	89	89	89	89	89	89		
	FD	B	94	94	94	96	96	98	98		
	FD	BX	94	94	94	96	96	98	98		
	FD	D	95	96	97	98	99	100	101		
	FD	DX	95	96	97	98	99	100	101		
Floating point divide extended precision	EFD	R	183	183	183	183	183	183	183		
	EFD	D	190	191	192	194	195	197	198		
	EFD	DX	190	191	192	194	195	197	198		
Floating point compare	FC	R	6	6	6	6	6	6	6		
	FC	B	17	17	17	19	19	21	21		
	FC	BX	17	17	17	19	19	21	21		
	FC	D	18	19	20	21	22	23	24		
	FC	DX	18	19	20	21	22	23	24		
Floating point compare extended precision	EFC	R	17	17	17	17	17	17	17		
	EFC	D	33	34	35	37	38	40	41		
	EFC	DX	33	34	35	37	38	40	41		
Floating point absolute value	FABS	R	9	9	9	9	9	9	9	Pos. number	
	FABS	R	21	21	21	21	21	21	21	Neg. number	
Floating point negate	FNEG	R	18	18	18	18	18	18	18		

See footnotes at end of list.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-87665
		REVISION LEVEL B	SHEET 36

DESC FORM 193A
JUL 91

74E ■ 9004708 0000131 066 ■

MIL-STD-1750 implemented instruction	Mnemonic	Address mode	Number of clock cycles								Notes
			WD = Wait states instr. fetch								
			0	1	2	1	2	1	2		
			WA = Wait states data R/W								
			0	0	0	1	1	2	2		
Convert floating point to 16-bit integer	FIX	R	22	23	24	23	24	23	24		
Convert 16-bit integer to floating point	FLT	R	16	17	18	17	18	17	18		
Convert floating point extended precision to 32-bit integer	EFIX	R	43	44	45	44	45	44	45		
Convert 32-bit integer to extended precision floating point	EFLT	R	25	26	27	26	27	26	27		
Bit operations											
Set bit	SB	R	4	5	6	5	6	5	6		
	SB	D	12	14	16	15	17	16	18		
	SB	DX	12	14	16	15	17	16	18		
	SB	I	16	18	20	20	22	22	24		
	SB	IX	16	18	20	20	22	22	24		
Reset bit	RB	R	4	5	6	5	6	5	6		
	RB	D	12	14	16	15	17	16	18		
	RB	DX	12	14	16	15	17	16	18		
	RB	I	16	18	20	20	22	22	24		
	RB	IX	16	18	20	20	22	22	24		
Test bit	TB	R	6	6	6	6	6	6	6		
	TB	D	14	15	16	16	17	17	18		
	TB	DX	14	15	16	16	17	17	18		
	TB	I	18	19	20	21	22	23	24		
	TB	IX	18	19	20	21	22	23	24		
Test and set bit	TSB	D	19	20	21	21	22	22	23		
	TSB	DX	19	20	21	21	22	22	23		
Set variable bit reset variable bit test variable bit	SVBR	R	4	5	6	5	6	5	6		
	RVBR	R	4	5	6	5	6	5	6		
	TVBR	R	6	6	6	6	6	6	6		

See footnotes at end of list.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-87665
		REVISION LEVEL B	SHEET 37

DESC FORM 193A
JUL 91

74E ■ 9004708 0000132 TT2 ■

MIL-STD-1750 implemented instruction	Mnemonic	Address mode	Number of clock cycles								Notes				
			WO = Wait states instr. fetch												
			0	1	2	1	2	1	2						
			WA = Wait states data R/W												
								0	0	0	1	1	2	2	
Shift operations															
Shift left logical	SLL	R	9	9	9	9	9	9	9	9	9	9	9	One shift	
	SLL	R	1	1	1	1	1	1	1	1	1	1	1	Incremental	
Shift right logical	SRL	R	9	9	9	9	9	9	9	9	9	9	9	One shift	
	SRL	R	1	1	1	1	1	1	1	1	1	1	1	Incremental	
Shift right Arithmetic	SRA	R	9	9	9	9	9	9	9	9	9	9	9	One shift	
	SRA	R	1	1	1	1	1	1	1	1	1	1	1	Incremental	
Shift left cyclic	SLC	R	9	9	9	9	9	9	9	9	9	9	9	One shift	
	SLC	R	1	1	1	1	1	1	1	1	1	1	1	Incremental	
Double shift left Logical	DSLL	R	15	15	15	15	15	15	15	15	15	15	15	One shift	
	DSLL	R	1	1	1	1	1	1	1	1	1	1	1	Incremental	
Double shift right Logical	DSRL	R	15	15	15	15	15	15	15	15	15	15	15	One shift	
	DSRL	R	1	1	1	1	1	1	1	1	1	1	1	Incremental	
Double shift right Arithmetic	DSRA	R	15	15	15	15	15	15	15	15	15	15	15	One shift	
	DSRA	R	1	1	1	1	1	1	1	1	1	1	1	Incremental	
Double shift left Cyclic	DSLCL	R	15	15	15	15	15	15	15	15	15	15	15	One shift	
	DSLCL	R	1	1	1	1	1	1	1	1	1	1	1	Incremental	
Shift logical count in register	SLR	R	12	12	12	12	12	12	12	12	12	12	12	No shift	
			15	15	15	15	15	15	15	15	15	15	15	Right	
	SLR	R	1	1	1	1	1	1	1	1	1	1	1	Incremental	
			18	18	18	18	18	18	18	18	18	18	18	Left	
			1	1	1	1	1	1	1	1	1	1	Incremental		
Shift arithmetic count in register	SAR	R	12	12	12	12	12	12	12	12	12	12	12	No shift	
			15	15	15	15	15	15	15	15	15	15	15	Right	
	SAR	R	1	1	1	1	1	1	1	1	1	1	1	Incremental	
			18	18	18	18	18	18	18	18	18	18	18	Left	
			1	1	1	1	1	1	1	1	1	1	Incremental		
Shift cyclic count in register	SCR	R	12	12	12	12	12	12	12	12	12	12	12	No shift	
			12	12	12	12	12	12	12	12	12	12	12	Right	
	SCR	R	1	1	1	1	1	1	1	1	1	1	1	Incremental	
			18	18	18	18	18	18	18	18	18	18	18	Left	
			1	1	1	1	1	1	1	1	1	1	Incremental		
Double shift logical count in register	DSLRL	R	12	12	12	12	12	12	12	12	12	12	12	No shift	
			21	21	21	21	21	21	21	21	21	21	21	Right	
	DSLRL	R	1	1	1	1	1	1	1	1	1	1	1	Incremental	
			24	24	24	24	24	24	24	24	24	24	24	Left	
			1	1	1	1	1	1	1	1	1	1	Incremental		

See footnotes at end of list.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-87665
		REVISION LEVEL B	SHEET 38

DESC FORM 193A
JUL 91

74E ■ 9004708 0000133 939 ■

MIL-STD-1750 implemented instruction	Mnemonic	Address mode	Number of clock cycles								Notes
			W0 = Wait states instr. fetch								
			0	1	2	1	2	1	2		
			WA = Wait states data R/W								
			0	0	0	1	1	2	2		
Double shift arithmetic count in register	DSAR	R	12	12	12	12	12	12	12	No shift Right Incremental Left Incremental	
			21	21	21	21	21	21	21		
	DSAR	R	1	1	1	1	1	1	1		
			24	24	24	24	24	24	24		
			1	1	1	1	1	1	1		
Double shift cyclic count in register	DSCR	R	12	12	12	12	12	12	12	No shift Right Incremental Left Incremental	
			21	21	21	21	21	21	21		
	DSCR	R	1	1	1	1	1	1	1		
			24	24	24	24	24	24	24		
			1	1	1	1	1	1	1		
Load/store/exchange											
Load single precision	L	R	4	5	6	5	6	5	6		
	L	B	11	12	13	13	14	14	15		
	L	BX	11	12	13	13	14	14	15		
	L	ISP	4	5	6	5	6	5	6		
	L	ISN	4	5	6	5	6	5	6		
	L	D	12	14	16	15	17	16	18		
	L	DX	12	14	16	15	17	16	18		
	L	IM	8	10	12	10	12	10	12		
	L	IMX	8	10	12	10	12	10	12		
	L	I	16	18	20	20	22	22	24		
L	IX	16	18	20	20	22	22	24			
Load double precision	DL	R	9	9	9	9	9	9	9		
	DL	B	15	15	15	17	17	19	19		
	DL	BX	15	15	15	17	17	19	19		
	DL	D	16	17	18	19	20	21	22		
	DL	DX	16	17	18	19	20	21	22		
	DL	I	25	26	27	29	30	32	33		
	DL	IX	25	26	27	29	30	32	33		
Load floating point extended precision	EFL	D	29	31	33	34	36	37	39		
	EFL	DX	29	31	33	34	36	37	39		
Load from upper byte	LUB	D	14	15	16	16	17	17	18		
	LUB	DX	14	15	16	16	17	17	18		
	LUB	I	18	19	20	21	22	23	24		
	LUB	IX	18	19	20	21	22	23	24		
Load from lower byte	LLB	D	12	14	16	15	17	16	18		
	LLB	DX	12	14	16	15	17	16	18		
	LLB	I	16	18	20	20	22	22	24		
	LLB	IX	16	18	20	20	22	22	24		

See footnotes at end of list.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-87665
		REVISION LEVEL B	SHEET 39

DESC FORM 193A
JUL 91

74E ■ 9004708 0000134 875 ■

MIL-STD-1750 implemented instruction	Mnemonic	Address mode	Number of clock cycles								Notes
			WO = Wait states instr. fetch								
			0 1 2 1 2 1 2								
			WA = Wait states data R/W								
0 0 0 1 1 2 2											
Store single precision	ST	B	11	12	13	13	14	14	15		
	ST	BX	11	12	13	13	14	14	15		
	ST	D	12	14	16	15	17	16	18		
	ST	DX	12	14	16	15	17	16	18		
	ST	I	16	18	20	20	22	22	24		
	ST	IX	16	18	20	20	22	22	24		
Store a positive constant	STC	D	12	14	16	15	17	16	18		
	STC	DX	12	14	16	15	17	16	18		
	STC	I	16	18	20	20	22	22	24		
	STC	IX	16	18	20	20	22	22	24		
Store double precision	DST	B	15	16	17	18	19	20	21		
	DST	BX	15	16	17	18	19	20	21		
	DST	D	16	18	20	20	22	22	24		
	DST	DX	16	18	20	20	22	22	24		
	DST	I	20	22	24	25	27	28	30		
	DST	IX	20	22	24	25	27	28	30		
Store register through mask	SRM	D	21	23	25	24	26	25	27	Bus lock	
	SRM	DX	21	23	25	24	26	25	27	Bus lock	
Store floating point extended precision	EFST	D	20	22	24	25	27	28	30		
	EFST	DX	20	22	24	25	27	28	30		
Store into upper byte	STUB	D	16	18	20	20	22	22	24	Bus lock	
	STUB	DX	16	18	20	20	22	22	24	Bus lock	
	STUB	I	20	22	24	25	26	28	30	Bus lock	
	STUB	IX	20	22	24	25	26	28	30	Bus lock	
Store into lower byte	STLB	D	16	18	20	20	22	22	24	Bus lock	
	STLB	DX	16	18	20	20	22	22	24	Bus lock	
	STLB	I	20	22	24	25	27	28	30	Bus lock	
	STLB	IX	20	22	24	25	27	28	30	Bus lock	
Exchange bytes in register words in register	XBR	R	6	6	6	6	6	6	6		
	XWR	R	6	6	6	6	6	6	6		
Multiple load/store											
Push multiple registers onto the stack	PSHM	R	18	18	18	21	21	24	24	One push	
	PSHM	R	10	10	10	11	11	12	12	Incremental	

See footnotes at end of list.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-87665
		REVISION LEVEL B	SHEET 40

DESC FORM 193A
JUL 91

74E ■ 9004708 0000135 701 ■

MIL-STD-1750 implemented instruction	Mnemonic	Address mode	Number of clock cycles								Notes
			WO = Wait states instr. fetch 0 1 2 1 2 1 2								
			WA = Wait states data R/W 0 0 0 1 1 2 2								
Pop multiple registers off the stack	POPM	R	23	24	25	25	26	26	27	One pop Incremental	
	POPM	R	13	13	13	14	14	15	15		
Load multiple registers	LM	D	16	18	20	20	22	22	24	One load Incremental One load Incremental	
	LM	D	4	4	4	5	5	6	6		
	LM	DX	16	18	20	20	22	22	24		
	LM	DX	4	4	4	5	5	6	6		
Store multiple registers	STM	D	15	17	19	18	20	19	21	One load Incremental One load Incremental	
	STM	D	4	4	4	5	5	6	6		
	STM	DX	15	17	19	18	20	19	21		
	STM	DX	4	4	4	5	5	6	6		
Move multiple words memory-to-memory	MOV	D	10	11	12	11	12	11	12	No move One move Incremental	
	MOV	D	36	37	38	39	40	41	42		
	MOV	D	8	8	8	10	10	12	12		
Program control											
Jump on condition	JC	D	8	10	12	10	12	10	12	No jump Jump No jump Jump No jump Jump No jump Jump	
	JC	D	16	18	20	18	20	18	20		
	JC	DX	8	10	12	10	12	10	12		
	JC	DX	16	18	20	18	20	18	20		
	JC	I	12	14	16	15	17	16	18		
	JC	I	20	22	24	25	27	28	30		
	JC	IX	12	14	16	15	17	16	18		
	JC	IX	20	22	24	25	27	28	30		
Jump to subroutine	JS	D	12	15	18	15	18	15	18		
	JS	DX	12	15	18	15	18	15	18		
Subtract one and jump	SOJ	D	15	17	19	17	19	17	19	No jump Jump No jump Jump	
	SOJ	D	15	19	23	19	23	19	23		
	SOJ	DX	15	17	19	17	19	17	19		
	SOJ	DX	15	19	23	19	23	19	23		
Branch unconditionally	BR	ICR	12	15	18	15	18	15	18		
Branch if equal to zero	BEZ	ICR	4	5	6	5	6	5	6	No branch Branch	
	BEZ	ICR	12	15	18	15	18	15	18		
Branch if less than zero	BLT	ICR	4	5	6	5	6	5	6	No branch Branch	
	BLT	ICR	12	15	18	15	18	15	18		

See footnotes at end of list.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-87665
		REVISION LEVEL B	SHEET 41

DESC FORM 193A
JUL 91

74E ■ 9004708 0000136 648 ■

MIL-STD-1750 implemented instruction	Mnemonic	Address mode	Number of clock cycles								Notes
			WO = Wait states instr. fetch								
			0	1	2	1	2	1	2		
			WA = Wait states data R/W								
			0	0	0	1	1	2	2		
Branch if less than or equal to zero	BLE	ICR	4	5	6	5	6	5	6	No branch Branch	
	BLE	ICR	12	15	18	15	18	15	18		
Branch if greater than zero	BGT	ICR	4	5	6	5	6	5	6	No branch Branch	
	BGT	ICR	12	15	18	15	18	15	18		
Branch if not equal to zero	BNZ	ICR	4	5	6	5	6	5	6	No branch Branch	
	BNZ	ICR	12	15	18	15	18	15	18		
Branch if greater than or equal to zero	BGE	ICR	4	5	6	5	6	5	6	No branch Branch	
	BGE	ICR	12	15	18	15	18	15	18		
Branch to executive	BEX	S	101	103	105	112	113	121	123	No MMU With MMU	
	BEX	S	98	100	102	109	111	118	120		
Load status	LST	D	38	38	38	38	38	38	38	No MMU With MMU No MMU With MMU No MMU With MMU No MMU With MMU	
	LST	D	41	41	41	41	41	41	41		
	LST	DX	38	38	38	38	38	38	38		
	LST	DX	41	41	41	41	41	41	41		
	LST	I	44	44	44	44	44	44	44		
	LST	I	47	47	47	47	47	47	47		
	LST	IX	44	44	44	44	44	44	44		
	LST	IX	47	47	47	47	47	47	47		
Stack IC and jump to subroutine	SJS	D	19	19	19	19	19	19	19		
	SJS	DX	19	19	19	19	19	19	19		
Unstack IC and return from subroutine	URS	S	15	15	15	15	15	15	15		
No operation	NOP	S	4	4	4	4	4	4	4		
Break point	BPT	S	20	20	20	20	20	20	20	No console I/O	
Built-in function to implement external co-processor	BIF	D	35	35	35	35	35	35	35		
	BIF	DX	35	35	35	35	35	35	35		
	BIF	I	39	39	39	39	39	39	39		
	BIF	IX	39	39	39	39	39	39	39		

See footnotes at end of list.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-87665
		REVISION LEVEL B	SHEET 42

DESC FORM 193A
JUL 91

74E ■ 9004708 0000137 584 ■

MIL-STD-1750 implemented instruction	Mnemonic	Address mode	Number of clock cycles						Notes	
			WO = Wait states instr. fetch							
			0	1	2	1	2	1		2
			WA = Wait states data R/W							
			0	0	0	1	1	2	2	
Execute input/output	XIO	IM	45							Input
	XIO	IMX	45							Input
	XIO	IM	33							Output
	XIO	IMX	33							Output
Vectored input/output <u>2/ 3/ 4/</u>	VIO	D	93							Overhead-in
	VIO	D	62							Incremental
	VIO	D	12							Incremental-unused
	VIO	DX	93							Overhead-in
	VIO	DX	62							Incremental
	VIO	DX	12							Incremental-unused
	VIO	D	84							Overhead-out
	VIO	D	53							Incremental
	VIO	D	12							Incremental-unused
	VIO	DX	84							Overhead-out
	VIO	DX	53							Incremental
	VIO	DX	12							Incremental-unused

- 1/ The number of clock cycles required by the CPU is listed as a function of the number of wait states. Both instruction fetch and data read/write wait states of 0, 1, and 2 clock cycles are shown in this list.
- 2/ Overhead-in is the input VIO instruction overhead including one XIO.
- 3/ Incremental is the number of cycles for each additional XIO.
- 4/ Incremental unused is the number of cycles for each unused bit(0) in the vector register.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-87665
		REVISION LEVEL B	SHEET 43

DESC FORM 193A
JUL 91

74E ■ 9004708 0000138 410 ■

6.6.2 Instruction clock cycles - Device types 05, 06, and 07.

Instruction clock cycles - effect of wait states 1/

MIL-STD-1750 implemented instruction	Mnemonic	Address mode	Number of clock cycles								Notes
			WO = Wait states instr. fetch								
			0	1	2	1	2	1	2		
			WA = Wait states data R/W								
			0	0	0	1	1	2	2		
Integer arithmetic and logic											
Single precision add	A A A A A A	R B BX ISP D DX IM	4 10 10 6 12 12 8	5 11 11 7 14 14 10	6 12 12 8 16 16 12	5 12 12 7 15 15 10	6 13 13 8 17 17 12	5 13 13 7 16 16 10	6 14 14 8 18 18 12		
Double precision add	DA DA DA	R D DX	6 16 18	6 18 19	6 20 20	6 20 21	6 22 22	6 22 23	6 24 24		
Single precision subtract	S S S S S S S	R B BX ISP D DX IM	4 10 10 6 12 12 8	5 11 11 7 14 14 10	6 12 12 8 16 16 12	5 12 12 7 15 15 10	6 13 13 8 17 17 12	5 13 13 7 16 16 10	6 14 14 8 18 18 12		
Double precision subtract	DS DS DS	R D DX	6 16 18	6 18 19	6 20 20	6 20 21	6 22 22	6 22 23	6 24 24		
Single precision multiply 16-bit product	MS MS MS MS MS MS	R ISP ISN D DX IM	4 6 6 12 12 8	5 7 7 14 14 10	6 8 8 16 16 12	5 7 7 15 15 10	6 8 8 17 17 12	5 7 7 16 16 10	5 13 13 17 17 11		
Single precision multiply 32-bit product	M M M M M M	R B BX D DX IM	5 11 11 13 13 9	5 11 11 14 14 10	5 11 11 15 15 11	5 12 12 15 15 10	5 12 12 16 16 11	5 13 13 16 16 10	5 13 13 17 17 11		
Double precision multiply	DM DM DM	R D DX	9 17 19	9 19 21	9 21 21	9 21 23	9 23 23	9 23 25	9 25 27		

See footnotes at end of list.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-87665
		REVISION LEVEL B	SHEET 44

DESC FORM 193A
JUL 91

74E ■ 9004708 0000139 357 ■

MIL-STD-1750 implemented instruction	Mnemonic	Address mode	Number of clock cycles								Notes
			WD = Wait states instr. fetch								
			0	1	2	1	2	1	2		
			WA = Wait states data R/W								
			0	0	0	1	1	2	2		
Single precision divide 16-bit dividend	DV	R	48	48	48	48	48	48	48		
	DV	ISP	50	50	50	50	50	50	50		
	DV	ISN	50	50	50	50	50	50	50		
	DV	D	52	52	52	53	53	54	54		
	DV	DX	54	54	54	55	55	56	56		
	DV	IM	52	53	54	53	54	53	54		
Single precision divide 32-bit dividend	D	R	58	58	58	58	58	58	58		
	D	B	64	65	66	65	66	65	66		
	D	BX	64	65	66	65	66	65	66		
	D	D	62	62	62	63	63	64	64		
	D	DX	64	64	64	65	65	66	66		
	D	IM	62	63	64	63	64	63	64		
Double precision divide	DD	R	88	88	88	88	88	88	88		
	DD	D	96	96	96	98	98	100	100		
	DD	DX	98	98	98	100	100	102	102		
Increment memory by positive integer	INCM	D	16	18	20	20	22	22	24		
	INCM	DX	16	18	20	20	22	22	24		
Decrement memory by positive integer	DECM	D	16	18	20	20	22	22	24		
	DECM	DX	16	18	20	20	22	22	24		
Single precision absolute value	ABS	R	4	5	6	5	6	5	6	Pos. number	
	ABS	R	6	6	6	6	6	6	6	Neg. number	
Double precision absolute value	DABS	R	6	6	6	6	6	6	6	Pos. number	
	DABS	R	8	8	8	8	8	8	8	Neg. Number	
Single precision negate	NEG	R	4	5	6	5	6	5	6		
Double precision negate	DNEG	R	6	6	6	6	6	6	6		
Single precision compare	C	R	4	5	6	5	6	5	6		
	C	B	10	11	12	12	13	13	14		
	C	BX	10	11	12	12	13	13	14		
	C	ISP	6	7	8	7	8	7	8		
	C	ISN	6	7	8	7	8	7	8		
	C	D	12	14	16	15	17	16	18		
	C	DX	12	14	16	15	17	16	18		
	C	IM	8	10	12	10	12	10	12		

See footnotes at end of list.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-87665
		REVISION LEVEL B	SHEET 45

DESC FORM 193A
JUL 91

74E ■ 9004708 0000140 079 ■

MIL-STD-1750 implemented instruction	Mnemonic	Address mode	Number of clock cycles								Notes
			W0 = Wait states instr. fetch 0 1 2 1 2 1 2								
			WA = Wait states data R/W 0 0 0 1 1 2 2								
Compare between limits	CBL	D	20	21	22	23	24	25	26		
	CBL	DX	20	21	22	23	24	25	26		
Double precision compare	DC	R	4	5	6	5	6	5	6		
	DC	D	16	18	20	20	22	22	24		
	DC	DX	16	18	20	20	22	22	24		
Logical inclusive-OR	OR	R	4	5	6	5	6	5	6		
	OR	B	10	11	12	12	13	13	14		
	OR	BX	10	11	12	12	13	13	14		
	OR	D	12	14	16	15	17	16	18		
	OR	DX	12	14	16	15	17	16	18		
	OR	IM	8	10	12	10	12	10	12		
Logical exclusive-OR	XOR	R	4	5	6	5	6	5	6		
	XOR	D	12	14	16	15	17	16	18		
	XOR	DX	12	14	16	15	17	16	18		
	XOR	IM	8	10	12	10	12	10	12		
Logical AND	AND	R	4	5	6	5	6	5	6		
	AND	B	10	11	12	12	13	13	14		
	AND	BX	10	11	12	12	13	13	14		
	AND	D	12	14	16	15	17	16	18		
	AND	DX	12	14	16	15	17	16	18		
	AND	IM	8	10	12	10	12	10	12		
Logical NAND	NAND	R	4	5	6	5	6	5	6		
	NAND	D	12	14	16	15	17	16	18		
	NAND	DX	12	14	16	15	17	16	18		
	NAND	IM	8	10	12	10	12	10	12		
Floating point arithmetic											
Floating point add	FA	R	18	18	18	18	18	18	18		
	FA	B	28	28	28	30	30	32	32		
	FA	BX	28	28	28	30	30	32	32		
	FA	D	26	26	26	28	28	30	30		
	FA	DX	28	28	28	30	30	32	32		
Floating point add extended precision	EFA	R	34	34	34	34	34	34	34		
	EFA	D	46	46	46	49	49	52	52		
	EFA	DX	48	48	48	51	51	54	54		

See footnotes at end of list.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-87665
		REVISION LEVEL B	SHEET 46

DESC FORM 193A
JUL 91

74E ■ 9004708 0000141 T05 ■

MIL-STD-1750 implemented instruction	Mnemonic	Address mode	Number of clock cycles								Notes
			WO = Wait states instr. fetch								
			0	1	2	1	2	1	2		
			WA = Wait states data R/W								
			0	0	0	1	1	2	2		
Floating point subtract	FS	R	18	18	18	18	18	18	18		
	FS	B	28	28	28	30	30	32	32		
	FS	BX	28	28	28	30	30	32	32		
	FS	D	26	26	26	28	28	30	30		
	FS	DX	28	28	28	30	30	32	32		
Floating point subtract extended precision	EFS	R	34	34	34	34	34	34	34		
	EFS	D	46	46	46	49	49	52	52		
	EFS	DX	48	48	48	51	51	54	54		
Floating point multiply	FM	R	9	9	9	9	9	9	9		
	FM	B	19	19	19	21	21	23	23		
	FM	BX	19	19	19	21	21	23	23		
	FM	D	17	19	21	21	23	23	25		
	FM	DX	19	21	23	23	25	25	27		
Floating point multiply extended precision	EFM	R	17	17	17	17	17	17	17		
	EFM	D	29	29	29	32	32	35	35		
	EFM	DX	31	31	31	34	34	37	37		
Floating point divide	FD	R	74	74	74	74	74	74	74		
	FD	B	84	84	84	86	86	88	88		
	FD	BX	84	84	84	86	86	88	88		
	FD	D	82	82	82	84	84	86	86		
	FD	DX	84	84	84	86	86	88	88		
Floating point divide extended precision	EFD	R	122	122	122	122	122	122	122		
	EFD	D	134	134	134	137	137	140	140		
	EFD	DX	136	136	136	139	139	142	142		
Floating point compare	FC	R	4	5	6	5	6	5	6		
	FC	B	14	15	16	17	18	19	20		
	FC	BX	14	15	16	17	18	19	20		
	FC	D	16	18	20	20	22	22	24		
	FC	DX	16	18	20	20	22	22	24		
Floating point compare extended precision	EFC	R	10	10	10	10	10	10	10		
	EFC	D	22	22	24	25	27	28	30		
	EFC	DX	24	24	26	27	29	30	32		
Floating point absolute value	FABS	R	6	6	6	6	6	6	6	Pos. number	
	FABS	R	14	14	14	14	14	14	14	Neg. number	
Floating point negate	FNEG	R	12	12	12	12	12	12	12		

See footnotes at end of list.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-87665
		REVISION LEVEL B	SHEET 47

DESC FORM 193A
JUL 91

74E ■ 9004708 0000142 941 ■

MIL-STD-1750 implemented instruction	Mnemonic	Address mode	Number of clock cycles	Notes
			WO = Wait states instr. fetch 0 1 2 1 2 1 2 WA = Wait states data R/W 0 0 0 1 1 2 2	
Convert floating point to 16-bit integer	FIX	R	14 14 14 14 14 14 14	
Convert 16-bit integer to floating point	FLT	R	10 10 10 10 10 10 10	
Convert floating point extended precision to 32-bit integer	EFIX	R	28 28 28 28 28 28 28	
Convert 32-bit integer to extended precision floating point	EFLT	R	16 16 16 16 16 16 16	
Bit operations				
Set bit	SB	R	4 5 6 5 6 5 6	
	SB	D	12 14 16 15 17 16 18	
	SB	DX	12 14 16 15 17 16 18	
	SB	I	16 18 20 20 22 22 24	
	SB	IX	16 18 20 20 22 22 24	
Reset bit	RB	R	4 5 6 5 6 5 6	
	RB	D	12 14 16 15 17 16 18	
	RB	DX	12 14 16 15 17 16 18	
	RB	I	16 18 20 20 22 22 24	
	RB	IX	16 18 20 20 22 22 24	
Test bit	TB	R	4 5 6 5 6 5 6	
	TB	D	12 14 16 15 17 16 18	
	TB	DX	12 14 16 15 17 16 18	
	TB	I	16 18 20 20 22 22 24	
	TB	IX	16 18 20 20 22 22 24	
Test and set bit	TSB	D	18 20 22 22 24 24 26	
	TSB	DX	18 20 22 22 24 24 26	
Set variable bit reset variable bit test variable bit	SVBR	R	4 5 6 5 6 5 6	
	RVBR	R	4 5 6 5 6 5 6	
	TVBR	R	4 5 6 5 6 5 6	

See footnotes at end of list.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-87665
		REVISION LEVEL B	SHEET 48

DESC FORM 193A
JUL 91

74E ■ 9004708 0000143 888 ■

MIL-STD-1750 implemented instruction	Mnemonic	Address mode	Number of clock cycles								Notes
			WO = Wait states instr. fetch								
			0 1 2 1 2 1 2								
			WA = Wait states data R/W								
0 0 0 1 1 2 2											
Shift operations											
Shift left logical	SLL	R	6	6	6	6	6	6	6	One shift	
	SLL	R	1	1	1	1	1	1	1	Incremental	
Shift right logical	SRL	R	6	6	6	6	6	6	6	One shift	
	SRL	R	1	1	1	1	1	1	1	Incremental	
Shift right	SRA	R	6	6	6	6	6	6	6	One shift	
Arithmetic	SRA	R	1	1	1	1	1	1	1	Incremental	
Shift left cyclic	SLC	R	6	6	6	6	6	6	6	One shift	
	SLC	R	1	1	1	1	1	1	1	Incremental	
Double shift left	DSL	R	10	10	10	10	10	10	10	One shift	
Logical	DSL	R	1	1	1	1	1	1	1	Incremental	
Double shift right	DSRL	R	10	10	10	10	10	10	10	One shift	
Logical	DSRL	R	1	1	1	1	1	1	1	Incremental	
Double shift right	DSRA	R	10	10	10	10	10	10	10	One shift	
Arithmetic	DSRA	R	1	1	1	1	1	1	1	Incremental	
Double shift left	DSL	R	10	10	10	10	10	10	10	One shift	
Cyclic	DSL	R	1	1	1	1	1	1	1	Incremental	
Shift logical	SLR	R	8	8	8	8	8	8	8	No shift	
Count in register			10	10	10	10	10	10	10	Right	
	SLR	R	1	1	1	1	1	1	1	Incremental	
			12	12	12	12	12	12	12	Left	
			1	1	1	1	1	1	1	Incremental	
Shift arithmetic	SAR	R	8	8	8	8	8	8	8	No shift	
count in register			10	10	10	10	10	10	10	Right	
	SAR	R	1	1	1	1	1	1	1	Incremental	
			12	12	12	12	12	12	12	Left	
			1	1	1	1	1	1	1	Incremental	
Shift cyclic	SCR	R	8	8	8	8	8	8	8	No shift	
count in register			8	8	8	8	8	8	8	Right	
	SCR	R	1	1	1	1	1	1	1	Incremental	
			12	12	12	12	12	12	12	Left	
			1	1	1	1	1	1	1	Incremental	
Double shift	DSL	R	8	8	8	8	8	8	8	No shift	
logical count in			14	14	14	14	14	14	14	Right	
register	DSL	R	1	1	1	1	1	1	1	Incremental	
			16	16	16	16	16	16	16	Left	
			1	1	1	1	1	1	1	Incremental	

See footnotes at end of list.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-87665
		REVISION LEVEL B	SHEET 49

DESC FORM 193A
JUL 91

74E ■ 9004708 0000144 714 ■

MIL-STD-1750 implemented instruction	Mnemonic	Address mode	Number of clock cycles								Notes
			WD = Wait states instr. fetch								
			0	1	2	1	2	1	2		
			WA = Wait states data R/W								
			0	0	0	1	1	2	2		
Double shift arithmetic count in register	DSAR	R	8	8	8	8	8	8	8	No shift Right Incremental Left Incremental	
			14	14	14	14	14	14	14		
	DSAR	R	1	1	1	1	1	1	1		
			16	16	16	16	16	16	16		
			1	1	1	1	1	1	1		
Double shift cyclic count in register	DSCR	R	8	8	8	8	8	8	8	No shift Right Incremental Left Incremental	
			14	14	14	14	14	14	14		
	DSCR	R	1	1	1	1	1	1	1		
			16	16	16	16	16	16	16		
			1	1	1	1	1	1	1		
Load/store/exchange											
Load single precision	L	R	4	5	6	5	6	5	6		
	L	B	10	11	12	12	13	13	14		
	L	BX	10	11	12	12	13	13	14		
	L	ISP	4	5	6	5	6	5	6		
	L	ISN	4	5	6	5	6	5	6		
	L	D	12	14	16	15	17	16	18		
	L	DX	12	14	16	15	17	16	18		
	L	IM	8	10	12	10	12	10	12		
	L	IMX	8	10	12	10	12	10	12		
	L	I	16	18	20	20	22	22	24		
L	IX	16	18	20	20	22	22	24			
Load double precision	DL	R	6	6	6	6	6	6	6		
	DL	B	14	14	14	16	16	18	18		
	DL	BX	14	14	14	16	16	18	18		
	DL	D	16	18	20	20	22	22	24		
	DL	DX	16	18	20	20	22	22	24		
	DL	I	22	24	26	27	29	30	32		
	DL	IX	22	24	26	27	29	30	32		
Load floating point extended precision	EFL	D	20	22	24	25	27	28	30		
	EFL	DX	20	22	24	25	27	28	30		
Load from upper byte	LUB	D	12	14	16	15	17	16	18		
	LUB	DX	12	14	16	15	17	16	18		
	LUB	I	16	18	20	20	22	22	24		
	LUB	IX	16	18	20	20	22	22	24		
Load from lower byte	LLB	D	12	14	16	15	17	16	18		
	LLB	DX	12	14	16	15	17	16	18		
	LLB	I	16	18	20	20	22	22	24		

See footnotes at end of list.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-87665
		REVISION LEVEL B	SHEET 50

DESC FORM 193A
JUL 91

74E ■ 9004708 0000145 650 ■

MIL-STD-1750 implemented instruction	Mnemonic	Address mode	Number of clock cycles								Notes
			W0 = Wait states instr. fetch								
			0	1	2	1	2	1	2		
			WA = Wait states data R/W								
			0	0	0	1	1	2	2		
Store single precision	ST	B	10	11	12	12	13	13	14		
	ST	BX	10	11	12	12	13	13	14		
	ST	D	12	14	16	15	17	16	18		
	ST	DX	12	14	16	15	17	16	18		
	ST	I	16	18	20	20	22	22	24		
	ST	IX	16	18	20	20	22	22	24		
Store a positive constant	STC	D	12	14	16	15	17	16	18		
	STC	DX	12	14	16	15	17	16	18		
	STC	I	16	18	20	20	22	22	24		
	STC	IX	16	18	20	20	22	22	24		
Store double precision	DST	B	14	15	16	17	18	19	20		
	DST	BX	14	15	16	17	18	19	20		
	DST	D	16	18	20	20	22	22	24		
	DST	DX	16	18	20	20	22	22	24		
	DST	I	20	22	24	25	27	28	30		
	DST	IX	20	22	24	25	27	28	30		
Store register through mask	SRM	D	18	20	22	22	24	24	26	Bus lock	
	SRM	DX	18	20	22	22	24	24	26	Bus lock	
Store floating Point extended Precision	EFST	D	20	22	24	25	27	28	30		
	EFST	DX	20	22	24	25	27	28	30		
Store into upper byte	STUB	D	16	18	20	20	22	22	24	Bus lock	
	STUB	DX	16	18	20	20	22	22	24	Bus lock	
	STUB	I	20	22	24	25	26	28	30	Bus lock	
	STUB	IX	20	22	24	25	26	28	30	Bus lock	
Store into lower byte	STLB	D	16	18	20	20	22	22	24	Bus lock	
	STLB	DX	16	18	20	20	22	22	24	Bus lock	
	STLB	I	20	22	24	25	27	28	30	Bus lock	
	STLB	IX	20	22	24	25	27	28	30	Bus lock	
Exchange Bytes in register Words in register	XBR	R	4	5	6	5	6	5	6		
	XWR	R	4	5	6	5	6	5	6		
Multiple load/store											
Push multiple registers onto the stack	PSHM	R	16	17	18	18	19	19	20	One push Incremental	
	PSHM	R	8	8	8	9	9	10	10		

See footnotes at end of list.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-87665
		REVISION LEVEL B	SHEET 51

DESC FORM 193A
JUL 91

74E ■ 9004708 0000146 597 ■

MIL-STD-1750 implemented instruction	Mnemonic	Address mode	Number of clock cycles								Notes
			W0 = Wait states instr. fetch 0 1 2 1 2 1 2								
			WA = Wait states data R/W 0 0 0 1 1 2 2								
Pop multiple registers off the stack	POPM	R	18	19	20	20	21	21	22	One pop Incremental	
	POPM	R	10	10	10	11	11	12	12		
Load multiple registers	LM	D	16	18	20	19	21	20	22	One load Incremental One load Incremental	
	LM	D	4	4	4	5	5	6	6		
	LM	DX	16	18	20	19	21	20	22		
	LM	DX	4	4	4	5	5	6	6		
Store multiple registers	STM	D	14	16	18	17	19	18	20	One load Incremental One load Incremental	
	STM	D	4	4	4	5	5	6	6		
	STM	DX	14	16	18	17	19	18	20		
	STM	DX	4	4	4	5	5	6	6		
Move multiple words memory-to-memory	MOV	D	8	9	10	9	10	9	10	No move One move Incremental	
	MOV	D	24	26	28	27	29	28	30		
	MOV	D	8	8	8	10	10	12	12		
Program control											
Jump on condition	JC	D	8	10	12	10	12	10	12	No jump Jump No jump Jump No jump Jump No jump Jump	
	JC	D	8	10	12	10	12	10	12		
	JC	DX	10	12	14	12	14	12	14		
	JC	DX	10	12	14	12	14	12	14		
	JC	I	12	14	16	15	17	16	18		
	JC	I	12	14	16	15	17	16	18		
	JC	IX	14	16	18	17	19	18	20		
	JC	IX	14	16	18	17	19	18	20		
Jump to subroutine	JS	D	10	12	14	12	14	12	14		
	JS	DX	10	12	14	12	14	12	14		
Subtract one and jump	SOJ	D	14	17	20	17	20	17	20	No jump Jump No jump Jump	
	SOJ	D	10	11	12	11	12	11	12		
	SOJ	DX	16	19	22	19	22	19	22		
	SOJ	DX	12	13	14	13	14	13	14		
Branch unconditionally	BR	ICR	8	10	12	10	12	10	12		
Branch if equal to zero	BEZ	ICR	4	5	6	5	6	5	6	No branch Branch	
	BEZ	ICR	8	10	12	10	12	10	12		
Branch if less than zero	BLT	ICR	4	5	6	5	6	5	6	No branch Branch	
	BLT	ICR	8	10	12	10	12	10	12		

See footnotes at end of list.

STANDARDIZED
MILITARY DRAWING
DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

SIZE
A

5962-87665

REVISION LEVEL
B

SHEET

52

74E 9004708 0000147 423

MIL-STD-1750 implemented instruction	Mnemonic	Address mode	Number of clock cycles								Notes
			WD = Wait states instr. fetch								
			0	1	2	1	2	1	2		
			WA = Wait states data R/W								
			0	0	0	1	1	2	2		
Branch if less than or equal to zero	BLE	ICR	4	5	6	5	6	5	6	No branch Branch	
	BLE	ICR	8	10	12	10	12	10	12		
Branch if greater than zero	BGT	ICR	4	5	6	5	6	5	6	No branch Branch	
	BGT	ICR	8	10	12	10	12	10	12		
Branch if not equal to zero	BNZ	ICR	4	5	6	5	6	5	6	No branch Branch	
	BNZ	ICR	8	10	12	10	12	10	12		
Branch if greater than or equal to zero	BGE	ICR	4	5	6	5	6	5	6	No branch Branch	
	BGE	ICR	8	10	12	10	12	10	12		
Branch to executive	BEX	S	71	77	77	88	88	89	89	No MMU With MMU	
	BEX	S	75	75	75	86	86	97	97		
Load status	LST	D	32	34	36	37	39	40	42	No MMU With MMU No MMU With MMU No MMU With MMU No MMU With MMU	
	LST	D	34	36	38	39	41	42	44		
	LST	DX	32	34	36	37	39	40	42		
	LST	DX	34	36	38	39	41	42	44		
	LST	I	38	40	42	44	46	48	50		
	LST	I	40	42	44	46	48	50	52		
	LST	IX	38	40	42	44	46	48	50		
	LST	IX	40	42	44	46	48	50	52		
Stack IC and jump to subroutine	SJS	D	14	16	18	17	19	18	20		
	SJS	DX	14	16	18	17	19	18	20		
Unstack IC and return from subroutine	URS	S	14	16	18	17	19	18	20		
No operation	NOP	S	4	4	4	4	4	4	4		
Break point	BPT	S	14	14	14	14	14	14	14	No console I/O	
Built-in function to implement external co-processor	BIF	D	30	31	32	32	33	33	34		
	BIF	DX	30	31	32	32	33	33	34		
	BIF	I	34	35	36	36	37	37	38		
	BIF	IX	34	35	36	36	37	37	38		

See footnotes at end of list.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-87665
		REVISION LEVEL B	SHEET 53

DESC FORM 193A
JUL 91

74E ■ 9004708 0000148 36T ■

MIL-STD-1750 implemented instruction	Mnemonic	Address mode	Number of clock cycles						Notes	
			WD = Wait states instr. fetch							
			0	1	2	1	2	1		2
			WA = Wait states data R/W							
			0	0	0	1	1	2	2	
Execute input/output	XIO	IM	34						Input	
	XIO	IMX	34						Input	
	XIO	IM	24						Output	
	XIO	IMX	24						Output	
Vectored input/output <u>2/ 3/ 4/</u>	VIO	D	70						Overhead-in	
	VIO	D	44						Incremental	
	VIO	D	8						Incremental-unused	
	VIO	DX	70						Overhead-in	
	VIO	DX	44						Incremental	
	VIO	DX	8						Incremental-unused	
	VIO	D	62						Overhead-out	
	VIO	D	36						Incremental	
	VIO	D	8						Incremental-unused	
	VIO	DX	62						Overhead-out	
	VIO	DX	36						Incremental	
	VIO	DX	8						Incremental-unused	

- 1/ The number of clock cycles required by the CPU is listed as a function of the number of wait states. Both instruction fetch and data read/write wait states of 0, 1, and 2 clock cycles are shown in this list.
- 2/ Overhead-in is the input VIO instruction overhead including one XIO.
- 3/ Incremental is the number of cycles for each additional XIO.
- 4/ Incremental unused is the number of cycles for each unused bit(0) in the vector register.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-87665
		REVISION LEVEL B	SHEET 54

DESC FORM 193A
JUL 91

74E ■ 9004708 0000149 276 ■

6.6.2.1 Instruction clock cycles built in functions - Device types 05, 06, and 07 only.

Instruction	Mnemonic	Address mode	# of clocks	Notes
Memory parametric dot product single	VDPS	4F3(RA)	10+(8N)	Interruptable
Memory parametric dot product-double	VDPD	4F1(RA)	10+(16N)	Interruptable
3 X 3 register dot product	R3DP	4F03	6	
Double precision multiply accumulate	MACD	4F02	8	
Polynomial	POLY	4F06	7N-2	
Clear accumulator	CLAC	4F00	4	
Store accumulator (32-bit)	STA	4F08	7	
Store accumulator (48-bit)	STAL	4F04	11	
Load accumulator (32-bit)	LAC	4F05	9	
Load accumulator long (48-bit)	LACL	4F07	9	
Move mmu page block	MMPG	4F0F		Privileged
Load timer A reset register	LTAR	4F0D	4	
Load timer B reset register	LTBR	4F0E	4	

NOTE: 6.6.1 and 6.6.2 show the number of basic CPU clock cycles required for each device type to execute listed instructions. Specific application code may require additional clock cycles due to operand dependencies which are created by the sequence of instructions in the application code. These operand dependent additional clock cycles are not included in 6.1.1 and 6.1.2.

6.7 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-87665
		REVISION LEVEL B	SHEET 55

DESC FORM 193A
JUL 91

74E ■ 9004708 0000150 T18 ■