REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																								
SHEET																								
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SHEET	22	23	24	25																				
REV STATUS OF SHEETS	REV																							
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21		

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY: Robert M. Hebes

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APPROVED BY: [signature]

DRAWING APPROVAL DATE: 20 DECEMBER 1988

REVISION LEVEL:

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, LINEAR, MIL-STD-1553 BUS CONTROLLER, RTU, AND MONITOR UNIT, HYBRID

SIZE	CAGE CODE	
A	67268	5962-88585

SHEET 1 OF 25

DESC FORM 193
SEP 87

* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60911

5962-E829

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

5962-88585	01	X	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device type. The device type shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	BUS-65600	MIL-STD-1553, BUS controller, RTU, and monitor unit

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
X	See figure 1 (78-lead, 1.870" x 2.100" x .250"), dual-in-line package
Y	See figure 2 (82-lead, 2.190" x 1.600" x .171"), flat package

1.3 Absolute maximum ratings.

Supply voltage range (V_{CC})	-0.5 V dc to +7.0 V dc
Input voltage range (V_{IN})	GND -0.3 V dc to V_{CC} +0.3 V dc
Supply current (I_{CC})	70 mA 1/
Power dissipation (P_D)	385 mW 1/
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Thermal rise, junction-to-case (Δ_{TJ})	+5°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	4.5 V dc to 5.5 V dc
Minimum logic high input voltage (V_{IH})	2.4 V dc
Maximum logic low input voltage (V_{IL})	0.7 V dc
Case operating temperature range (T_C)	-55°C to +125°C
Operating frequency (F_{OP})	12.0 MHz

1/ Applies up to T_C = +125°C with all outputs open.

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics

MIL-STD-1553 - Aircraft Internal Time Division Command/Response Multiplex Data Bus

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 3.

3.2.2 Block diagram. The block diagram shall be as specified on figure 4.

3.2.3 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-M-38510. The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.5 herein.

3.5 Manufacturer's eligibility. In addition to the general requirements of MIL-M-38510, appendix G, the manufacturer of the part described herein shall submit, for DESC-ECS review, electrical test data (variables format) on one QCI group A lot sample, produced on the certified line, for each device type listed herein. The data should also include a summary of all parameters manually tested, and for those which, if any, are guaranteed.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, unless otherwise specified		Group A subgroups 1/	Limits		Unit
					Min	Max	
Supply current	I_{CC}	V_{CC} = 5.5 V, F_{IN} = 12 MHz, measured at pin 20 for X case outline and pin 40 for Y case outline with all outputs open		1, 2, 3		70	mA
High level output voltage 2/	V_{OH1}	V_{CC} = 4.5 V, V_{IH} = 2.5 V, V_{IL} = 0.4 V	I_{OH} = -5.2 mA	1, 2, 3	2.7		V
High level output voltage 3/	V_{OH2}		I_{OH} = -40 µA	1, 2, 3	2.7		
High level output voltage 4/	V_{OH3}		I_{OH} = -80 µA	1, 2, 3	2.7		
Low level output voltage 2/	V_{OL1}	V_{CC} = 4.5 V, V_{IH} = 2.5 V, V_{IL} = 0.4 V	I_{OL} = 5.2 mA	1, 2, 3		0.4	V
Low level output voltage 3/	V_{OL2}		I_{OL} = 1.6 mA	1, 2, 3		0.4	
Low level output voltage 4/	V_{OL3}		I_{OL} = 2.4 mA	1, 2, 3		0.4	
High level input current 5/	I_{IH1}	V_{CC} = 5.5 V, V_{IN} = 2.5 V		1, 2, 3	-20	+20	µA
High level input current 6/	I_{IH2}			1, 2, 3	-10	+10	
High level input current 7/	I_{IH3}			1, 2, 3	0.0	-250	
High level input current 8/	I_{IH4}			1, 2, 3	0.0	-800	
Low level input current 5/	I_{IL1}	V_{CC} = 5.5 V, V_{IN} = 0.4 V		1, 2, 3	-20	+20	µA
Low level input current 6/	I_{IL2}			1, 2, 3	-10	+10	
Low level input current 7/	I_{IL3}			1, 2, 3	0.0	-500	
Low level input current 8/	I_{IL4}			1, 2, 3	0.0	1.6	mA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C < T_C < +125°C$, unless otherwise specified	Group A subgroups 1/	Limits		Unit
				Min	Max	
Functional tests 9/		V_{CC} = 4.5 V, V_{IH} = 2.5 V, V_{IL} = 0.4 V, f_{IN} = 12 MHz	7, 8			Pass/ fail
Delay timing:		V_{CC} = 4.5 V, V_{IH} = 2.5 V, V_{IL} = 0.4 V, f_{IN} = 12 MHz, See figures 5 thru 10 10/ 11/				
$\overline{BUSGRNT}$ delay, CMD word	t_{d1}		9,10,11		1.5	µs
$\overline{BUSGRNT}$ delay, TX data word	t_{d2}		9,10,11		15.5	µs
$\overline{BUSGRNT}$ delay, RX data	t_{d3}		9,10,11		2.33	µs
$\overline{BUSGRNT}$ to $\overline{BUSACK}$ delay (RTU handshake)	t_{d4}		9,10,11		250	ns
$\overline{BUSACK}$ to $\overline{OE}$ delay	t_{d5}		9,10,11		25	ns
$\overline{OE}$ to $\overline{CS}$ delay	t_{d6}		9,10,11		25	ns
$\overline{CS}$ to $\overline{ADRINC}$ delay	t_{d7}		9,10,11		110	ns
$\overline{BUSACK}$ to $\overline{WR}$ delay (BC write)	t_{d8}		9,10,11	300	378	ns
$\overline{WR}$ to $\overline{CS}$ delay	t_{d9}		9,10,11		25	ns
$\overline{NBGRNT}$ to LMC, WC, T/$\overline{R}$ delay	t_{d10}		9,10,11	500	667	ns
LMC to $\overline{ILLCMD}$ latch	t_{d11}		9,10,11	250		ns
$\overline{NBGRNT}$ to $\overline{INCMD}$ delay	t_{d12}		9,10,11	0.9	1.1	µs
$\overline{BUSACK}$ to $\overline{SOM}$ delay	t_{d13}		9,10,11	140	190	ns
$\overline{NBGRNT}$ low to status latch	t_{d14}		9,10,11	2.5	3.5	µs
$\overline{CS}$ to $\overline{ADRINC}$ delay (RTU read)	t_{d15}		9,10,11		110	ns
$\overline{BUSACK}$ to $\overline{WR}$ delay (RTU write)	t_{d16}		9,10,11	140	225	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C < T_C < +125°C$, unless otherwise specified	Group A subgroups 1/	Limits		Unit
				Min	Max	
Delay timing - continued:		V_{CC} = 4.5 V, V_{IH} = 2.5 V, V_{IL} = 0.4 V, f_{IN} = 12 MHz, See figures 5 thru 10 10/ 11/				
$\overline{WR}$ to $\overline{CS}$ delay (RTU write)	t_{d17}		9,10,11		25	ns
$\overline{BUSREQ}$ to $\overline{BUSGRNT}$ delay	t_{d18}		9,10,11		2.0	µs
$\overline{BUSGRNT}$ to $\overline{BUSACK}$ delay (MT transfer)	t_{d19}		9,10,11		250	ns
$\overline{BUSACK}$ to $\overline{WR}$ delay (MT transfer)	t_{d20}		9,10,11	300	378	ns
Pulse timing width:		V_{CC} = 4.5 V, V_{IH} = 2.5 V, V_{IL} = 0.4 V, f_{IN} = 12 MHz, See figures 5 thru 10 9/ 11/				
$\overline{BUSREQ}$ pulse width (RTU handshake)	t_{pw1}		9,10,11	667		ns
$\overline{BUSACK}$ pulse width (RTU handshake)	t_{pw2}		9,10,11	475	600	ns
$\overline{CS}$ ($\overline{OE}$) pulse width (BC read)	t_{pw3}		9,10,11	640	690	ns
$\overline{ADRINC}$ pulse width	t_{pw4}		9,10,11	60	110	ns
$\overline{CS}$ and $\overline{WR}$ pulse width (BC write)	t_{pw5}		9,10,11	140	190	ns
$\overline{NBGRNT}$ pulse width	t_{pw6}		9,10,11	140	190	ns
$\overline{SOM}$ pulse width	t_{pw7}		9,10,11	140	190	ns
$\overline{CS}$, $\overline{OE}$, and $\overline{BUSACK}$ pulse width (RTU read)	t_{pw8}		9,10,11	475	600	ns
$\overline{CS}$ and $\overline{WR}$ pulse width (RTU write)	t_{pw9}		9,10,11	140	190	ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C < T_C < +125°C$, unless otherwise specified	Group A subgroups 1/	Limits		Unit
				Min	Max	
Pulse width timing - continued:		V_{CC} = 4.5 V, V_{IH} = 2.5 V, V_{IL} = 0.4 V, f_{IN} = 12 MHz, See figures 5 thru 10 9/ 11/				
$\overline{BUSREQ}$ pulse width (BC handshake)	t_{pw10}		9,10,11	752		ns
$\overline{BUSGRNT}$ pulse width (BC handshake)	t_{pw11}		9,10,11	250		ns
$\overline{BUSACK}$ pulse width (BC handshake)	t_{pw12}		9,10,11	640	690	ns
$\overline{BUSGRNT}$ pulse width (MT transfer)	t_{pw13}		9,10,11	250		ns
Set-up timing:		V_{CC} = 4.5 V, V_{IH} = 2.5 V, V_{IL} = 0.4 V, f_{IN} = 12 MHz, See figures 5 thru 10 9/ 11/				
BC read data set-up time	t_{s1}		9,10,11		250	ns
BC write data valid set-up time	t_{s2}		9,10,11	100		ns
CMD valid set-up time	t_{s3}		9,10,11	100		ns
RTU read data set-up time	t_{s4}		9,10,11		166	ns
RTU write data valid set-up prior to leading edge of WR	t_{s5}		9,10,11	100		ns
ID word valid set-up time	t_{s6}		9,10,11	100		ns
Maximum clock frequency	f_{MAX}	50% duty cycle 10/	9,10,11		12.0	MHz

See footnotes on next page.

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1/ All Group A subgroup testing may be performed concurrently.

2/ Measured at the following pins:

Case X: Pins 14, 21 - 28, 54, and 60 - 67.
Case Y: Pins 28, 29, and 66 - 81.

3/ Measured at the following pins:

Case X: Pins 3 - 5, 9, 12, 13, 15 - 19, 29, 30, 42 - 44, 46, 49, 51 - 53, 55, 57, 59, 68, 71, and 75, 78.
Case Y: Pins 5 - 10, 18, 23 - 27, 30 - 32, 34 - 36, 38, 39, 44, 50, 58, and 63 - 65.

4/ Measured at the following pins:

Case X: Pins 31, 37, 69, and 76.
Case Y: Pins 48, 49, 61, and 62.

5/ Measured at the following pins:

Case X: Pins 1 and 45.
Case Y: Pins 2 and 11.

6/ Measured at the following pins:

Case X: Pins 2, 6 - 8, 10, 21 - 28, 32, 36, 38, 39, 41, 47, 48, 60 - 67, 70, and 77.
Case Y: Pins 3, 4, 12, 14 - 17, 20, 45 - 47, 51, 59, 60, and 66 - 81.

7/ Measured at the following pins:

Case X: Pins 33 and 58.
Case Y: Pins 37 and 57.

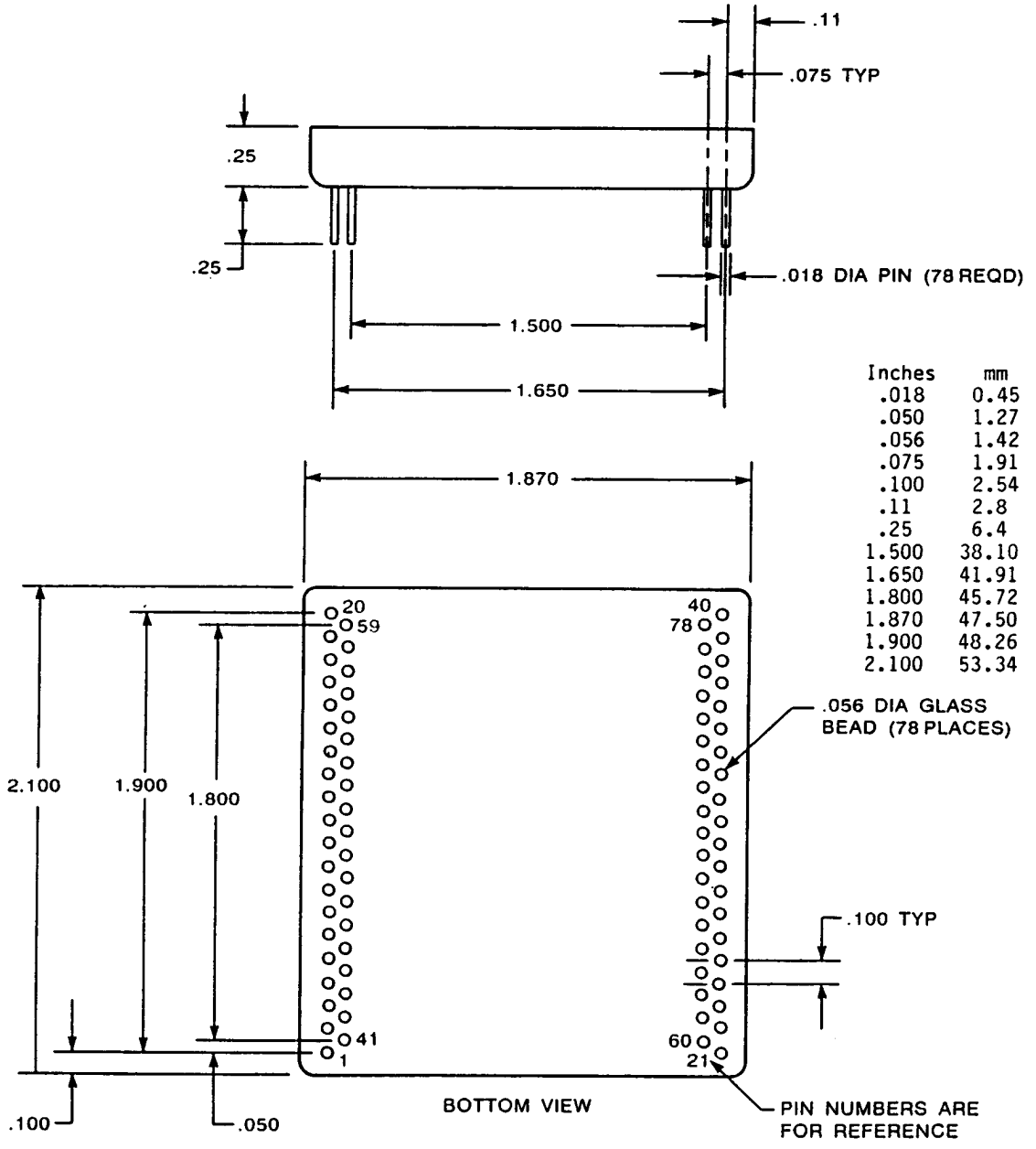
8/ Measured at the following pins:

Case X: Pins 34, 35, and 72 - 74.
Case Y: Pins 52 - 56.

9/ Functional tests performed to verify functionality of device as a MIL-STD-1553 Bus Controller (BC), Remote Terminal Unit (RTU), and Bus Monitor (BM). These tests shall be part of the vendors' test tapes and shall be available upon request.

10/ If not tested, shall be guaranteed to the limits specified in table I.

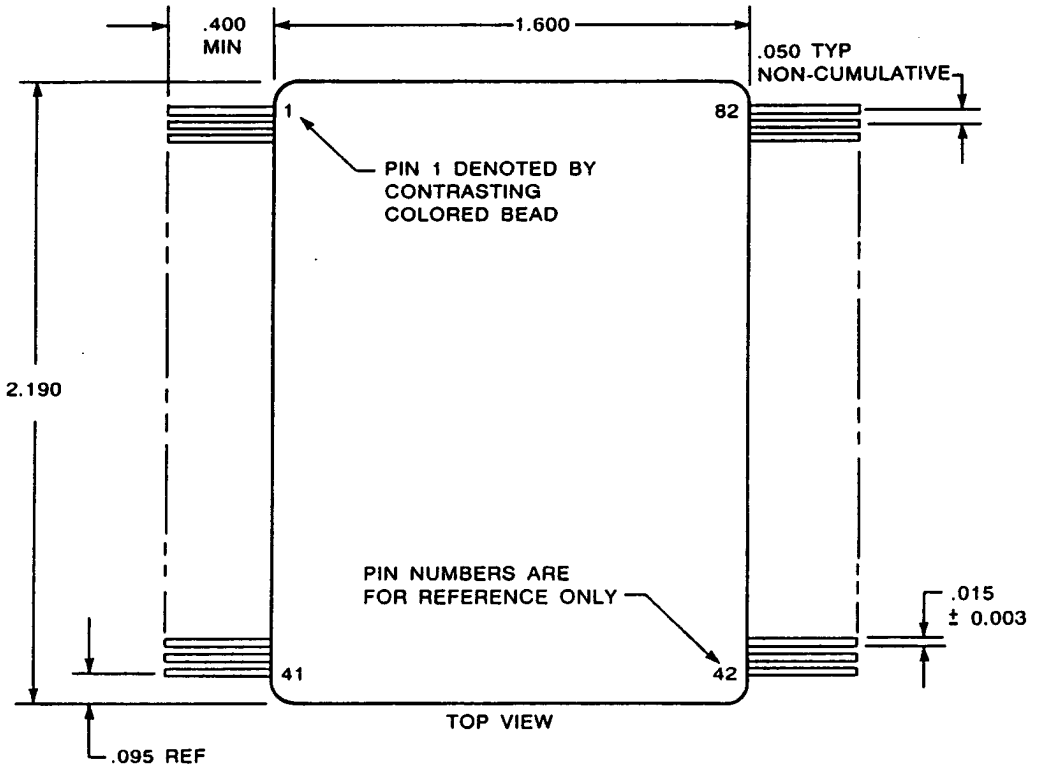
11/ All timing characteristics measured at 2.7 V and 0.4 V unless otherwise specified.

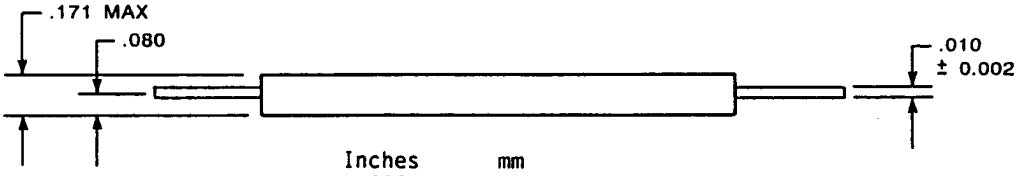


Inches	mm
.018	0.45
.050	1.27
.056	1.42
.075	1.91
.100	2.54
.11	2.8
.25	6.4
1.500	38.10
1.650	41.91
1.800	45.72
1.870	47.50
1.900	48.26
2.100	53.34

NOTES:
1. Dimensions are in inches.
2. Metric equivalents are given for general information only.
3. Unless otherwise specified, tolerance is ±.005 (0.13 mm) for three place decimals and ±.01 (0.25 mm) for two place decimals.

FIGURE 1. Case outline X.





Inches	mm
.002	0.05
.003	0.08
.010	0.25
.015	0.38
.050	1.27
.080	2.03
.095	2.41
.171	4.34
.400	10.16
1.600	40.64
2.190	55.63

NOTES:
1. Dimensions are in inches.
2. Metric equivalents are given for general information only.
3. Unless otherwise specified, tolerance is ±.005 (.13 mm) for three place decimals.

FIGURE 2. Case outline Y.

Device type	All		Device type	All	
Case outlines	X	Y	Case outlines	X	Y
Terminal number	Terminal symbol	Terminal symbol	Terminal number	Terminal symbol	Terminal symbol
1	RT/$\overline{BC}$	NC	42	$\overline{NBGRNT}$	NC
2	$\overline{MT}$	RT/$\overline{BC}$	43	$\overline{BITEN}$	GROUND
3	$\overline{STATEN}$	$\overline{BCSTART}$	44	$\overline{WR}$	$\overline{SOM}$
4	$\overline{TIMEOUT}$	$\overline{MT}$	45	$\overline{BUSGRNT}$	12MHz
5	$\overline{HSFAIL}$	$\overline{NBGRNT}$	46	$\overline{LOOPERR}$	$\overline{RXDATA\ B}$
6	$\overline{DBACCEPT}$	$\overline{STATEN}$	47	$\overline{SSBUSY}$	RXDATA B
7	$\overline{SSFLAG}$	$\overline{BITEN}$	48	$\overline{ILLCMD}$	TXDATA B
8	$\overline{SVCREQ}$	$\overline{TIMEOUT}$	49	$\overline{ADRINC}$	$\overline{TXDATA\ B}$
9	$\overline{INCMD}$	$\overline{WR}$	50	CHASSIS	$\overline{BCSTRCV}$
10	$\overline{SSER}$	$\overline{HSFAIL}$	51	WC0	$\overline{RESET}$
11	$\overline{TESTOUT}$	$\overline{BUSGRNT}$	52	WC2	RTAD4
12	WC1	$\overline{DBACCEPT}$	53	WC4	RTAD3
13	WC3	$\overline{LOOPERR}$	54	TXINH A	RTAD2
14	TXINH B	$\overline{SSFLAG}$	55	LMC	RTAD1
15	T/$\overline{R}$	$\overline{SSBUSY}$	56	$\overline{TESTIN}$	RTAD0
16	$\overline{CHA}$/CHB	$\overline{SVCREQ}$	57	$\overline{EOM}$	RTADP
17	$\overline{CS}$	$\overline{ILLCMD}$	58	$\overline{BUFENA}$	$\overline{NO\ DT}$
18	$\overline{OE}$	$\overline{INCMD}$	59	$\overline{BUSACK}$	$\overline{RXDATA\ A}$
19	BUSREQ	ADRINC	60	DB1	RXDATA A
20	+5V	$\overline{SSER}$	61	DB3	TXDATA A
21	DB0 (LSB)	CHASSIS	62	DB5	$\overline{TXDATA\ A}$
22	DB2	$\overline{TESTOUT}$	63	DB7	$\overline{MSGERR}$
23	DB4	WC0	64	DB9	$\overline{STATERR}$
24	DB6	WC1	65	DB11	LWORD
25	DB8	WC2	66	DB13	DB15 (MSB)
26	DB10	WC3	67	DB15 (MSB)	DB14
27	DB12	WC4	68	$\overline{STATERR}$	DB13
28	DB14	TXINH B	69	$\overline{TXDATA\ A}$	DB12
29	LWORD	TXINH A	70	RXDATA A	DB11
30	$\overline{MSGERR}$	T/$\overline{R}$	71	$\overline{NO\ DT}$	DB10
31	TXDATA A	LMC	72	RTAD0	DB9
32	$\overline{RXDATA\ A}$	$\overline{CHA}$/CHB	73	RTAD2	DB8
33	RTADP	$\overline{TESTIN}$	74	RTAD 4	DB7
34	RTAD1	$\overline{CS}$	75	$\overline{BCSTRCV}$	DB6
35	RTAD3	$\overline{EOM}$	76	TXDATA B	DB5
36	$\overline{RESET}$	$\overline{OE}$	77	$\overline{RXDATA\ B}$	DB4
37	$\overline{TXDATA\ B}$	$\overline{BUFENA}$	78	$\overline{SOM}$	DB3
38	RXDATA B	$\overline{BUSREQ}$	79	----	DB2
39	12MHz	$\overline{BUSACK}$	80	----	DB1
40	GND	+5V	81	----	DB0 (LSB)
41	$\overline{BCSTART}$	NC	82	----	NC

FIGURE 3. Terminal connections.

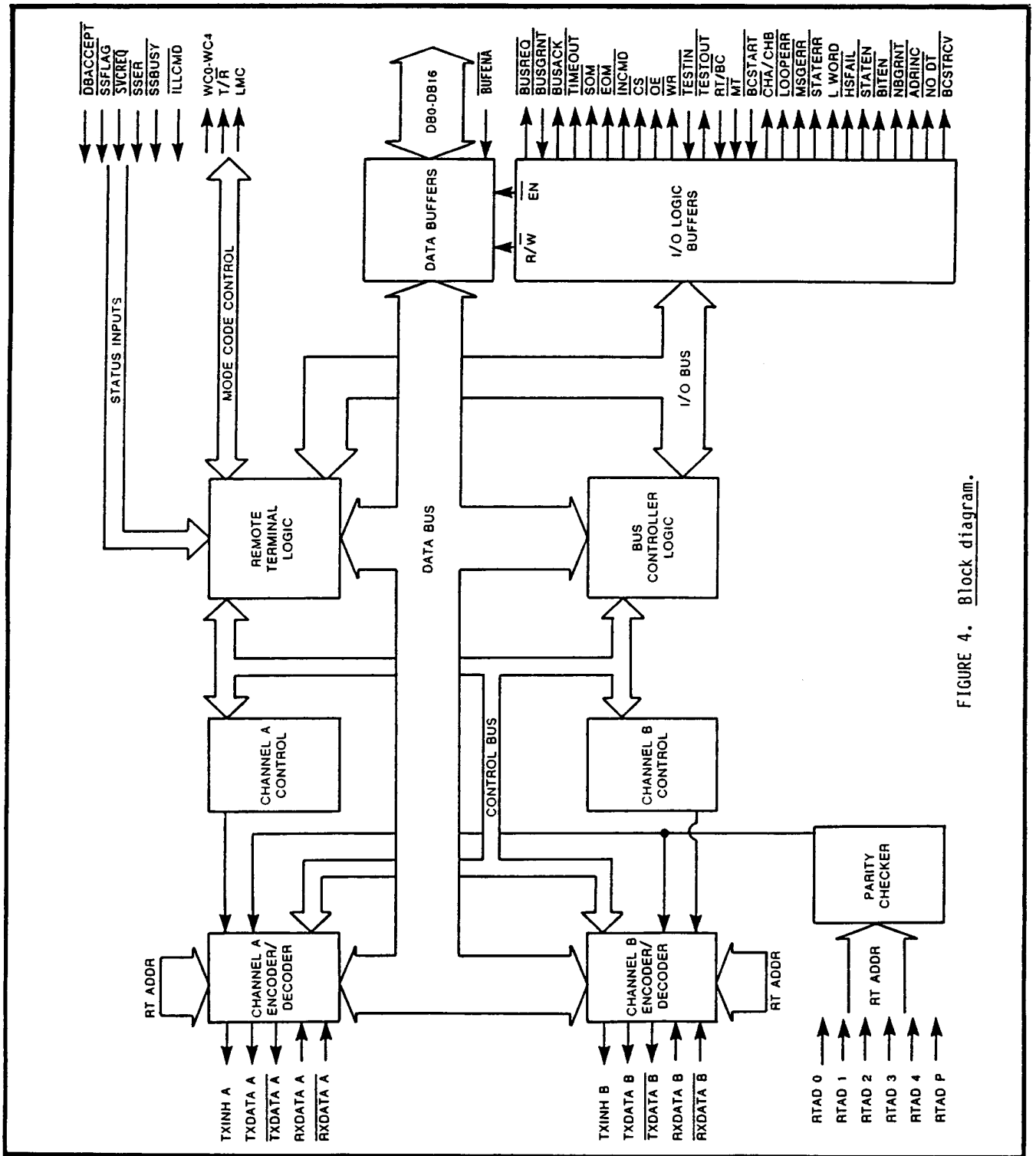


FIGURE 4. Block diagram.

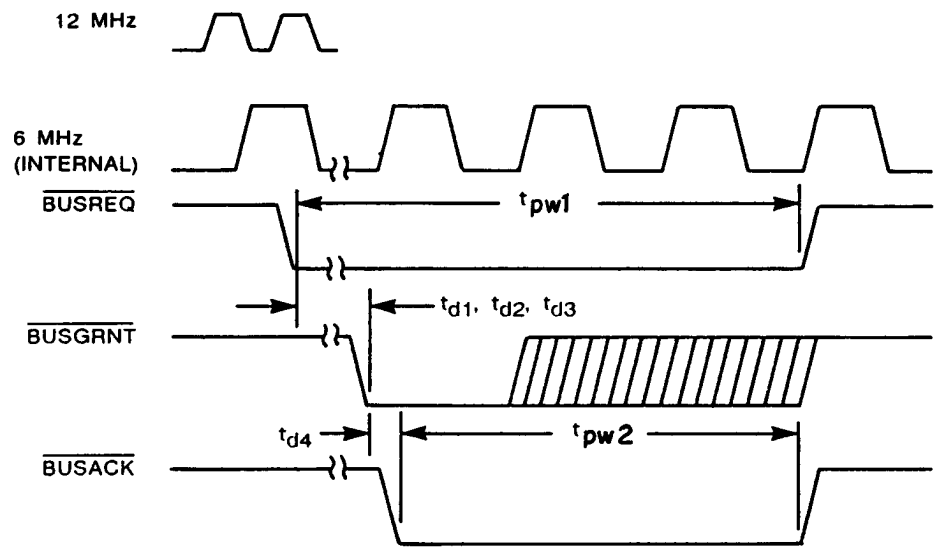


FIGURE 5. Timing diagram - RTU handshake.

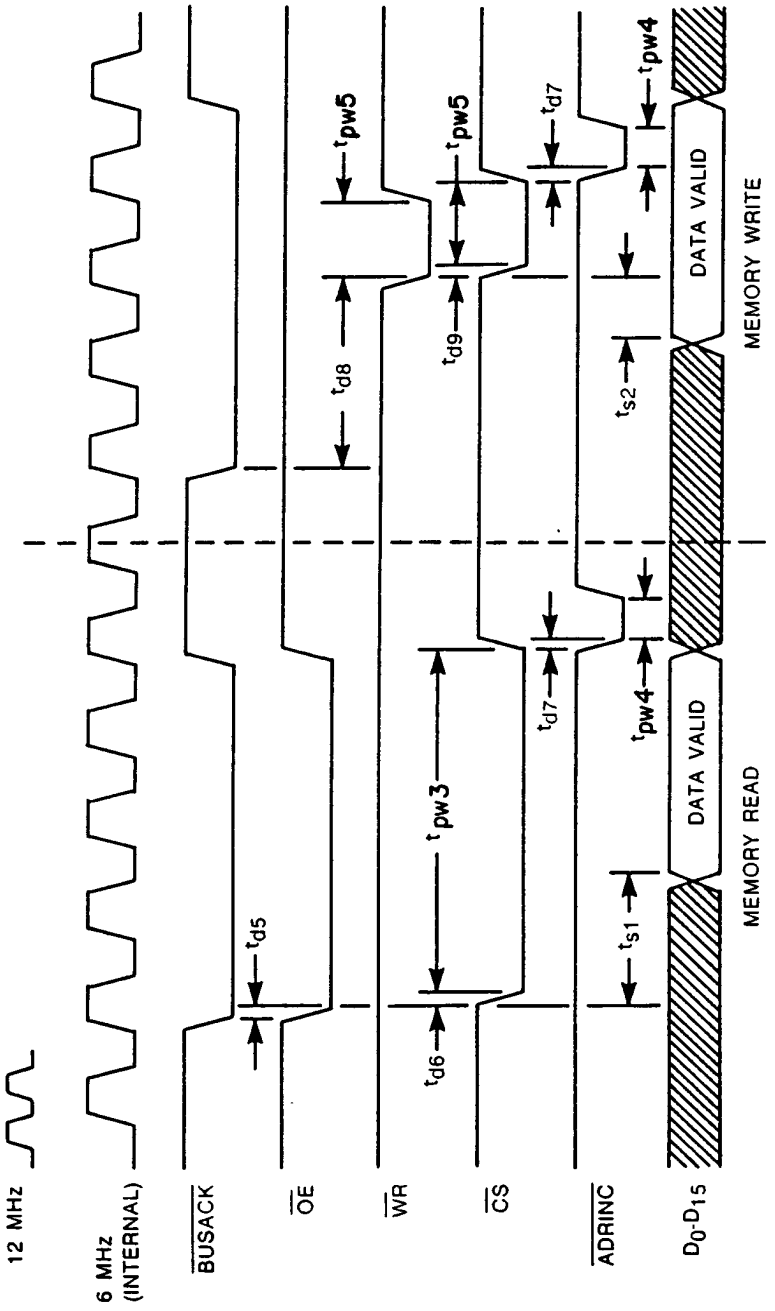


FIGURE 6. Timing diagram - BC read/write.

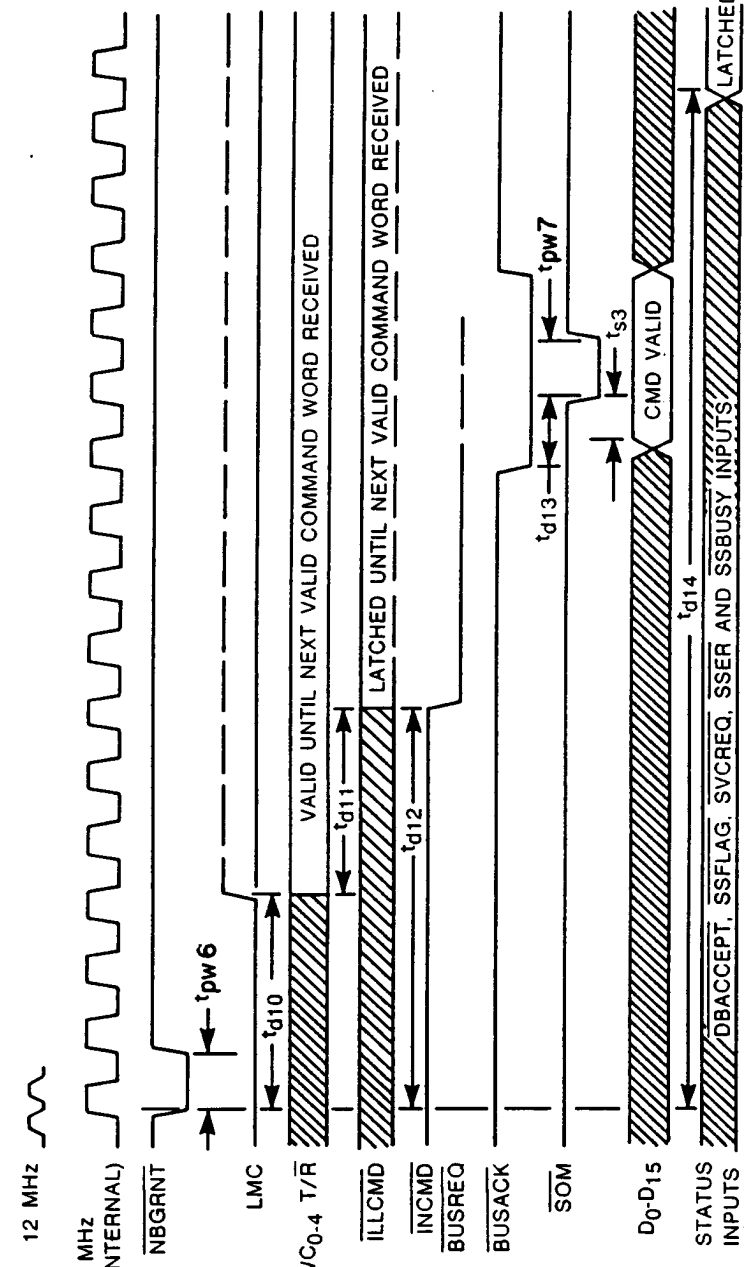


FIGURE 7. Timing diagram - RTU command word handling/status inputs.

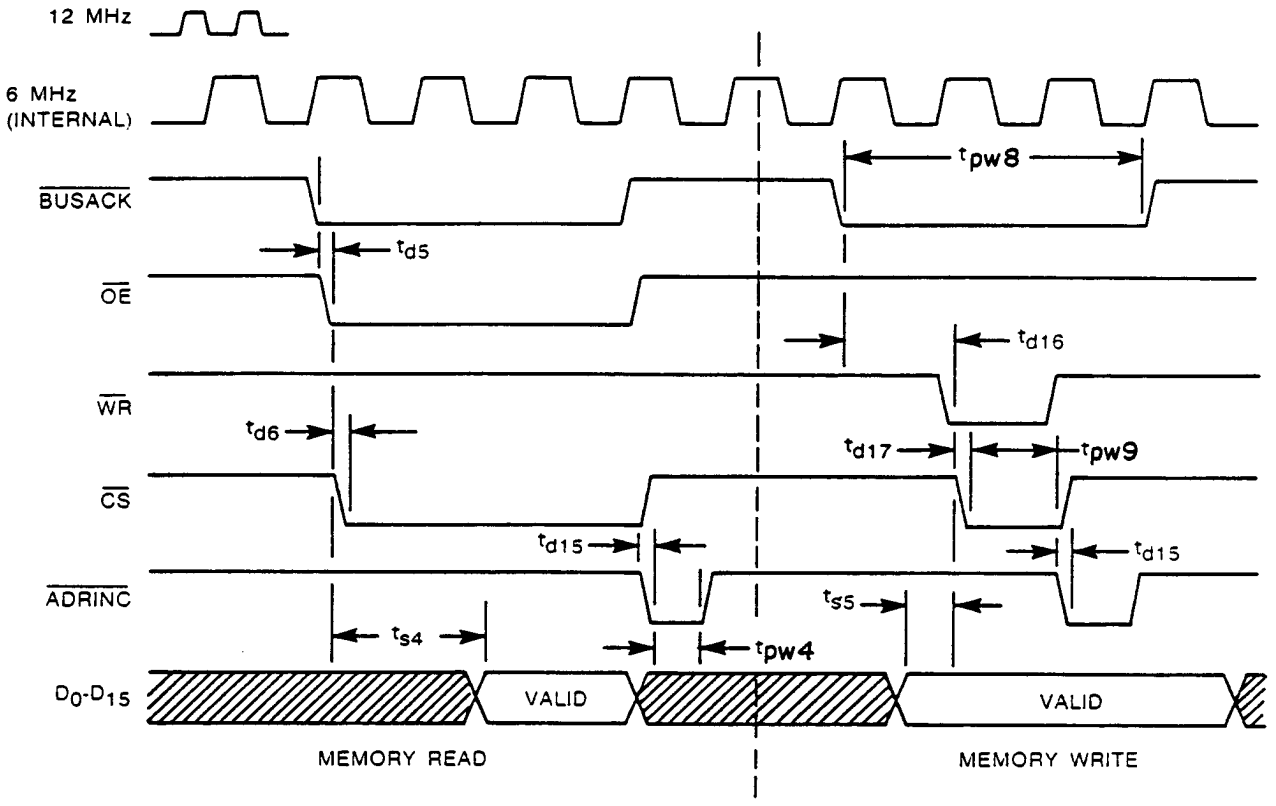


FIGURE 8. Timing diagram - RTU read/write.

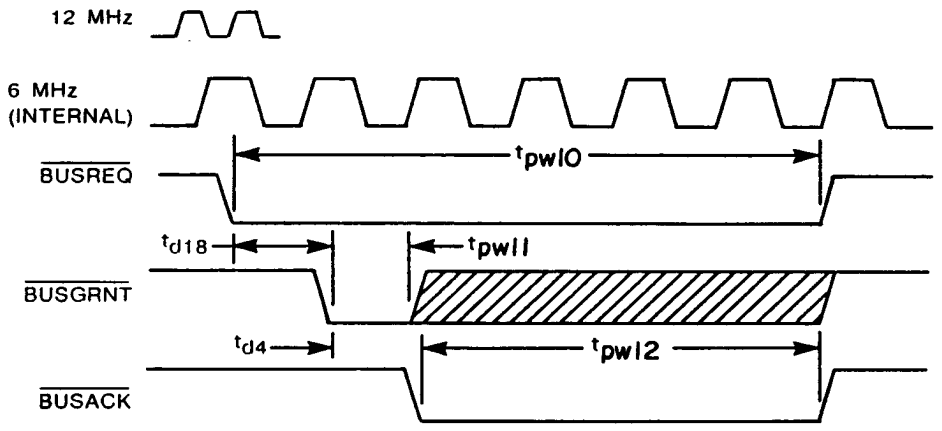


FIGURE 9. Timing diagram - BC handshake.

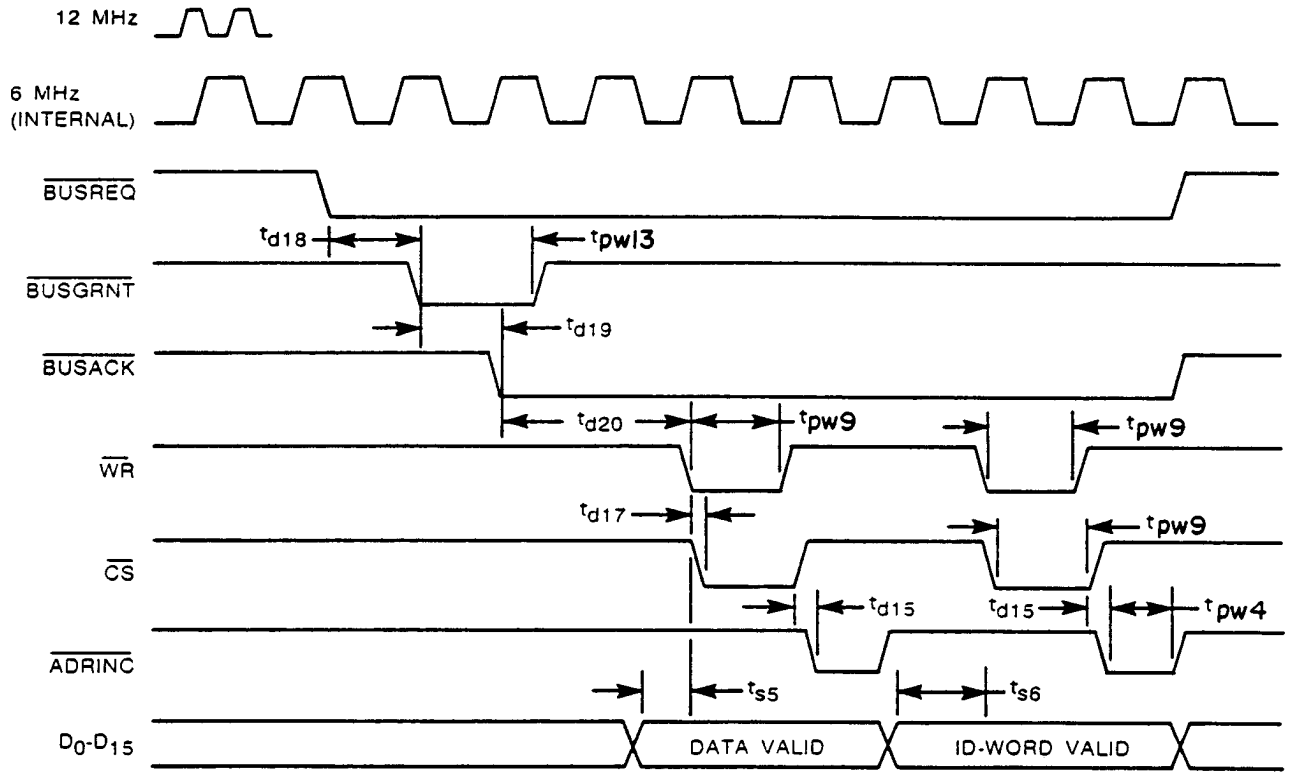


FIGURE 10. Timing diagram - MT transfer.

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3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.5. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5008 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5008 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 in table X, method 5008 of MIL-STD-883 shall be omitted.

4.3.2 Groups C and D inspections.

a. Group C end-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test method 1005 of MIL-STD-883 conditions:

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883, method 5008 test requirements	Subgroups (per method 5008, group A test table
Interim electrical parameters	1,7,9
Final electrical test parameters	1*,2,3,7*,8,9*, 10,11
Group A test requirements	1,2,3,7,8,9, 10,11
Groups C end-point electrical parameters	1,2,3,7,8,9, 10,11

* PDA applies to subgroups 1, 7, and 9.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Pin functions. Microcircuits conforming to this drawing shall have pin functions as specified in table III herein.

TABLE III. Pin functions.

Pin name	I/O	Description
RT/$\overline{BC}$	I	Remote Terminal/Bus Controller. Logic "1" for RT mode, logic "0" for BC mode.
$\overline{MT}$	I	Bus monitor. Logic "0" for MT mode, Logic "1" for BC mode.
$\overline{STATEN}$	O	Status Enable. Indicates status word being transferred on internal bus.
$\overline{TIMEOUT}$	O	Indicates No Response Timeout has occurred during BC or RTU (RT to RT transfer).
$\overline{HSFAIL}$	O	Handshake Failure. Indicates subsystem failed to grant a bus request (DMA handshake) within the required time period.
$\overline{DBACCEPT}$	I	Dynamic Bus Control Accept. Controls the DBACCEPT bit in RTU status word for response to valid mode command on 1553 bus.
$\overline{SSFLAG}$	I	Subsystem Flag. Controls SSFLAG in RTU status word.
$\overline{SVCREQ}$	I	Service Request. Controls SVCREQ bit in RTU status word.
$\overline{INCMD}$	O	In Command. Indicates BC/RTU currently in message transfer sequence.
$\overline{SSER}$	I	Subsystem Error. Controls Terminal Flag bit in status word.
$\overline{TESTOUT}$	-	Factory test pin, no connection.
WC1	O	Word Count bit 1. Received from Command Word.
WC3	O	Word Count bit 3. Received from Command Word.

TABLE III. Pin functions - Continued.

Pin name	I/O	Description
TXINH B	O	Transmitter Inhibit Channel B.
T/$\overline{R}$	O	Transmit/Receive. Indicates T/$\overline{R}$ bit of current Command Word in RTU mode.
CHA/$\overline{CHB}$	O	Channel A/Channel B. Indicates current selected channel.
$\overline{CS}$	O	Chip Select. Used for external memory operations.
$\overline{OE}$	O	Output Enable. Used for memory read operation.
$\overline{BUSREQ}$	O	Bus Request. Initiates handshaking prior to all subsystem transfers.
+5V	I	+5 V dc input.
DB0 (LSB)	I/O	Data Bus Bit 0.
DB2	I/O	Data Bus Bit 2.
DB4	I/O	Data Bus Bit 4.
DB6	I/O	Data Bus Bit 6.
DB8	I/O	Data Bus Bit 8.
DB10	I/O	Data Bus Bit 10.
DB12	I/O	Data Bus Bit 12.
DB14	I/O	Data Bus Bit 14.
LWORD	-	For factory use only. Last word output in BC mode indicates last data word of current message transfer has been transferred on data bus.
$\overline{MSGERR}$	O	Indicates error occurred during current message sequence in BC/RTU mode.
TXDATA A	O	Transmit Data A. Data output to tranceiver input.
$\overline{RXDATA\ A}$	I	Receive Data A. Data input from transceiver.
RTADP	I	RT Address Parity Bit.
RTAD1	I	RT Address Bit 1.
RTAD3	I	RT Address Bit 3.
$\overline{RESET}$	I	Resets all unit parameters (200 ns minimum pulse).

TABLE III. Pin functions - Continued.

Pin name	I/O	Description
TXDATA B	O	Transmit Data B. Data output to transmitter input.
RXDATA B	I	Receive Data B. Data input from transceiver.
12 MHz	I	12 MHz TTL clock.
GND	-	Signal ground.
BCSTART	I	Bus Controller Start. Initiates BC message transfer and begins MT operation (on rising edge).
NBGRNT	O	New Bus Grant. Indicates start of message transfer sequence.
BITEN	O	Built In Test Enable. Indicates RT transfer of BIT word on internal 16 bit bus.
WR	O	Write Enable. Enables memory write operation from unit.
BUSGRNT	I	Bus Grant. Response to BUSREQ output (DMA-type handshake).
LOOPERR	O	Loop Error. Logic "0" indicates failure during loop back of last transmitted data in BC/RTU mode.
SSBUSY	I	Subsystem Busy. Controls the (Subsystem) Busy bit in Status Word.
ILLCMD	I	Illegal Command. Used to block RT response to illegal command.
ADRINC	O	Address Increment. Low level pulse which returns high after the rising edge of CS (memory read/write). Used to increment external address counter.
CHASSIS	-	Chassis ground.
WC0	O	Word Count Bit 0. Received from Command Word.
WC2	O	Word Count Bit 2. Received from Command Word.
WC4	O	Word Count Bit 4. Received from Command Word.
TXINH A	O	Transmitter Inhibit Channel A.
LMC	O	Latched Mode Command. Logic "1" indicates current command word is a mode code; WC0 - WC4 specifies mode.
TESTIN	-	Factory test input-enable fail safe counter for selected channel.
EOM	O	End Of Message. Logic "0" (pulse) occurs when BC/RTU message is completed.

TABLE III. Pin functions - Continued.

Pin name	I/O	Description
$\overline{\text{BUFENA}}$	I	Buffer Enable. May be driven low during STATEN or BITEN low. Allows subsystem to read status or BIT words. Enables internal 16 bit bus onto subsystem bus.
$\overline{\text{BUSACK}}$	O	Bus Acknowledge. Low during DMA handshake, in response to $\overline{\text{BUSGRNT}}$.
DB1	I/O	Data Bus Bit 1.
DB3	I/O	Data Bus Bit 3.
DB5	I/O	Data Bus Bit 5.
DB7	I/O	Data Bus Bit 7.
DB9	I/O	Data Bus Bit 9.
DB11	I/O	Data Bus Bit 11.
DB13	I/O	Data Bus Bit 13.
DB15 (MSB)	I/O	Data Bus Bit 15.
$\overline{\text{STATERR}}$	O	Status Error. Indicates one or more bits set or address mismatch in received status word.
$\overline{\text{TXDATA A}}$	O	Transmit Data A. Data output to transceiver input.
RXDATA A	I	Receive Data A. Data input from transceiver.
$\overline{\text{NO DT}}$	O	No Data. Logic "0" indicates idle 1553, "1" indicates selected bus channel active.
RTAD0	I	RT Address Bit 0.
RTAD2	I	RT Address Bit 2.
RTAD4	I	RT Address Bit 4.
$\overline{\text{BCSTRCV}}$	O	Broadcast Receive. Indicates current command is broadcast.
TXDATA B	O	Transmit Data B. Data output to transmitter input.
$\overline{\text{RXDATA B}}$	I	Receive Data B. Data input from transceiver.
$\overline{\text{SOM}}$	O	Start Of Message. Indicates Command Word available to subsystem on parallel data bus. Active during the Command Word DMA handshake period.

6.4 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.5 Approved source of supply. An approved source of supply is listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/
5962-8858501XX	19645	BUS-65600-883B
5962-8858501YX	19645	BUS-65601-883B

1/ Caution. Do not use this number for item acquisition. Items acquired by this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
19645	ILC Data Device Corporation 105 Wilbur Place Bohemia, NY 11716