| REVISIONS | | | |
|---|---|---|---|
| LTR | DESCRIPTION | DATE (YR-MO-DA) | APPROVED |
| A | Technical changes were made in table I. Clarifications were made in figure 4. Editorial changes throughout. | 1990 AUG 20 | Weckman |

| | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| REV | | | | | | | | | | | | | | | | | | | | | | | | |
| SHEET | | | | | | | | | | | | | | | | | | | | | | | | |
| REV | A | A | | | A | | | | | | | | | | | | | | | | | | | |
| SHEET | 22 | 23 | 24 | 25 | 26 | | | | | | | | | | | | | | | | | | | |

| REV STATUS OF SHEETS | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| REV | A | | A | | A | | A | | | A | | A | | A | | | | | | | | A | | A |
| SHEET | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | | | |

PMIC N/A

**STANDARDIZED MILITARY DRAWING**

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY: Greg A. Pitz

CHECKED BY: Ray Monnin

APPROVED BY: D A DiCenzo

DRAWING APPROVAL DATE: 19 August 1988

REVISION LEVEL: A

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, DIGITAL BIPOLAR DYNAMIC MEMORY CONTROLLER MONOLITHIC SILICON

| SIZE | CAGE CODE | |
|---|---|---|
| A | 67268 | 5962-88696 |

SHEET 1

DESC FORM 193
SEP 87

* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60911

5962-E1774-1

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

| 5962-88696 | 01 | X | X |
|---|---|---|---|
| Drawing number | Device type (1.2.1) | Case outline (1.2.2) | Lead finish per MIL-M-38510 |

1.2.1 Device types. The device types shall identify the circuit function as follows:

| Device type | Generic number | Circuit function |
|---|---|---|
| 01 | 2968A | Dynamic memory controller |
| 02 | 2968A | Dynamic memory controller with output enable |

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

| Outline letter | Case outline |
|---|---|
| X | D-14 (48 lead, 2.435" x .620" x .225"), dual-in-line package |
| Y | C-7 (68 terminal, .962" x .962" x .120"), square chip carrier package |

1.3 Absolute maximum ratings.

| | |
|---|---|
| Supply voltage range | 0.5 V dc to 7.0 V dc |
| Input voltage range | 0.5 V dc to 5.5 V dc |
| Storage temperature range | -65°C to +150°C |
| Maximum power dissipation ($P_D$) 1/ | 1.63 W |
| Lead temperature (soldering, 10 seconds) | +300°C |
| Thermal resistance, junction-to-case ($\theta_{JC}$): | |
| Cases X and Y | See MIL-M-38510, appendix C |
| Junction temperature ($T_J$) | +185°C |
| DC voltage applied to outputs for high output state | -0.5 V to $V_{CC}$ maximum |
| DC input voltage | -0.5 V to +5.5 V |
| DC input current | -30 mA to +5.0 mA |

1.4 Recommended operating conditions.

| | |
|---|---|
| Supply voltage range ($V_{CC}$) | +4.5 V dc minimum to +5.5 V dc maximum |
| Minimum high level input voltage ($V_{IH}$) | +2.0 V dc |
| Maximum low level input voltage ($V_{IL}$) | +0.8 V dc |
| Case operating temperature range ($T_C$) | -55°C to +125°C |

1/ Must with stand added $P_D$ due to short circuit test, e.g; $I_{OS}$.



☆ U.S. GOVERNMENT PRINTING OFFICE: 1989 749-013

2. APPLICABLE DOCUMENTS

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawing (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth tables. The truth tables shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

3.2.4 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

TABLE I. Electrical performance characteristics.

| Test | Symbol | Conditions<br>$-55°C \le T_C \le +125°C$<br>$4.5\ V \le V_{CC} \le 5.5\ V$<br>Unless otherwise specified | Device type | Group A subgroups | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Output high voltage | $V_{OH}$ | $V_{CC}$ = 4.5 V<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$<br>$I_{OH}$ = -1 mA | All | 1, 2, 3 | 2.5 | | V |
| Output low voltage | $V_{OL}$ | $V_{CC}$ = 4.5 V, $V_{IN}$ = $V_{IH}$ or $V_{IL}$, $I_{OL}$ = 1 mA | All | | | 0.5 | V |
| | | $V_{CC}$ = 4.5 V, $V_{IN}$ = $V_{IH}$ or $V_{IL}$, $I_{OL}$ = 12 mA | All | | | 0.8 | V |
| Input high level | $V_{IH}$ | Guaranteed input logical-high voltage for all inputs | All | | 2.0 | | V |
| Input low level | $V_{IL}$ | Guaranteed input logical-low voltage for all inputs | All | | | 0.8 | V |
| Input clamp voltage | $V_{IC}$ | $V_{CC}$ = 4.5 V $I_{IN}$ = -18 mA | All | | | -1.2 | V |
| Input low current | $I_{IL}$ | $V_{CC}$ = 5.5 V $V_{IN}$ = 0.4 V | All | | | -400 | µA |
| Input high current | $I_{IH}$ | $V_{CC}$ = 5.5 V $V_{IN}$ = 2.7 V | All | | | 20 | µA |
| Input high current | $I_I$ | $V_{CC}$ = 5.5 V $V_{IN}$ = 5.5 V | All | | | 100 | µA |
| Off-state current | $I_{OZH}$ | $V_O$ = 2.4 V | 02 | | | 50 | µA |
| Off-state current | $I_{OZL}$ | $V_O$ = 0.4 V | 02 | | | -50 | µA |
| Output sink current | $I_{OL}$ | $V_{OL}$ = 2.0 V | All | | 45 | | mA |
| Output short-circuit current | $I_{OS}$ | $V_{CC}$ = 5.5 V, $V_O$ = 0 V 1/ | All | | -60 | -275 | mA |
| Power supply current | $I_{CC}$ | $V_{CC}$ = 5.5 V | All | | | 295 | mA |

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

| Test | Symbol | Conditions $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$, Unless otherwise specified | Parameter reference number | Device type | Group A subgroups | Limits | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Max | |
| Output disable time from low, high | $t_{PLZ}$ | See figure 4, $C_L$ = 50 pF | | 02 | 9,10,11 | | 22 | ns |
| | $t_{PHZ}$ | | | | | | 20 | ns |
| Output enable time from low, high | $t_{PZL}$ | | | 02 | 9,10,11 | | 19 | ns |
| | $t_{PZH}$ | | | | | | 21 | ns |
| $A_i$ to $Q_i$ delay | $t_{PD1}$ | | 1 | All | 9,10,11 | 3 | 20 | ns |
| RASI to $\overline{RAS}_i$ | $t_{PD2}$ | | 2 | | 9,10,11 | 3 | 18 | ns |
| CASI to $\overline{CAS}_i$ | $t_{PD3}$ | | 3 | | 9,10,11 | 3 | 17 | ns |
| MSEL to $Q_i$ | $t_{PD4}$ | | 4 | | 9,10,11 | 3 | 20 | ns |
| $MC_i$ to $Q_i$ 2/ | $t_{PD5}$ | | 5 | | 9,10,11 | 5 | 24 | ns |
| LE to $\overline{RAS}_i$ | $t_{PD6}$ | | 6 | | 9,10,11 | | 25 | ns |
| LE to $\overline{CAS}_i$ | $t_{PD7}$ | | 7 | | 9,10,11 | | 24 | ns |
| $MC_i$ to $\overline{RAS}_i$ | $t_{PD8}$ | | 8 | | 9,10,11 | 3 | 21 | ns |
| $MC_i$ to $\overline{CAS}_i$ 2/ | $t_{PD9}$ | | 9 | | 9,10,11 | 3 | 19 | ns |
| LE to $Q_i$ | $t_{PD10}$ | | 10 | | 9,10,11 | 5 | 25 | ns |
| RASI, CASI | $t_{PWL}$ | | 11 | | 9,10,11 | 20 | | ns |
| RASI, CASI | $t_{PWH}$ | | 12 | | 9,10,11 | 20 | | ns |

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

| Test | Symbol | Conditions $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$, Unless otherwise specified | Parameter reference number | Device type | Group A subgroups | Limits | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Max | |
| $A_i$ to LE | $t_{S1}$ | See figure 4, $C_L$ = 50 pF | 13 | All | 9,10,11 | 5 | | ns |
| $A_i$ to LE 2/ | $t_{H1}$ | | 14 | | 9,10,11 | 5 | | ns |
| $\overline{CS}$ to $Q_i$ | $t_{PD11}$ | | 15 | | 9,10,11 | | 23 | ns |
| $\overline{CS}$ to $\overline{RAS}_i$ | $t_{PD12}$ | | 16 | | 9,10,11 | | 20 | ns |
| $\overline{CS}$ to $\overline{CAS}_i$ | $t_{PD13}$ | | 17 | | 9,10,11 | | 19 | ns |
| $SEL_i$ to $\overline{RAS}_i$ | $t_{PD14}$ | | 18 | | 9,10,11 | | 20 | ns |
| $SEL_i$ to $\overline{CAS}_i$ | $t_{PD15}$ | | 19 | | 9,10,11 | | 18 | ns |
| $SEL_i$ to LE | $t_{S2}$ | | 20 | | 9,10,11 | 5 | | ns |
| $SEL_i$ to LE 2/ | $t_{H2}$ | | 21 | | 9,10,11 | 5 | | ns |
| $Q_i$ to $\overline{RAS}_i$ ($MC_i$ = 10) | $t_{SKEW1}$ | | 22 | | 9,10,11 | | 17 | ns |
| $Q_i$ to $\overline{RAS}_i$ ($MC_i$ = 00,01) | $t_{SKEW2}$ | | 23 | | 9,10,11 | | 17 | ns |
| $Q_i$ to $\overline{RAS}_i$ | $t_{SKEW3}$ | | 24 | | 9,10,11 | | 10 | ns |
| $Q_i$ to $\overline{CAS}_i$ | $t_{SKEW4}$ | | 25 | | 9,10,11 | | 17 | ns |

See footnotes at end of table.



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TABLE I. Electrical performance characteristics - Continued.

| Test | Symbol | Conditions $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$, Unless otherwise specified | Parameter reference number | Device type | Group A subgroups | Limits | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Max | |
| $MC_i$ to RASI 2/ | tH3 | See figure 4, $C_L$ = 50 pF | 26 | All | 9,10,11 | 5 | | ns |
| $\overline{CS}$ to RASI 2/ | tS3 | | 27 | | 9,10,11 | 5 | | ns |
| $SEL_i$ to $\overline{RAS}_i$ 2/ | tS4 | | 28 | | 9,10,11 | 5 | | ns |
| Output undershoot voltage 2/ | $V_{ONP}$ | | | | 9,10,11 | | -0.5 | V |
| $A_i$ to $Q_i$ delay | $t_{PD1}$ | See figure 4 3/, $C_L$ = 150 pF | 1 | | 9,10,11 | 9 | 24 | ns |
| RASI to $\overline{RAS}_i$ | $t_{PD2}$ | | 2 | | 9,10,11 | 9 | 23 | ns |
| CASI to $\overline{CAS}_i$ | $t_{PD3}$ | | 3 | | 9,10,11 | 9 | 22 | ns |
| MSEL to $Q_i$ | $t_{PD4}$ | | 4 | | 9,10,11 | 9 | 26 | ns |
| $MC_i$ to $Q_i$ 2/ | $t_{PD5}$ | | 5 | | 9,10,11 | 10 | 28 | ns |
| LE to $\overline{RAS}_i$ | $t_{PD6}$ | | 6 | | 9,10,11 | | 28 | ns |
| LE to $\overline{CAS}_i$ | $t_{PD7}$ | | 7 | | 9,10,11 | | 27 | ns |
| $MC_i$ to $\overline{RAS}_i$ | $t_{PD8}$ | | 8 | | 9,10,11 | 9 | 25 | ns |
| $MC_i$ to $\overline{CAS}_i$ 2/ | $t_{PD9}$ | | 9 | | 9,10,11 | 9 | 23 | ns |
| LE to $Q_i$ | $t_{PD10}$ | | 10 | | 9,10,11 | 10 | 27 | ns |
| RASI, CASI | $t_{PWL}$ | | 11 | | 9,10,11 | 20 | | ns |
| RASI, CASI | $t_{PWH}$ | | 12 | | 9,10,11 | 20 | | ns |

See footnotes at end of table.



☆ U.S. GOVERNMENT PRINTING OFFICE: 1989—749-033

TABLE I. Electrical performance characteristics - Continued.

| Test | Symbol | Conditions<br>$-55°C \le T_C \le +125°C$<br>$4.5\ V \le V_{CC} \le 5.5\ V$<br>Unless otherwise specified | Parameter reference number | Device type | Group A subgroups | Limits | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Max | |
| $A_i$ to LE | $t_{S1}$ | See figure 4 3/<br>$C_L$ = 150 pF | 13 | All | 9,10,11 | 5 | | ns |
| $A_i$ to LE 2/ | $t_{H1}$ | | 14 | | 9,10,11 | 5 | | ns |
| $\overline{CS}$ to $Q_i$ | $t_{PD11}$ | | 15 | | 9,10,11 | | 27 | ns |
| $\overline{CS}$ to $\overline{RAS}_i$ | $t_{PD12}$ | | 16 | | 9,10,11 | | 22 | ns |
| $\overline{CS}$ to $\overline{CAS}_i$ | $t_{PD13}$ | | 17 | | 9,10,11 | | 22 | ns |
| $SEL_i$ to $\overline{RAS}_i$ | $t_{PD14}$ | | 18 | | 9,10,11 | | 23 | ns |
| $SEL_i$ to $\overline{CAS}_i$ | $t_{PD15}$ | | 19 | | 9,10,11 | | 22 | ns |
| $SEL_i$ to LE | $t_{S2}$ | | 20 | | 9,10,11 | 5 | | ns |
| $SEL_i$ to LE 2/ | $t_{H2}$ | | 21 | | 9,10,11 | 5 | | ns |
| $Q_i$ to $\overline{RAS}_i$ ($MC_i$ = 10) | $t_{SKEW1}$ | | 22 | | 9,10,11 | | 15 | ns |
| $Q_i$ to $\overline{RAS}_i$ ($MC_i$ = 00,01) | $t_{SKEW2}$ | | 23 | | 9,10,11 | | 17 | ns |
| $Q_i$ to $\overline{RAS}_i$ | $t_{SKEW3}$ | | 24 | | 9,10,11 | | 8 | ns |
| $Q_i$ to $\overline{CAS}_i$ | $t_{SKEW4}$ | | 25 | | 9,10,11 | | 17 | ns |

See footnotes at end of table.



☆ U.S. GOVERNMENT PRINTING OFFICE: 1989—749-033

TABLE I. Electrical performance characteristics - Continued.

| Test | Symbol | Conditions<br>$-55°C \le T_C \le +125°C$<br>$4.5\ V \le V_{CC} \le 5.5\ V$<br>Unless otherwise specified | Parameter reference number | Device type | Group A subgroups | Limits | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Max | |
| $MC_i$ to RASI 2/ | $t_{H3}$ | See figure 4 3/<br>$C_L$ = 150 pF | 26 | All | 9,10,11 | 5 | | ns |
| $\overline{CS}$ to RASI 2/ | $t_{S3}$ | | 27 | | 9,10,11 | 5 | | ns |
| $SEL_i$ to $\overline{RAS}_i$ 2/ | $t_{S4}$ | | 28 | | 9,10,11 | 5 | | ns |
| Output undershoot voltage 2/ | $V_{ONP}$ | | | | 9,10,11 | | -0.5 | V |
| $A_i$ to $Q_i$ delay | $t_{PD1}$ | See figure 4<br>$C_L$ = 500 pF | 1 | | 9,10,11 | 12 | 40 | ns |
| RASI to $\overline{RAS}_i$ | $t_{PD2}$ | | 2 | | 9,10,11 | 12 | 40 | ns |
| CASI to $\overline{CAS}_i$ | $t_{PD3}$ | | 3 | | 9,10,11 | 12 | 37 | ns |
| MSEL to $Q_i$ | $t_{PD4}$ | | 4 | | 9,10,11 | 12 | 42 | ns |
| $MC_i$ to $Q_i$ 2/ | $t_{PD5}$ | | 5 | | 9,10,11 | 12 | 44 | ns |
| LE to $\overline{RAS}_i$ | $t_{PD6}$ | | 6 | | 9,10,11 | | 46 | ns |
| LE to $\overline{CAS}_i$ | $t_{PD7}$ | | 7 | | 9,10,11 | | 45 | ns |
| $MC_i$ to $\overline{RAS}_i$ | $t_{PD8}$ | | 8 | | 9,10,11 | 12 | 40 | ns |
| $MC_i$ to $\overline{CAS}_i$ 2/ | $t_{PD9}$ | | 9 | | 9,10,11 | 12 | 40 | ns |
| LE to $Q_i$ | $t_{PD10}$ | | 10 | | 9,10,11 | 12 | 46 | ns |
| RASI, CASI | $t_{PWL}$ | | 11 | | 9,10,11 | 20 | | ns |
| RASI, CASI | $t_{PWH}$ | | 12 | | 9,10,11 | 20 | | ns |

See footnotes at end of table.



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TABLE I. Electrical performance characteristics - Continued.

| Test | Symbol | Conditions $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$, Unless otherwise specified | Parameter reference number | Device type | Group A subgroups | Limits | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Max | |
| $A_i$ to LE | $t_{S1}$ | See figure 4, $C_L$ = 500 pF | 13 | All | 9,10,11 | 5 | | ns |
| $A_i$ to LE 2/ | $t_{H1}$ | | 14 | | 9,10,11 | 5 | | ns |
| $\overline{CS}$ to $Q_i$ | $t_{PD11}$ | | 15 | | 9,10,11 | | 45 | ns |
| $\overline{CS}$ to $\overline{RAS}_i$ | $t_{PD12}$ | | 16 | | 9,10,11 | | 40 | ns |
| $\overline{CS}$ to $\overline{CAS}_i$ | $t_{PD13}$ | | 17 | | 9,10,11 | | 38 | ns |
| $SEL_i$ to $\overline{RAS}_i$ | $t_{PD14}$ | | 18 | | 9,10,11 | | 42 | ns |
| $SEL_i$ to $\overline{CAS}_i$ | $t_{PD15}$ | | 19 | | 9,10,11 | | 41 | ns |
| $SEL_i$ to LE | $t_{S2}$ | | 20 | | 9,10,11 | 5 | | ns |
| $SEL_i$ to LE 2/ | $t_{H2}$ | | 21 | | 9,10,11 | 5 | | ns |
| $Q_i$ to $\overline{RAS}_i$ ($MC_i$ = 10) | $t_{SKEW1}$ | | 22 | | 9,10,11 | | 18 | ns |
| $Q_i$ to $\overline{RAS}_i$ ($MC_i$ = 00,01) | $t_{SKEW2}$ | | 23 | | 9,10,11 | | 18 | ns |
| $Q_i$ to $\overline{RAS}_i$ | $t_{SKEW3}$ | | 24 | | 9,10,11 | | 8 | ns |
| $Q_i$ to $\overline{CAS}_i$ | $t_{SKEW4}$ | | 25 | | 9,10,11 | | 20 | ns |

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

| Test | Symbol | Conditions $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$, Unless otherwise specified | Parameter reference number | Device type | Group A subgroups | Limits | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Max | |
| $MC_i$ to RASI 2/ | tH3 | See figure 4, $C_L$ = 500 pF | 26 | All | 9,10,11 | 5 | | ns |
| $\overline{CS}$ to RASI 2/ | tS3 | | 27 | | 9,10,11 | 5 | | ns |
| $SEL_i$ to RASI 2/ | tS4 | | 28 | | 9,10,11 | 5 | | ns |
| Output undershoot voltage 2/ | $V_{ONP}$ | | | | 9,10,11 | | -0.5 | V |

1/ Not more than one output should be shorted at a time. Duration of the short-circuit test should not exceed 1 second.

2/ Guaranteed if not tested to the limits specified.

3/ Production ac testing at 150 pF load is not done. Performance at 150 pF load is guaranteed by characterization data and correlation to the 50 pF and 500 pF measurements.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-ECC prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECC shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.



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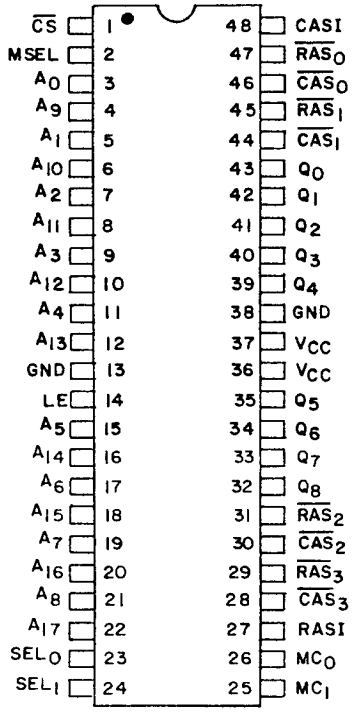
Device type 01

Case X




Device type 02

Case Y

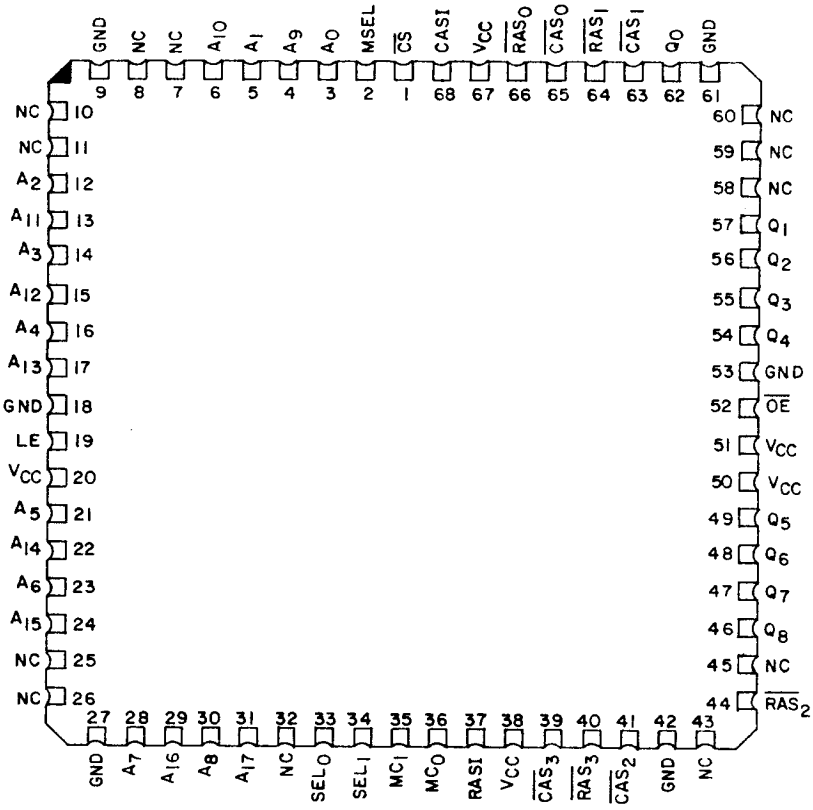



FIGURE 1. Terminal connections.

| STANDARDIZED MILITARY DRAWING<br>DEFENSE ELECTRONICS SUPPLY CENTER<br>DAYTON, OHIO 45444 | SIZE<br>A | | 5962-88696 |
|---|---|---|---|
| | | REVISION LEVEL | SHEET<br>12 |

DESC FORM 193A
SEP 87

☆ U.S. GOVERNMENT PRINTING OFFICE 1989- 749-043

Device types 01 and 02

ADDRESS OUTPUT FUNCTION TABLE

| $\overline{CS}$ | $MC_1$ | $MC_0$ | MSEL | Mode | MUX Output |
|---|---|---|---|---|---|
| 0 | 0 | 0 | X | Refresh without scrubbing | Row counter address |
| | 0 | 1 | 1 | Refresh with scrubbing | Column counter address |
| | | | 0 | | Row counter address |
| | 1 | 0 | 1 | Read/Write | Column address latch |
| | | | 0 | | Row address latch |
| | 1 | 1 | X | Clear refresh counter | Zero |
| 1 | 0 | 0 | X | Refresh without scrubbing | Row counter address |
| | 0 | 1 | 1 | Refresh with scrubbing | Column counter address |
| | | | 0 | | Row counter address |
| | 1 | 0 | X | Read/Write | Zero |
| | 1 | 1 | X | Clear refresh counter | Zero |

FIGURE 2. Truth table.

Device types 01 and 02

$\overline{RAS}$ OUTPUT FUNCTION TABLE

| RAS1 | $\overline{CS}$ | $MC_1$ | $MC_0$ | $SEL_1$ | $SEL_0$ | Mode | $\overline{RAS}_0$ | $\overline{RAS}_1$ | $\overline{RAS}_2$ | $\overline{RAS}_3$ |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | X | X | X | X | X | X | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | X | X | Refresh without scrubbing | 0 | 0 | 0 | 0 |
| | | 0 | 1 | X | X | Refresh with scrubbing | 0 | 0 | 0 | 0 |
| | | 1 | 0 | 0 | 0 | Read/Write | 0 | 1 | 1 | 1 |
| | | | | 0 | 1 | | 1 | 0 | 1 | 1 |
| | | | | 1 | 0 | | 1 | 1 | 0 | 1 |
| | | | | 1 | 1 | | 1 | 1 | 1 | 0 |
| | | 1 | 1 | X | X | Clear refresh counter | 0 | 0 | 0 | 0 |
| | 1 | 0 | 0 | X | X | Refresh without scrubbing | 0 | 0 | 0 | 0 |
| | | 0 | 1 | | | Refresh with scrubbing | 0 | 0 | 0 | 0 |
| | | 1 | 0 | | | Read/Write | 1 | 1 | 1 | 1 |
| | | 1 | 1 | | | Clear refresh counter | 0 | 0 | 0 | 0 |

FIGURE 2. Truth table - Continued.

Device types 01 and 02

$\overline{CAS}$ OUTPUT FUNCTION TABLE

| Inputs | | | | | | Internal | | Outputs | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| CASI | $\overline{CS}$ | $MC_1$ | $MC_0$ | $SEL_1$ | $SEL_0$ | $CNTR_1$ | $CNTR_0$ | $\overline{CAS}_0$ | $\overline{CAS}_1$ | $\overline{CAS}_2$ | $\overline{CAS}_3$ |
| 1 | 0 | 0 | 0 | X | X | X | X | 1 | 1 | 1 | 1 |
| | | 0 | 1 | X | X | 0 | 0 | 0 | 1 | 1 | 1 |
| | | | | | | 0 | 1 | 1 | 0 | 1 | 1 |
| | | | | | | 1 | 0 | 1 | 1 | 0 | 1 |
| | | | | | | 1 | 1 | 1 | 1 | 1 | 0 |
| | | 1 | 0 | 0 | 0 | X | X | 0 | 1 | 1 | 1 |
| | | | | 0 | 1 | | | 1 | 0 | 1 | 1 |
| | | | | 1 | 0 | | | 1 | 1 | 0 | 1 |
| | | | | 1 | 1 | | | 1 | 1 | 1 | 0 |
| | | 1 | 1 | X | X | X | X | 1 | 1 | 1 | 1 |
| | 1 | 0 | 0 | X | X | X | X | 1 | 1 | 1 | 1 |
| | | 0 | 1 | X | X | 0 | 0 | 0 | 1 | 1 | 1 |
| | | | | | | 0 | 1 | 1 | 0 | 1 | 1 |
| | | | | | | 1 | 0 | 1 | 1 | 0 | 1 |
| | | | | | | 1 | 1 | 1 | 1 | 1 | 0 |
| | | 1 | 0 | X | X | X | X | 1 | 1 | 1 | 1 |
| | | 1 | 1 | | | | | | | | |
| 0 | X | X | X | X | X | X | X | 1 | 1 | 1 | 1 |

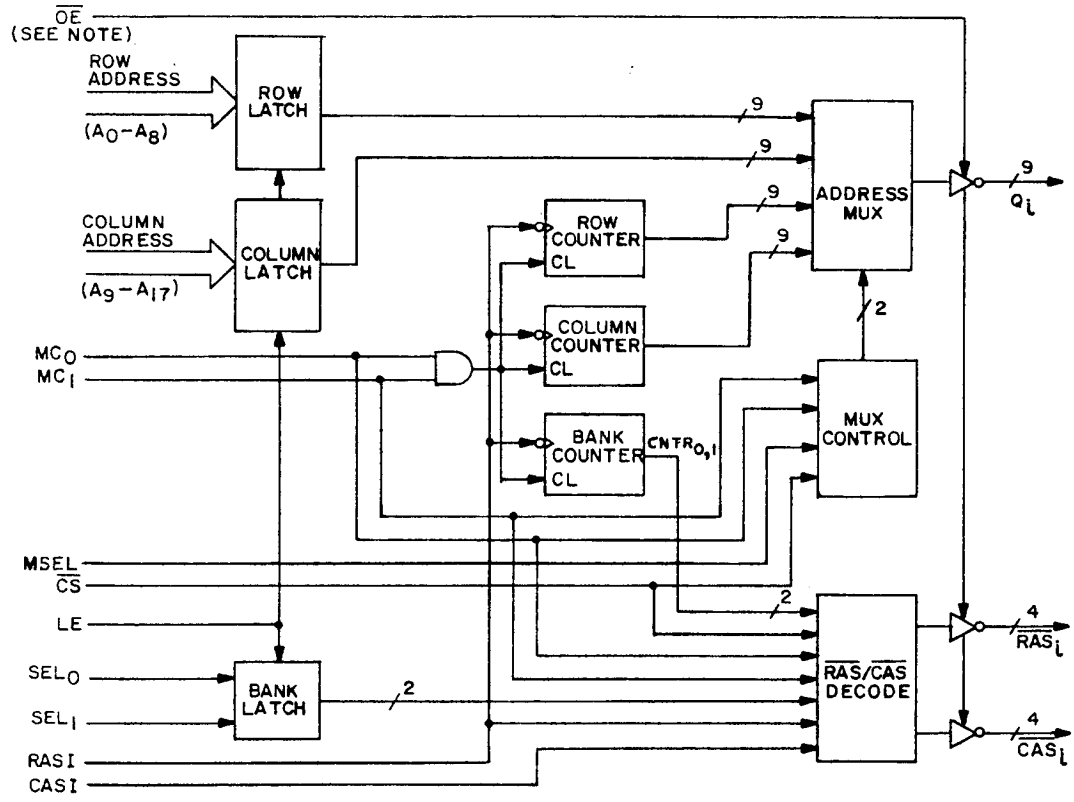
FIGURE 2. Truth table - Continued.

Device types 01 and 02

MODE CONTROL FUNCTION TABLES

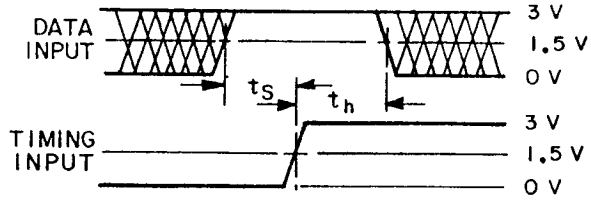
| $MC_1$ | $MC_0$ | Operating mode |
|---|---|---|
| 0 | 0 | Refresh without scrubbing. Refresh cycles are performed with only the row counter being used to generate addresses. In this mode, all four $\overline{RAS}_i$ outputs are active while the four $\overline{CAS}_i$ signals are kept HIGH. |
| 0 | 1 | Refresh with scrubbing/initialize. During this mode, refresh cycles are done with both the row and column counters generating the addresses. MSEL is used to select between the row and column counter. All four $\overline{RAS}_i$ go active in response to RASI, while only one $\overline{CAS}_i$ output goes LOW in response to CASI. The bank counter keeps track of which $\overline{CAS}_i$ output will go active. This mode is also used on system power-up so that the memory can be written with a known data pattern. |
| 1 | 0 | Read/Write. This mode is used to perform Read/Write cycles. Both the row and column addresses are latched and multiplexed to the address output lines using MSEL, $SEL_0$, and $SEL_1$, and are decoded to determine which $\overline{RAS}_i$ $\overline{CAS}_i$ will be active. |
| 1 | 1 | Clear refresh counter. This mode will clear the three refresh counters (row, column, and bank) on the high-to-low transition of RASI, putting them at the start of the refresh sequence. In this mode, all four $\overline{RAS}_i$ are driven LOW upon receipt of RASI so that DRAM wake-up cycles may be performed |

FIGURE 2. Truth tables - Continued.



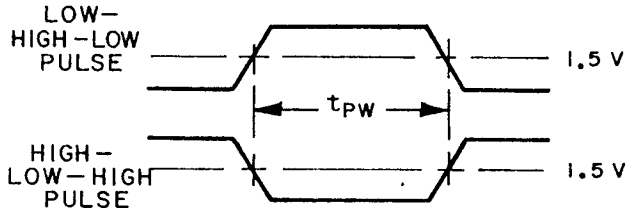

NOTE: $\overline{OE}$ applies to device type 02.

FIGURE 3. Block diagram.



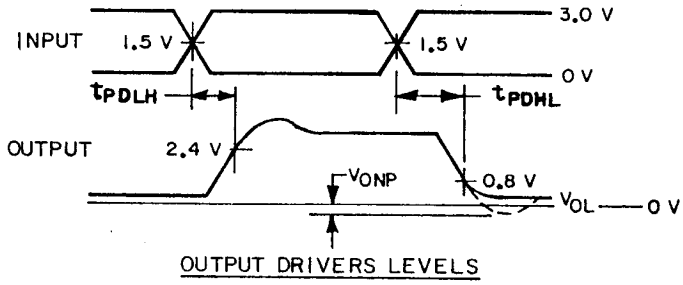

SETUP, HOLD AND RELEASE TIMES

NOTES:
1. Diagram shown for HIGH data only. Output transition may be opposite sense.
2. Cross-hatched are "don't care" condition.

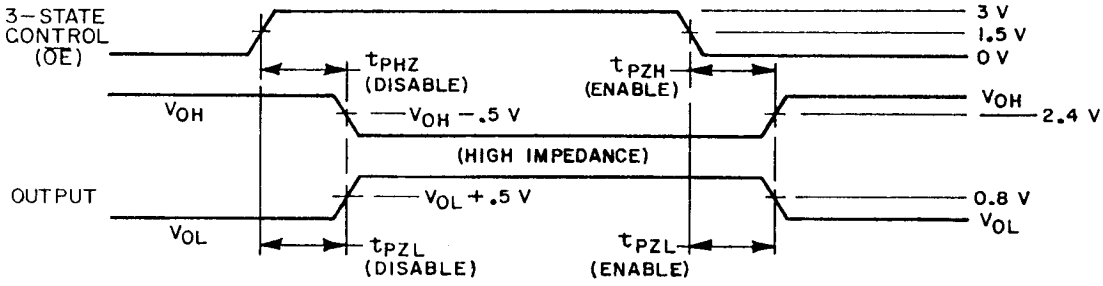



PULSE WIDTH

FIGURE 4. Switching waveforms and test circuits.



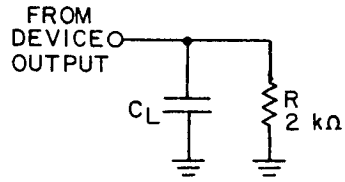

OUTPUT DRIVERS LEVELS




THREE-STATE CONTROL LEVELS
(FOR DEVICE TYPE 02 ONLY)

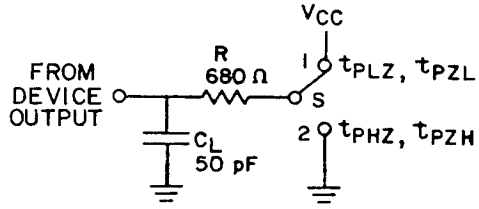
NOTE: Decoupling is needed for all ac tests.

FIGURE 4. Switching waveforms and test circuits.




NOTE: $t_{PD}$ specified at $C_L$ = 50, 150 and 500pF.

CAPACITIVE LOAD SWITCHING




THREE-STATE ENABLE/DISABLE
(FOR DEVICE TYPE 02 ONLY)

FIGURE 4. Switching waveforms and test circuits - Continued.

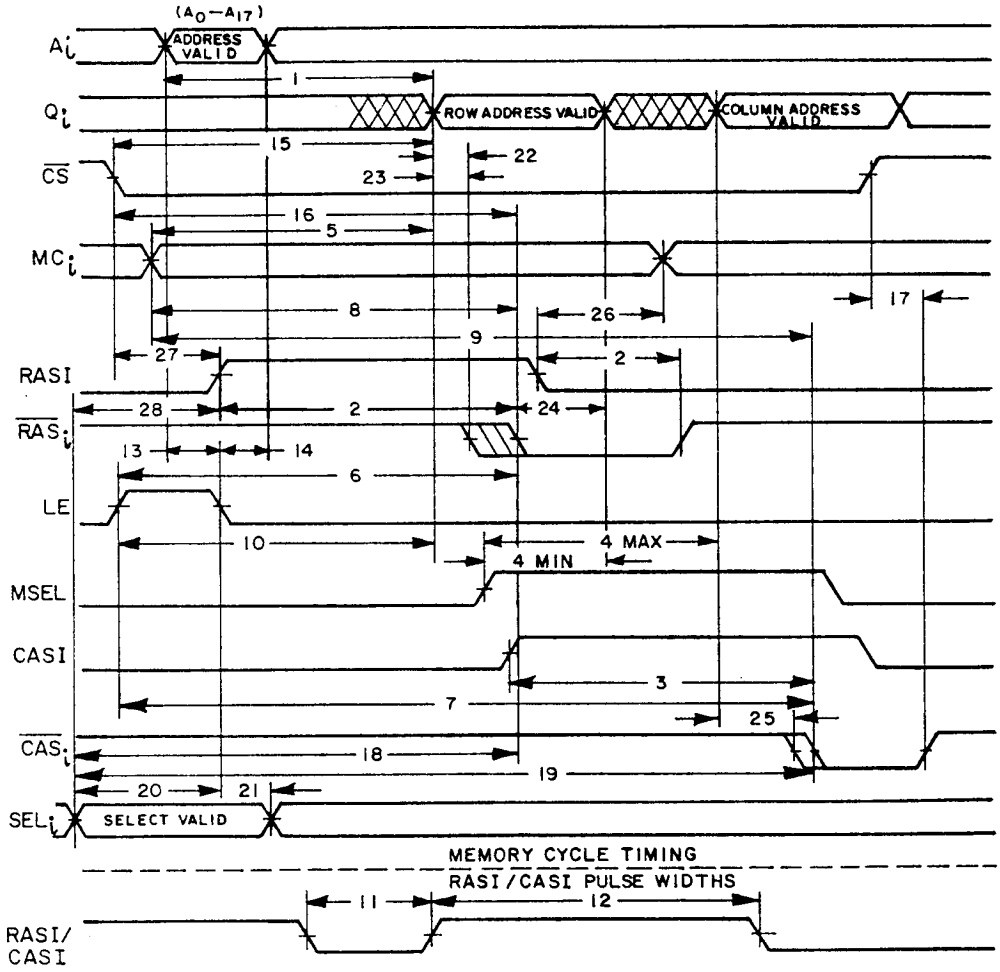



FIGURE 5. Dynamic memory controller timing.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) $T_A$ = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 7 and 8 testing shall be sufficient to verify the functional operation of the device. These tests form a part of the vendors test tape and shall be maintained and available from the approved source of supply.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) $T_A$ = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

| MIL-STD-883 test requirements | Subgroups (per method 5005, table I) |
|---|---|
| Interim electrical parameters (method 5004) | --- |
| Final electrical test parameters (method 5004) | 1*, 2, 3, 7, 8, 9, 10, 11 |
| Group A test requirements (method 5005) | 1, 2, 3, 7, 8, 9, 10, 11 |
| Groups C and D end-point electrical parameters (method 5005) | 1, 2, 3 |

* PDA applies to subgroup 1.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECC, telephone (513) 296-6022.

6.5 Comments. Comments on this drawing should be directed to DESC-ECC, Dayton, Ohio 45444, or telephone (513) 296-8525.

6.6 Pin description.

| Pin number Case X | Pin number Case Y | Name | I/O | Description |
|---|---|---|---|---|
| 3-12<br>15-22 | 3-6<br>12-17<br>21-24<br>28-31 | $A_0$-$A_{17}$ | I | $A_0$-$A_8$ are latched in as the nine-bit Row Address for the RAM. These inputs drive $Q_0$-$Q_8$ when the device is in the Read/Write mode and MSEL is low. $A_9$-$A_{17}$ are latched in as the Column Address, and will drive $Q_0$-$Q_8$ when MSEL is high and the DMC is in the Read/Write mode. The addresses are latched with the Latch Enable (LE) signal. |
| 23,24 | 33,34 | $SEL_{0-1}$ | I | These two inputs are normally the two higher-order address bits and are used in the Read/Write mode to select which bank of memory will be receiving the $\overline{RAS}_i$ and $\overline{CAS}_i$ signals after RASI and CASI go high. |
| 14 | 19 | LE | I | This active-high input causes the Row, Column, and Bank Select latches to become transparent allowing the latches to accept new input data. A low input on LE latches the input data, assuming it meets the setup and hold time requirements. |
| 2 | 2 | MSEL | I | This input determines whether the Row or Column Address will be sent to the memory address inputs. When MSEL is high the Column Address is selected, while the Row Address is selected when MSEL is low. The address may come from either the address latch or refresh address counter depending on $MC_{0-1}$. |
| 1 | 1 | $\overline{CS}$ | I | This active-low input is used to select the DMC. When $\overline{CS}$ is active, the device operates normally in all four modes. When $\overline{CS}$ goes high, the device will not enter the Read/Write mode. This allows more than one device DMC to control the same memory, thus providing an easy method for expanding the memory size. |
| | 52 | $\overline{OE}$ | I | This active-low input enables/disables the output signals. When $\overline{OE}$ is high, the outputs of the DMC enter the high-impedance state. $\overline{OE}$ is available on device 02 only. |
| 25,26 | 35,36 | $MC_{0-1}$ | I | These inputs are used to specify which of the four operating modes the DMC should be using. The description of the four operating modes is given in figure 2. |
| 32-35<br>39-43 | 46-49<br>54-57<br>62 | $Q_{0-8}$ | O | These address outputs will feed the DRAM address inputs, and provide drive for memory systems up to 500 picofarads in capacitance. |

| Pin number Case X | Pin number Case Y | Name | I/O | Description |
|---|---|---|---|---|
| 27 | 37 | RASI | I | During normal memory cycles, the decoded $\overline{RAS}_i$ output ($\overline{RAS}_0$, $\overline{RAS}_1$, $\overline{RAS}_2$, or $\overline{RAS}_3$) is forced low after receipt of RASI. In either Refresh mode, all four $\overline{RAS}_i$ outputs will go low following RASI going high. |
| 29,31 45,47 | 40,44 64,66 | $\overline{RAS}_{0-3}$ | O | Each one of the Row Address Strobe outputs provides a $\overline{RAS}_i$ signal to one of the four banks of dynamic memory. Each will go low only when selected by $SEL_0$ and $SEL_1$ and only after RASI goes high. All four go low in response to RASI in either of the Refresh modes. |
| 48 | 68 | CASI | I | This input going active will cause the selected $\overline{CAS}_i$ output to be forced low. |
| 28,30 44,46 | 39,41 63,65 | $\overline{CAS}_{0-3}$ | O | During normal Read/Write cycles the two select bits ($SEL_0$, $SEL_1$) determine which $\overline{CAS}_i$ output will go active following CASI going high. When memory scrubbing is performed, only the $\overline{CAS}_i$ signal selected by $CNTR_0$ and $CNTR_1$ will be active (see $\overline{CAS}$ Output Function Table). For nonscrubbing cycles, all four $\overline{CAS}_i$ outputs remain high. |

6.7 Approved source of supply. An approved source of supply is listed in MIL-BUL-103. Additional sources will be added to MIL-BUL-103 as they become available. The vendor listed in MIL-BUL-103 has agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECC. The approved source listed below is for information purposes only and is current only to the date of the last action of this document.

| Military drawing part number | Vendor CAGE number | Vendor similar part number 1/ |
|---|---|---|
| 5962-8869601XX | 34335 | AM2968A/BXC |
| 5962-8869602YX | 34335 | AM2968A/BUA |

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

| Vendor CAGE number | Vendor name and address |
|---|---|
| 34335 | Advanced Micro Devices, Incorporated<br>901 Thompson Place<br>P.O. Box 3453<br>Sunnyvale, CA 94088 |



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