- –55°C to 125°C Operating Temperature Range; QML Processing
- Highest Performance Floating-Point Digital Signal Processor (DSP)
  - 'C40-50:
    40-ns Instruction Cycle Time:
    50 MFLOPS, 25 MIPS, 275 MOPS,
    320 Mbytes/s
  - 'C40-40:
    50-ns Instruction Cycle Time:
    40 MFLOPS, 20 MIPS, 220 MOPS,
    256 Mbytes/s
  - 'C40-33:
    60-ns Instruction Cycle Time:
    33 MFLOPS, 16 MIPS, 181 MOPS,
    211 Mbytes/s
- Six Communications Ports
- 6-Channel Direct Memory Access (DMA) Coprocessor
- Single-Cycle Conversion to and From IEEE-745 Floating-Point Format
- Single Cycle 1/x, $1/\sqrt{x}$
- Source-Code Compatible With SMJ320C30
- Validated Ada Compiler
- Single-Cycle 40-Bit Floating-Point, 32-Bit Integer Multipliers
- 12 40-Bit Registers, 8 Auxiliary Registers, 14 Control Registers, and 2 Timers
- IEEE Standard 1149.1† Test-Access Port (JTAG)
- Two Identical External Data and Address Buses Supporting Shared Memory Systems and High Data-Rate, Single-Cycle Transfers:
  - High Port-Data Rate of 100 MBytes/s (Each Bus)
  - 16G-Byte Continuous Program/Data/Peripheral Address Space
  - Memory-Access Request for Fast, Intelligent Bus Arbitration
  - Separate Address, Data, and Control Enable Pins
  - Four Sets of Memory-Control Signals Support Different Speed Memories in Hardware
- Packaging:
  - 325-Pin Ceramic Grid Array (GF Suffix)
  - 352-Lead Ceramic Quad Flatpack (HFH Suffix)
  - 324-Pad JEDEC-Standard TAB Frame
- Fabricated Using 0.72-μm Enhanced Performance Implanted CMOS (EPIC™) Technology by Texas Instruments (TI™)
- Separate Internal Program, Data, and DMA Coprocessor Buses for Support of Massive Concurrent Input/Output (I/O) of Program and Data Throughput, Maximizing Sustained Central Processing Unit (CPU) Performance
- On-Chip Program Cache and Dual-Access/Single-Cycle RAM for Increased Memory-Access Performance
  - 512-Byte Instruction Cache
  - 8K Bytes of Single-Cycle Dual-Access Program or Data RAM
  - ROM-Based Bootloader Supports Program Bootup Using 8-, 16-, or 32-Bit Memories Over Any One of the Communications Ports

TXIS105

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

†IEEE Standard 1149.1-1990, IEEE Standard Test-Access Port and Boundary-Scan Architecture.

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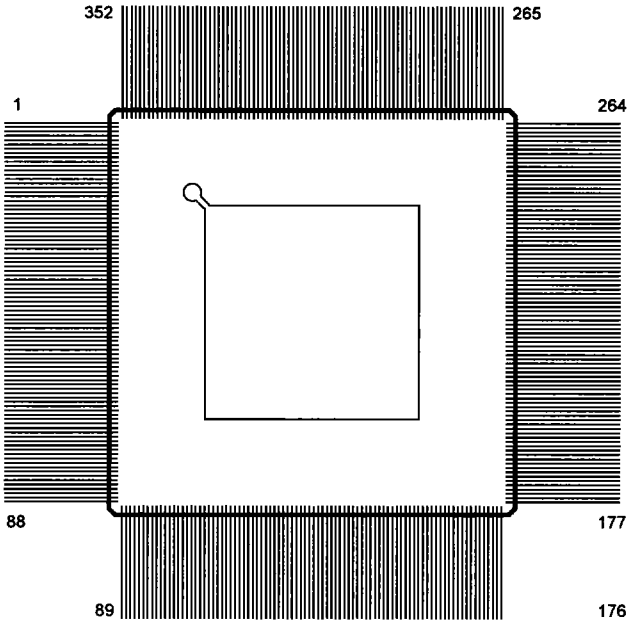
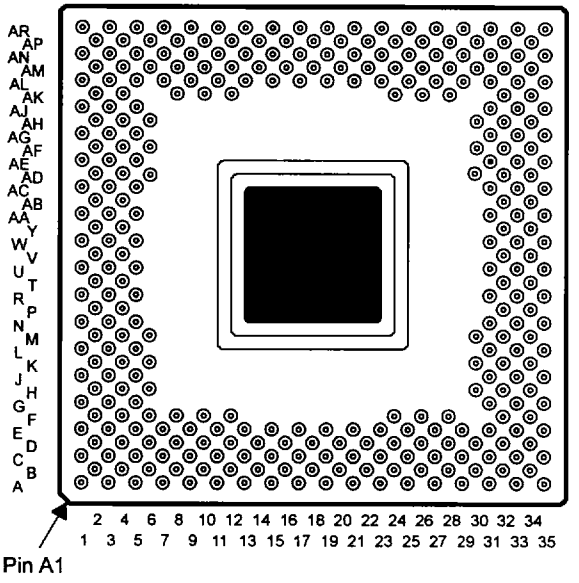
description

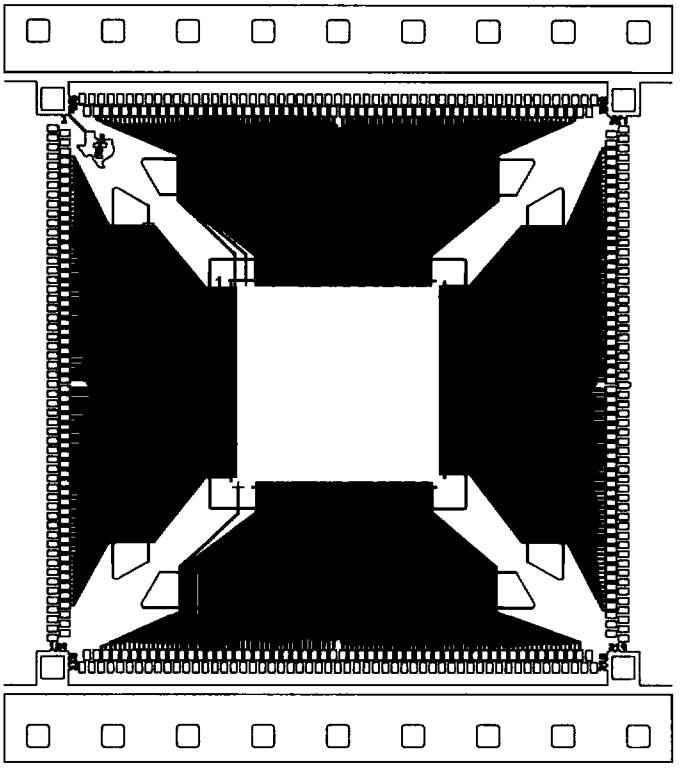
352-LEAD HFH QUAD FLATPACK PACKAGE
(TOP VIEW)†



325-PIN GF GRID ARRAY PACKAGE
(BOTTOM VIEW)†



TAB/TBB 325-LEAD OLB/ILB
TAPE AUTOMATED BONDING (TAB) PACKAGE
(TOP VIEW)†



† See Pin Assignments Table (page 13 for GF, page 17 for HFH and page 22 for the TAB) and Signal Description Table (page 10) for location and description of all pins.

description

The '320C40 digital signal processors (DSPs) are 32-bit, floating-point processors manufactured in 0.72-μm, double-level metal CMOS technology. The '320C40 is a part of the fourth generation of DSPs from Texas Instruments and is designed primarily for parallel processing.

operation

The '320C40 has six on-chip communication ports for processor-to-processor communication with no external hardware and simple communication software. This allows connectivity to other 'C4x processors with no external-glue logic. The communication ports remove input/output bottlenecks, and the independent smart DMA coprocessor is able to handle the CPU input/output burden.

central processing unit

The '320C40 CPU is configured for high-speed internal parallelism for the highest sustained performance. The key features of the CPU are:

- Eight operations/cycle:
  - 40/32-bit floating-point/integer multiply
  - 40/32-bit floating-point/integer arithmetic logic unit (ALU) operation
  - Two data accesses
  - Two address-register updates
- IEEE floating-point conversion
- Divide and square-root support
- 'C3x assembly language compatibility
- Byte and halfword accessibility

DMA coprocessor

The DMA coprocessor allows concurrent I/O and CPU processing for the highest sustained CPU performance. The key features of the DMA processor are:

- Link pointers that allow DMA channels to auto-initialize without CPU intervention
- Parallel CPU operation and DMA transfers
- Six DMA channels that support memory-to-memory data transfers
- Split-mode operation doubles the available DMA channel to 12 when data transfers to and from a communication port are required.

communication ports

The '320C40 is the first DSP with on-chip communication ports for processor-to-processor communication with no external hardware and simple communication software. The features of the communication ports are:

- Direct interprocessor communication and processor I/O
- Six communication ports for direct interprocessor communication and processor I/O
- 20M-byte/s bidirectional interface on each communication port for high-speed multiprocessor interface
- Separate input and output 8-word-deep FIFO buffers for processor-to-processor communication and I/O
- Automatic arbitration and handshaking for direct processor-to-processor connection

communication-port software reset ('C40 silicon revision ≥ 5.0)

The input and output FIFO levels for a communication port can be flushed by writing at least two back-to-back values to its communication-port software-reset address as specified in Table 1. This feature is not present in 'C40 silicon revision < 5.0. This software reset flushes any word or byte already present in the FIFOs but it does not affect the status of the communication-port pins. Figure 1 shows an example of communication-port-software reset.

Table 1. Communication-Port Software-Reset Address

COMMUNICATION PORT	SOFTWARE RESET ADDRESS
0	0x0100043
1	0x0100053
2	0x0100063
3	0x0100073
4	0x0100083
5	0x0100093

```
; ------------------------------------------------;
; RESET1:Flush's FIFO data for communication port 1;
; ------------------------------------------------;
RESET1 push   AR0           ; Save registers
       push   R0            ;
       push   RC            ;
       ldhi   010h,AR0      ; Set AR0 to base address of COM 1
       or     050h,AR0      ;
flush: rpts   1             ; Flush FIFO data with back-to-back write
       sti    R0,*+AR0(3)   ;
       rpts   10            ; Wait
       nop                  ;
       ldi    *+AR0(0),R0   ; Check for new data from other port
       and    01FE0h,R0     ;
       bnz    flush         ;
       pop    RC            ; Restore registers
       pop    R0            ;
       pop    AR0           ;
       rets                 ; Return
```

Figure 1. Example of Communication-Port-Software Reset

$\overline{\text{NMI}}$ with bus-grant feature ('C40 silicon revision ≥ 5.0)

The '320C40 devices have a software-configurable feature which allows forcing the internal-peripheral bus to ready when the $\overline{\text{NMI}}$ signal is asserted. This feature is not present in 'C40 silicon revision < 5.0. The $\overline{\text{NMI}}$ bus-grant feature is enabled when bits 19–18 of the status register (ST) are set to 10b. When enabled, a peripheral bus-grant signal is generated on the falling edge of $\overline{\text{NMI}}$. When $\overline{\text{NMI}}$ is asserted and this feature is not enabled, the CPU stalls on access to the peripheral bus if it is not ready. A stall condition occurs when writing to a full FIFO or reading an empty FIFO. This feature is useful in correcting communication-port errors when used in conjunction with the communication-port software-reset feature.

IDLE2 clock-stop power-down mode ('C40 silicon revision ≥ 5.0)

The '320C40 has a clock-stop mode or power-down mode (IDLE2) to achieve extremely low power consumption. When an IDLE2 instruction is executed, the clocks are halted with H1 being held high. To exit IDLE2, assert one of the $\overline{\text{IIOF3}}$–$\overline{\text{IIOF0}}$ pins configured as an external interrupt instead of a general-purpose I/O. A macro showing how to generate the IDLE2 opcode is given in Figure 2. During this power-down mode:

- No instructions are executed
- The CPU, peripherals, and internal memory retain their previous state.
- The external-bus outputs are idle. The address lines remain in their previous state, the data lines are in the high-impedance state, and the output-control signals are inactive.

```
; ------------------------------------------------;
; IDLE2: Macro to generate idle2 opcode           ;
; ------------------------------------------------;
IDLE2     .macro
          .word     06000001h
          .endm
```

Figure 2. Example of Software Subroutine Using IDLE2

IDLE2 is exited when one of the five external interrupts ($\overline{\text{NMI}}$ and $\overline{\text{IIOF3}}$–$\overline{\text{IIOF0}}$) is asserted low for at least four input clocks (two H1 cycles). The clocks then start after a delay of two input clocks (one H1 cycle). The clocks can start in the opposite phase; that is, H1 can be high when H3 was high before the clocks were stopped. However, the H1 and H3 clocks remain 180° out of phase with each other.

During IDLE2 operation, an external interrupt can be recognized and serviced by the CPU if it is enabled before entering IDLE2 and asserted for at least two H1 cycles. For the processor to recognize only one interrupt, the interrupt pin must be configured for edge-trigger mode or asserted less than three cycles in level-trigger mode. Any external interrupt pin can wake up the device from IDLE2, but for the CPU to recognize that interrupt, it must also be enabled. If an interrupt is recognized and executed by the CPU, the instruction following the IDLE2 instruction is not executed until after execution of a return opcode.

When the device is in emulation mode, the CPU executes an IDLE2 instruction as if it were an IDLE instruction. The clocks continue to run for correct operation of the emulator.

development tools

The 'C40 is supported by a host of parallel-processing development tools for developing and simulating code easily and for debugging parallel-processing systems. The code generation tools include:

- An ANSI C compiler optimized with a runtime support library that supports use of communication ports and DMA.
- Third party support for C, C++ and Ada compilers
- Several operating systems available for parallel-processing support, as well as DMA and communication port drivers
- An assembler and linker with support for mapping program and data to parallel processors

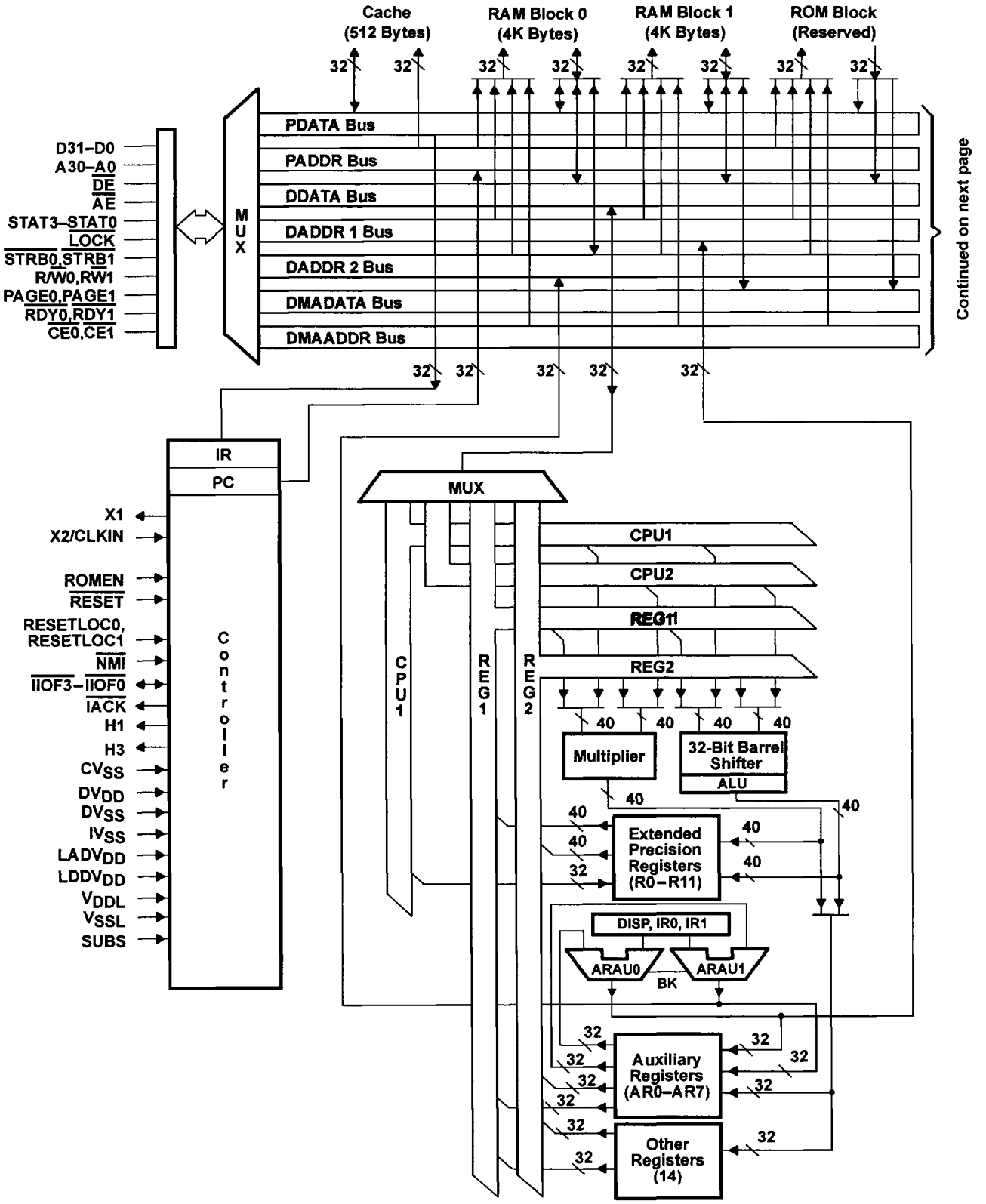
The simulation tools include:

- Parallel DSP system-level simulation with LAI hardware verification (HV) model and full function (FF) model
- TI software simulator with high-level language debugger interface for simulating a single processor

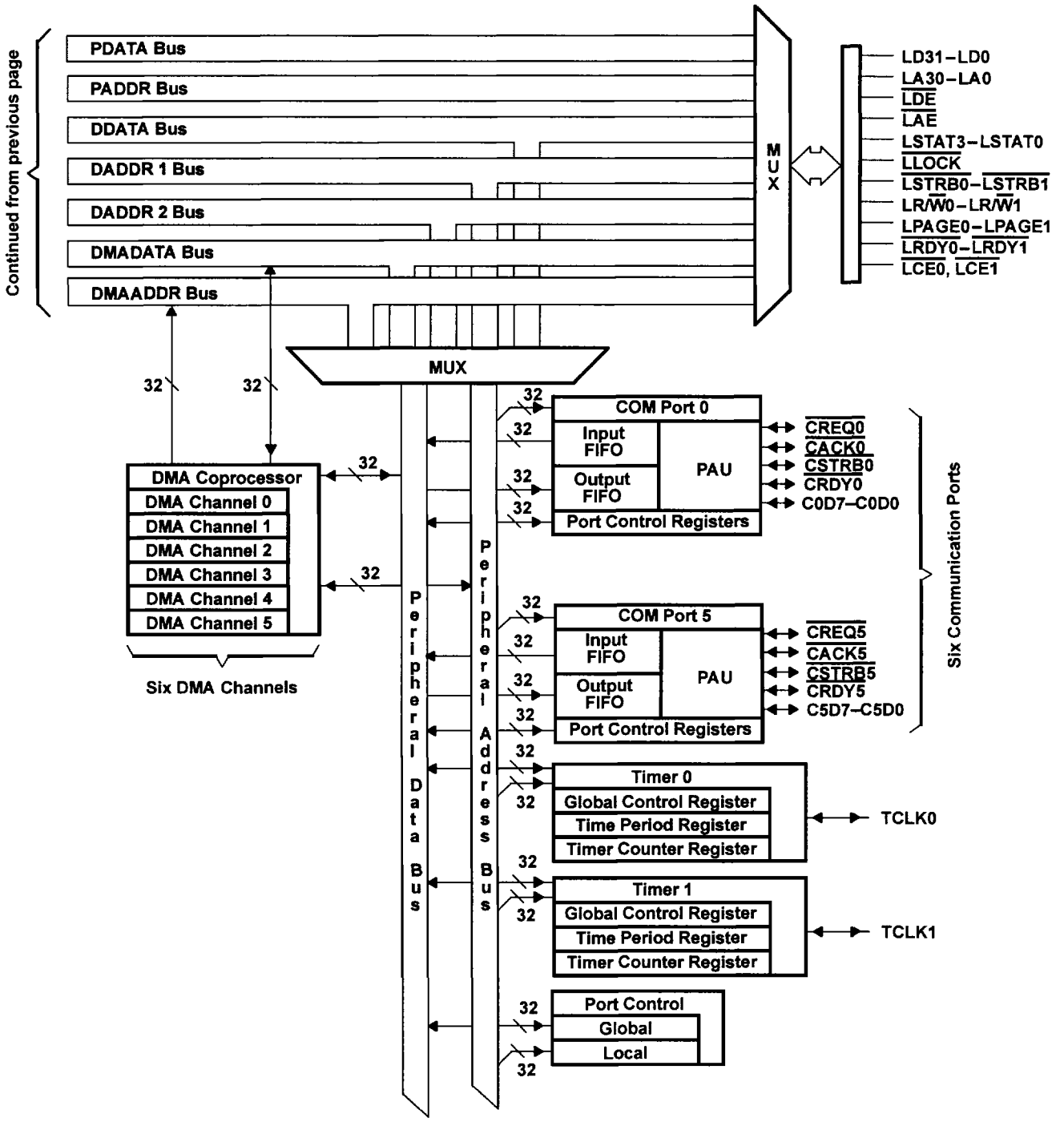
The hardware development and verification tools include:

- Parallel processor in-circuit emulator and high-level language debugger: XDS510
- Parallel processor development system (PPDS) with four '320C40s, local and global memory, and communication port connections

block diagram



block diagram (continued)



memory map

Figure 3 shows the memory map for the '320C40. Refer to the *TMS320C4x User's Guide* (literature number SPRU063) for a detailed description of this memory mapping.

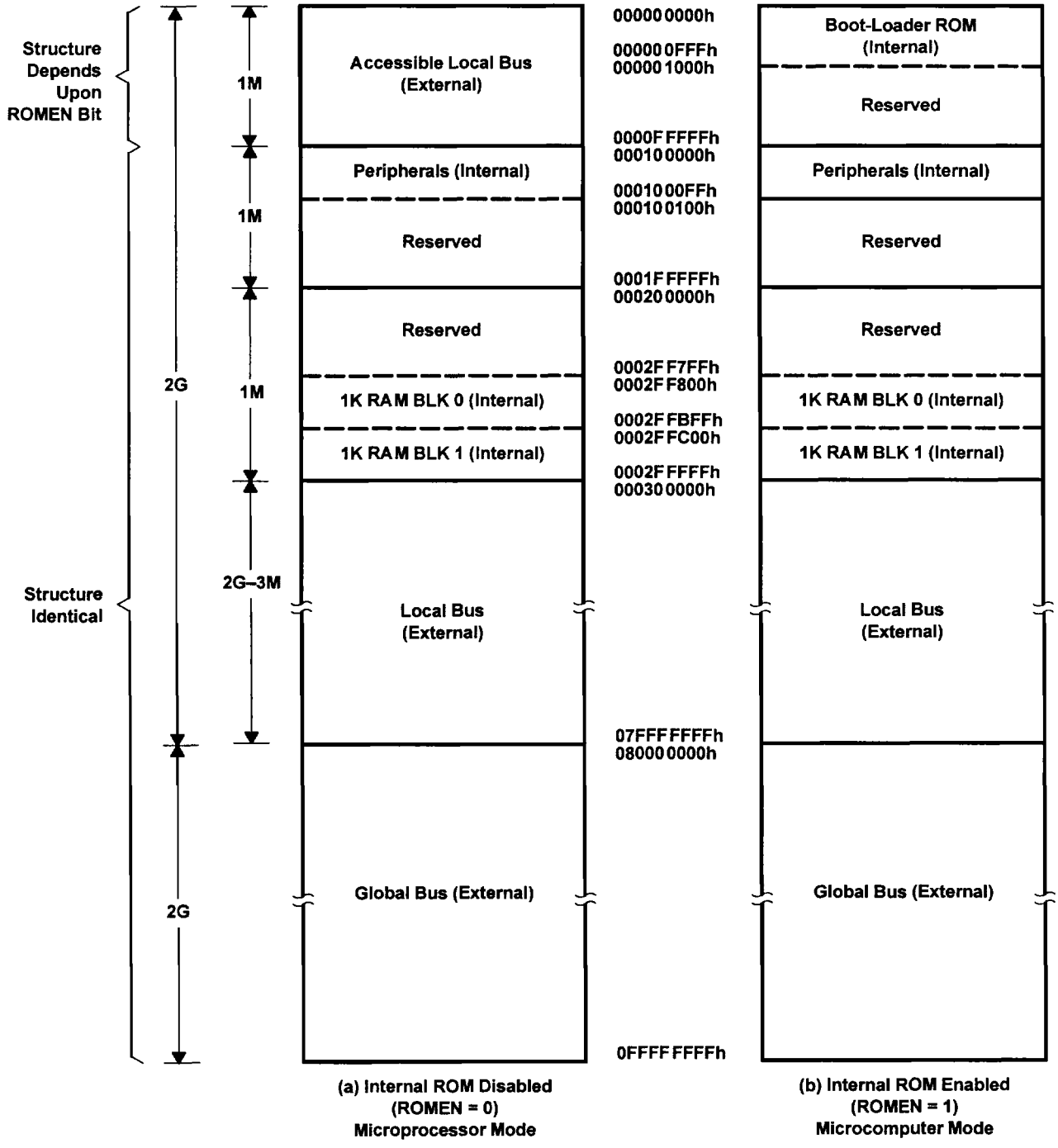


Figure 3. Memory Map for '320C40

signal descriptions

This section gives signal descriptions for the SMJ320C40 device. The SMJ320C40 signal descriptions table lists each signal, the number of pins, operating mode(s) (that is, input, output, or high-impedance state as indicated by I, O, or Z, respectively), and function. All pins labeled NC are not to be connected by the user. A line over a signal name (for example, $\overline{\text{RESET}}$) indicates that the signal is active low (true at a logic-0 level). The signals are grouped according to functions.

SMJ320C40 Signal Descriptions

SIGNAL NAME	NO. OF PINS	TYPE†	DESCRIPTION
GLOBAL BUS EXTERNAL INTERFACE (80 PINS)			
D31–D0	32	I/O/Z	32-bit data port of the global bus external interface
$\overline{\text{DE}}$	1	I	Data-bus-enable signal for the global bus external interface
A30–A0	31	O/Z	31-bit address port of the global bus external interface
$\overline{\text{AE}}$	1	I	Address-bus-enable signal for the global bus external interface
STAT3–STAT0	4	O	Status signals for the global bus external interface
$\overline{\text{LOCK}}$	1	O	Lock signal for the global bus external interface
$\overline{\text{STRB0}}$‡	1	O/Z	Access strobe 0 for the global bus external interface
R/$\overline{\text{W}}$0‡	1	O/Z	Read/write signal for $\overline{\text{STRB0}}$ accesses
PAGE0‡	1	O/Z	Page signal for $\overline{\text{STRB0}}$ accesses
$\overline{\text{RDY0}}$‡	1	I	Ready signal for $\overline{\text{STRB0}}$ accesses
$\overline{\text{CE0}}$‡	1	I	Control enable for the $\overline{\text{STRB0}}$, PAGE0, and R/$\overline{\text{W}}$0 signals
$\overline{\text{STRB1}}$‡	1	O/Z	Access strobe 1 for the global bus external interface
R/$\overline{\text{W}}$1‡	1	O/Z	Read/write signal for $\overline{\text{STRB1}}$ accesses
PAGE1‡	1	O/Z	Page signal for $\overline{\text{STRB1}}$ accesses
$\overline{\text{RDY1}}$‡	1	I	Ready signal for $\overline{\text{STRB1}}$ accesses
$\overline{\text{CE1}}$‡	1	I	Control enable for the $\overline{\text{STRB1}}$, PAGE1, and R/$\overline{\text{W}}$1 signals
LOCAL BUS EXTERNAL INTERFACE (80 PINS)			
LD31–LD0	32	I/O/Z	32-bit data port of the local bus external interface
$\overline{\text{LDE}}$	1	I	Data-bus-enable signal for the local bus external interface
LA30–LA0	31	O/Z	31-bit address port of the local bus external interface
$\overline{\text{LAE}}$	1	I	Address-bus-enable signal for the local bus external interface
LSTAT3–LSTAT0	4	O	Status signals for the local bus external interface
$\overline{\text{LLOCK}}$	1	O	Lock signal for the local bus external interface
$\overline{\text{LSTRB0}}$‡	1	O/Z	Access strobe 0 for the local bus external interface
LR/$\overline{\text{W}}$0	1	O/Z	Read/write signal for $\overline{\text{LSTRB0}}$ accesses
LPAGE0	1	O/Z	Page signal for $\overline{\text{LSTRB0}}$ accesses
$\overline{\text{LRDY0}}$	1	I	Ready signal for $\overline{\text{LSTRB0}}$ accesses
$\overline{\text{LCE0}}$	1	I	Control enable for the $\overline{\text{LSTRB0}}$, LPAGE0, and LR/$\overline{\text{W}}$0 signals
$\overline{\text{LSTRB1}}$‡	1	O/Z	Access strobe 1 for the local bus external interface
LR/$\overline{\text{W}}$1	1	O/Z	Read/write signal for $\overline{\text{LSTRB1}}$ accesses
LPAGE1	1	O/Z	Page signal for $\overline{\text{LSTRB1}}$ accesses
$\overline{\text{LRDY1}}$	1	I	Ready signal for $\overline{\text{LSTRB1}}$ accesses
$\overline{\text{LCE1}}$	1	I	Control enable for the $\overline{\text{LSTRB1}}$, LPAGE1, and LR/$\overline{\text{W}}$1 signals

† I = input, O = output, Z = high impedance

‡ $\overline{\text{STRB0}}$, $\overline{\text{STRB1}}$ and associated signals (R/$\overline{\text{W}}$1, R/$\overline{\text{W}}$0, PAGE0, PAGE1, etc.) are effective over the address ranges defined by the STRB ACTIVE bits.

SMJ320C40 Signal Descriptions (Continued)

SIGNAL NAME	NO. OF PINS	TYPE†	DESCRIPTION
COMMUNICATION PORT 0 INTERFACE (12 PINS)			
C0D7–C0D0	8	I/O	Communication port 0 data bus
$\overline{\text{CREQ0}}$	1	I/O	Communication port 0 token-request signal
$\overline{\text{CACK0}}$	1	I/O	Communication port 0 token-request-acknowledge signal
$\overline{\text{CSTRB0}}$	1	I/O	Communication port 0 data-strobe signal
$\overline{\text{CRDY0}}$	1	I/O	Communication port 0 data-ready signal
COMMUNICATION PORT 1 INTERFACE (12 PINS)			
C1D7–C1D0	8	I/O	Communication port 1 data bus
$\overline{\text{CREQ1}}$	1	I/O	Communication port 1 token-request signal
$\overline{\text{CACK1}}$	1	I/O	Communication port 1 token-request-acknowledge signal
$\overline{\text{CSTRB1}}$	1	I/O	Communication port 1 data-strobe signal
$\overline{\text{CRDY1}}$	1	I/O	Communication port 1 data-ready signal
COMMUNICATION PORT 2 INTERFACE (12 PINS)			
C2D7–C2D0	8	I/O	Communication port 2 data bus
$\overline{\text{CREQ2}}$	1	I/O	Communication port 2 token-request signal
$\overline{\text{CACK2}}$	1	I/O	Communication port 2 token-request-acknowledge signal
$\overline{\text{CSTRB2}}$	1	I/O	Communication port 2 data-strobe signal
$\overline{\text{CRDY2}}$	1	I/O	Communication port 2 data-ready signal
COMMUNICATION PORT 3 INTERFACE (12 PINS)			
C3D7–C3D0	8	I/O	Communication port 3 data bus
$\overline{\text{CREQ3}}$	1	I/O	Communication port 3 token-request signal
$\overline{\text{CACK3}}$	1	I/O	Communication port 3 token-request-acknowledge signal
$\overline{\text{CSTRB3}}$	1	I/O	Communication port 3 data-strobe signal
$\overline{\text{CRDY3}}$	1	I/O	Communication port 3 data-ready signal
COMMUNICATION PORT 4 INTERFACE (12 PINS)			
C4D7–C4D0	8	I/O	Communication port 4 data bus
$\overline{\text{CREQ4}}$	1	I/O	Communication port 4 token-request signal
$\overline{\text{CACK4}}$	1	I/O	Communication port 4 token-request-acknowledge signal
$\overline{\text{CSTRB4}}$	1	I/O	Communication port 4 data-strobe signal
$\overline{\text{CRDY4}}$	1	I/O	Communication port 4 data-ready signal
COMMUNICATION PORT 5 INTERFACE (12 PINS)			
C5D7–C5D0	8	I/O	Communication port 5 data bus
$\overline{\text{CREQ5}}$	1	I/O	Communication port 5 token-request signal
$\overline{\text{CACK5}}$	1	I/O	Communication port 5 token-request-acknowledge signal
$\overline{\text{CSTRB5}}$	1	I/O	Communication port 5 data-strobe signal
$\overline{\text{CRDY5}}$	1	I/O	Communication port 5 data-ready signal

† I = input, O = output, Z = high impedance

SMJ320C40 Signal Descriptions (Continued)

SIGNAL NAME	NO. OF PINS	TYPE†	DESCRIPTION
INTERRUPTS, I/O FLAGS, RESET, TIMER (12 PINS)			
$\overline{\text{IIOF3}}$–$\overline{\text{IIOF0}}$	4	I/O	Interrupt and I/O flags
$\overline{\text{NMI}}$	1	I	Nonmaskable interrupt. $\overline{\text{NMI}}$ is sensitive to a low-going edge.
$\overline{\text{IACK}}$	1	O	Interrupt acknowledge
$\overline{\text{RESET}}$	1	I	Reset signal
RESETLOC1–RESETLOC0	2	I	Reset-vector location pins
ROMEN	1	I	On-chip ROM enable (0 = disable, 1 = enable)
TCLK0	1	I/O	Timer 0 pin
TCLK1	1	I/O	Timer 1 pin
CLOCK (4 PINS)			
X1	1	O	Crystal pin
X2/CLKIN	1	I	Crystal/oscillator pin
H1	1	O	H1 clock
H3	1	O	H3 clock
POWER AND GROUND (70 PINS)‡			
CV_{SS}	15	I	Ground pins
DV_{SS}	15	I	Ground pins
IV_{SS}	6	I	Ground pins
DV_{DD}	13	I	5-V_{DC} supply pins
$GADV_{DD}$	3	I	5-V_{DC} supply pins
$GDDV_{DD}$	3	I	5-V_{DC} supply pins
$LADV_{DD}$	3	I	5-V_{DC} supply pins
$LDDV_{DD}$	3	I	5-V_{DC} supply pins
SUBS	1	I	Substrate pin (tie to ground)
V_{DDL}	4	I	5-V_{DC} supply pins
V_{SSL}	4	I	Ground pins
EMULATION (7 PINS)			
TCK	1	I	IEEE 1149.1 test port clock
TDO	1	O/Z	IEEE 1149.1 test port data out
TDI	1	I	IEEE 1149.1 test port data in
TMS	1	I	IEEE 1149.1 test port mode select
$\overline{\text{TRST}}$	1	I	IEEE 1149.1 test port reset
EMU0	1	I/O	Emulation pin 0
EMU1	1	I/O	Emulation pin 1

† I = input, O = output, Z = high impedance

‡ HFH package has additional power and ground pins to reduce noise problems.

GF package pin assignments — alphabetical listing

NAME	NO.	NAME	NO.	NAME	NO.	NAME	NO.	NAME	NO.
A0	D32	C0D6	AN7	C5D4	AM30	CV_{SS}	E35	D31	F32
A1	B32	C0D7	AK8	C5D5	AP32	CV_{SS}	AR25	$\overline{DE}$	AA31
A2	D30	C1D0	AL7	C5D6	AM32	CV_{SS}	AE1	DV_{DD}	AR11
A3	C29	C1D1	AP8	C5D7	AL31	CV_{SS}	AR13	DV_{DD}	AR29
A4	B30	C1D2	AM8	$\overline{CACK0}$	AN11	CV_{SS}	A19	DV_{DD}	A13
A5	F28	C1D3	AK12	$\overline{CACK1}$	AN13	CV_{SS}	R35	DV_{DD}	A7
A6	F24	C1D4	AK10	$\overline{CACK2}$	AM14	CV_{SS}	AL1	DV_{DD}	A17
A7	E29	C1D5	AN9	$\overline{CACK3}$	AM16	D0	U33	DV_{DD}	L35
A8	C27	C1D6	AL9	$\overline{CACK4}$	AK32	D1	V32	DV_{DD}	AR23
A9	D28	C1D7	AP10	$\overline{CACK5}$	AJ31	D2	T34	DV_{DD}	A29
A10	B28	C2D0	AM18	$\overline{CE0}$	AA33	D3	U31	DV_{DD}	L1
A11	F26	C2D1	AN19	$\overline{CE1}$	V34	D4	R33	DV_{DD}	AC1
A12	C25	C2D2	AL19	$\overline{CRDY0}$	AP12	D5	P34	DV_{DD}	AR17
A13	E27	C2D3	AP20	$\overline{CRDY1}$	AP14	D6	T32	DV_{DD}	A23
A14	B26	C2D4	AM20	$\overline{CRDY2}$	AL15	D7	N33	DV_{DD}	AJ1
A15	D26	C2D5	AN21	$\overline{CRDY3}$	AL17	D8	R31	DV_{SS}	AJ35
A16	C23	C2D6	AL21	$\overline{CRDY4}$	AH30	D9	M34	DV_{SS}	A21
A17	B24	C2D7	AP22	$\overline{CRDY5}$	AH32	D10	P32	DV_{SS}	A25
A18	E25	C3D0	AM22	$\overline{CREQ0}$	AM10	D11	L33	DV_{SS}	G35
A19	C21	C3D1	AN23	$\overline{CREQ1}$	AM12	D12	N31	DV_{SS}	A11
A20	D24	C3D2	AL23	$\overline{CREQ2}$	AN15	D13	K34	DV_{SS}	AG1
A21	B22	C3D3	AP24	$\overline{CREQ3}$	AN17	D14	M32	DV_{SS}	AM2
A22	E23	C3D4	AM24	$\overline{CREQ4}$	AN33	D15	J33	DV_{SS}	R1
A23	C19	C3D5	AN25	$\overline{CREQ5}$	AL33	D16	L31	DV_{SS}	AR21
A24	D22	C3D6	AL25	$\overline{CSTRB0}$	AL11	D17	M30	DV_{SS}	AR15
A25	B20	C3D7	AP26	$\overline{CSTRB1}$	AL13	D18	K32	DV_{SS}	A15
A26	E21	C4D0	AN27	$\overline{CSTRB2}$	AP16	D19	H34	DV_{SS}	AR27
A27	B18	C4D1	AM26	$\overline{CSTRB3}$	AP18	D20	J31	DV_{SS}	G1
A28	C17	C4D2	AK24	$\overline{CSTRB4}$	AM34	D21	G33	DV_{SS}	N35
A29	D20	C4D3	AL27	$\overline{CSTRB5}$	AK34	D22	K30	DV_{SS}	AR9
A30	B16	C4D4	AP28	CV_{SS}	AR19	D23	F34	EMU0	AA35
$\overline{AE}$	AG31	C4D5	AK26	CV_{SS}	AR7	D24	H32	EMU1	AD34
C0D0	AP4	C4D6	AN29	CV_{SS}	N1	D25	E33	$GADV_{DD}$	B2
C0D1	AL5	C4D7	AM28	CV_{SS}	AL35	D26	D34	$GADV_{DD}$	AR1
C0D2	AN5	C5D0	AL29	CV_{SS}	A27	D27	G31	$GADV_{DD}$	U35
C0D3	AM4	C5D1	AP30	CV_{SS}	A9	D28	C33	$GDDV_{DD}$	V2
C0D4	AP6	C5D2	AK28	CV_{SS}	E1	D29	H30	$GDDV_{DD}$	A35
C0D5	AM6	C5D3	AN31	CV_{SS}	J35	D30	E31	$GDDV_{DD}$	A1

GF package pin assignments — alphabetical listing (continued)

NAME	NO.	NAME	NO.	NAME	NO.	NAME	NO.
H1	AC3	LA25	R5	LD26	B4	STAT0	AD32
H3	AC5	LA26	T2	LD27	F8	STAT1	AE33
$\overline{\text{IACK}}$	W3	LA27	U3	LD28	D6	STAT2	AF34
$\overline{\text{IIOF0}}$	AN3	LA28	T4	LD29	C3	STAT3	AE31
$\overline{\text{IIOF1}}$	AL3	LA29	V4	LD30	E5	$\overline{\text{STRB0}}$	AD30
$\overline{\text{IIOF2}}$	AH6	LA30	U5	LD31	F6	$\overline{\text{STRB1}}$	AC33
$\overline{\text{IIOF3}}$	AK2	LADV_{DD}	B34	LDDV_{DD}	AR35	SUBS	C31
IV_{SS}	AR5	LADV_{DD}	AB2	LDDV_{DD}	AP2	TCK	Y34
IV_{SS}	AR31	LADV_{DD}	AP34	LDDV_{DD}	U1	TCLK0	AE3
IV_{SS}	AG35	$\overline{\text{LAE}}$	AB4	$\overline{\text{LDE}}$	AD4	TCLK1	AD2
IV_{SS}	A31	$\overline{\text{LCE0}}$	AG5	$\overline{\text{LLOCK}}$	AA5	TDO	AB34
IV_{SS}	J1	$\overline{\text{LCE1}}$	AF2	$\overline{\text{LOCK}}$	W33	TDI	AC35
IV_{SS}	A5	LD0	E19	LPAGE0	AH2	TMS	W35
LA0	D2	LD1	C15	LPAGE1	AG3	$\overline{\text{TRST}}$	AE35
LA1	D4	LD2	D18	$\overline{\text{LRDY0}}$	AF6	V_{DDL}	AN1
LA2	E3	LD3	B14	$\overline{\text{LRDY1}}$	AE5	V_{DDL}	AN35
LA3	F4	LD4	E17	LR/$\overline{\text{W0}}$	AH4	V_{DDL}	C35
LA4	H6	LD5	D16	LR/$\overline{\text{W1}}$	AF4	V_{DDL}	C1
LA5	F2	LD6	C13	LSTAT0	AA3	V_{SSL}	A3
LA6	G5	LD7	E15	LSTAT1	Y4	V_{SSL}	AR3
LA7	G3	LD8	B12	LSTAT2	Y2	V_{SSL}	AR33
LA8	H4	LD9	D14	LSTAT3	W5	V_{SSL}	A33
LA9	H2	LD10	C11	$\overline{\text{LSTRB0}}$	AJ3	X1	W1
LA10	K6	LD11	E13	$\overline{\text{LSTRB1}}$	AD6	X2/CLKIN	AA1
LA11	M6	LD12	B10	$\overline{\text{NMI}}$	AJ5		
LA12	J5	LD13	D12	PAGE0	AG33		
LA13	J3	LD14	C9	PAGE1	AB32		
LA14	K4	LD15	E11	$\overline{\text{RDY0}}$	Y32		
LA15	K2	LD16	F12	$\overline{\text{RDY1}}$	W31		
LA16	L3	LD17	D10	RESETLOC0	AF30		
LA17	L5	LD18	B8	RESETLOC1	AH34		
LA18	M2	LD19	E9	$\overline{\text{RESET}}$	AJ33		
LA19	M4	LD20	C7	ROMEN	AK4		
LA20	N3	LD21	F10	R/$\overline{\text{W0}}$	AF32		
LA21	N5	LD22	B6	R/$\overline{\text{W1}}$	AC31		
LA22	P2	LD23	D8				
LA23	P4	LD24	C5				
LA24	R3	LD25	E7				

GF package pin assignments — numerical listing

NAME	NO.	NAME	NO.	NAME	NO.	NAME	NO.
A1	$GDDV_{DD}$	AD30	$\overline{STRB0}$	AK24	C4D2	AM30	C5D4
A3	V_{SSL}	AD32	STAT0	AK26	C4D5	AM32	C5D6
A5	IV_{SS}	AD34	EMU1	AK28	C5D2	AM34	$\overline{CSTRB4}$
A7	DV_{DD}	AE1	CV_{SS}	AK32	$\overline{CACK4}$	AN1	V_{DDL}
A9	CV_{SS}	AE3	TCLK0	AK34	$\overline{CSTRB5}$	AN3	$\overline{IIOF0}$
A11	DV_{SS}	AE5	$\overline{LRDY1}$	AL1	CV_{SS}	AN5	C0D2
A13	DV_{DD}	AE31	STAT3	AL3	$\overline{IIOF1}$	AN7	C0D6
A15	DV_{SS}	AE33	STAT1	AL5	C0D1	AN9	C1D5
A17	DV_{DD}	AE35	$\overline{TRST}$	AL7	C1D0	AN11	$\overline{CACK0}$
A19	CV_{SS}	AF2	$\overline{LCE1}$	AL9	C1D6	AN13	$\overline{CACK1}$
A21	DV_{SS}	AF4	LR/$\overline{W}$1	AL11	$\overline{CSTRB0}$	AN15	$\overline{CREQ2}$
A23	DV_{DD}	AF6	$\overline{LRDY0}$	AL13	$\overline{CSTRB1}$	AN17	$\overline{CREQ3}$
A25	DV_{SS}	AF30	RESETLOC0	AL15	$\overline{CRDY2}$	AN19	C2D1
A27	CV_{SS}	AF32	R/$\overline{W}$0	AL17	$\overline{CRDY3}$	AN21	C2D5
A29	DV_{DD}	AF34	STAT2	AL19	C2D2	AN23	C3D1
A31	IV_{SS}	AG1	DV_{SS}	AL21	C2D6	AN25	C3D5
A33	V_{SSL}	AG3	LPAGE1	AL23	C3D2	AN27	C4D0
A35	$GDDV_{DD}$	AG5	$\overline{LCE0}$	AL25	C3D6	AN29	C4D6
AA1	X2/CLKIN	AG31	$\overline{AE}$	AL27	C4D3	AN31	C5D3
AA3	LSTAT0	AG33	PAGE0	AL29	C5D0	AN33	$\overline{CREQ4}$
AA5	$\overline{LLOCK}$	AG35	IV_{SS}	AL31	C5D7	AN35	V_{DDL}
AA31	$\overline{DE}$	AH2	LPAGE0	AL33	$\overline{CREQ5}$	AP2	$LDDV_{DD}$
AA33	$\overline{CE0}$	AH4	LR/$\overline{W}$0	AL35	CV_{SS}	AP4	C0D0
AA35	EMU0	AH6	$\overline{IIOF2}$	AM2	DV_{SS}	AP6	C0D4
AB2	$LADV_{DD}$	AH30	$\overline{CRDY4}$	AM4	C0D3	AP8	C1D1
AB4	$\overline{LAE}$	AH32	$\overline{CRDY5}$	AM6	C0D5	AP10	C1D7
AB32	PAGE1	AH34	RESETLOC1	AM8	C1D2	AP12	$\overline{CRDY0}$
AB34	TDO	AJ1	DV_{DD}	AM10	$\overline{CREQ0}$	AP14	$\overline{CRDY1}$
AC1	DV_{DD}	AJ3	$\overline{LSTRB0}$	AM12	$\overline{CREQ1}$	AP16	$\overline{CSTRB2}$
AC3	H1	AJ5	$\overline{NMI}$	AM14	$\overline{CACK2}$	AP18	$\overline{CSTRB3}$
AC5	H3	AJ31	$\overline{CACK5}$	AM16	$\overline{CACK3}$	AP20	C2D3
AC31	R/$\overline{W}$1	AJ33	$\overline{RESET}$	AM18	C2D0	AP22	C2D7
AC33	$\overline{STRB1}$	AJ35	DV_{SS}	AM20	C2D4	AP24	C3D3
AC35	TDI	AK2	$\overline{IIOF3}$	AM22	C3D0	AP26	C3D7
AD2	TCLK1	AK4	ROMEN	AM24	C3D4	AP28	C4D4
AD4	$\overline{LDE}$	AK8	C0D7	AM26	C4D1	AP30	C5D1
AD6	$\overline{LSTRB1}$	AK10	C1D4	AM28	C4D7	AP32	C5D5
		AK12	C1D3			AP34	$LADV_{DD}$

GF package pin assignments — numerical listing (continued)

NAME	NO.	NAME	NO.	NAME	NO.	NAME	NO.	NAME	NO.
AR1	$GADV_{DD}$	C1	V_{DDL}	E1	CV_{SS}	H2	LA9	P2	LA22
AR3	V_{SSL}	C3	LD29	E3	LA2	H4	LA8	P4	LA23
AR5	IV_{SS}	C5	LD24	E5	LD30	H6	LA4	P32	D10
AR7	CV_{SS}	C7	LD20	E7	LD25	H30	D29	P34	D5
AR9	DV_{SS}	C9	LD14	E9	LD19	H32	D24	R1	DV_{SS}
AR11	DV_{DD}	C11	LD10	E11	LD15	H34	D19	R3	LA24
AR13	CV_{SS}	C13	LD6	E13	LD11	J1	IV_{SS}	R5	LA25
AR15	DV_{SS}	C15	LD1	E15	LD7	J3	LA13	R31	D8
AR17	DV_{DD}	C17	A28	E17	LD4	J5	LA12	R33	D4
AR19	CV_{SS}	C19	A23	E19	LD0	J31	D20	R35	CV_{SS}
AR21	DV_{SS}	C21	A19	E21	A26	J33	D15	T2	LA26
AR23	DV_{DD}	C23	A16	E23	A22	J35	CV_{SS}	T4	LA28
AR25	CV_{SS}	C25	A12	E25	A18	K2	LA15	T32	D6
AR27	DV_{SS}	C27	A8	E27	A13	K4	LA14	T34	D2
AR29	DV_{DD}	C29	A3	E29	A7	K6	LA10	U1	$LDDV_{DD}$
AR31	IV_{SS}	C31	SUBS	E31	D30	K30	D22	U3	LA27
AR33	V_{SSL}	C33	D28	E33	D25	K32	D18	U5	LA30
AR35	$LDDV_{DD}$	C35	V_{DDL}	E35	CV_{SS}	K34	D13	U31	D3
B2	$GADV_{DD}$	D2	LA0	F2	LA5	L1	DV_{DD}	U33	D0
B4	LD26	D4	LA1	F4	LA3	L3	LA16	U35	$GADV_{DD}$
B6	LD22	D6	LD28	F6	LD31	L5	LA17	V2	$GDDV_{DD}$
B8	LD18	D8	LD23	F8	LD27	L31	D16	V4	LA29
B10	LD12	D10	LD17	F10	LD21	L33	D11	V32	D1
B12	LD8	D12	LD13	F12	LD16	L35	DV_{DD}	V34	$\overline{CE1}$
B14	LD3	D14	LD9	F24	A6	M2	LA18	W1	X1
B16	A30	D16	LD5	F26	A11	M4	LA19	W3	$\overline{IACK}$
B18	A27	D18	LD2	F28	A5	M6	LA11	W5	LSTAT3
B20	A25	D20	A29	F32	D31	M30	D17	W31	$\overline{RDY1}$
B22	A21	D22	A24	F34	D23	M32	D14	W33	$\overline{LOCK}$
B24	A17	D24	A20	G1	DV_{SS}	M34	D9	W35	TMS
B26	A14	D26	A15	G3	LA7	N1	CV_{SS}	Y2	LSTAT2
B28	A10	D28	A9	G5	LA6	N3	LA20	Y4	LSTAT1
B30	A4	D30	A2	G31	D27	N5	LA21	Y32	$\overline{RDY0}$
B32	A1	D32	A0	G33	D21	N31	D12	Y34	TCK
B34	$LADV_{DD}$	D34	D26	G35	DV_{SS}	N33	D7		
						N35	DV_{SS}		

HFH package pin assignments — alphabetical listing

NAME	NO.	NAME	NO.	NAME	NO.	NAME	NO.	NAME	NO.
A0	348	C1D0	168	$\overline{\text{CACK0}}$	153	CV_{SS}†	241	$\overline{\text{DE}}$	53
A1	347	C1D1	167	$\overline{\text{CACK1}}$	149	CV_{SS}†	263	DV_{DD}‡	63
A2	346	C1D2	166	$\overline{\text{CACK2}}$	144	CV_{SS}†	282	DV_{DD}‡	77
A3	345	C1D3	165	$\overline{\text{CACK3}}$	138	CV_{SS}†	306	DV_{DD}‡	91
A4	343	C1D4	164	$\overline{\text{CACK4}}$	86	CV_{SS}†	307	DV_{DD}‡	100
A5	342	C1D5	163	$\overline{\text{CACK5}}$	82	CV_{SS}†	327	DV_{DD}‡	112
A6	341	C1D6	162	$\overline{\text{CE0}}$	51	CV_{SS}†	328	DV_{DD}‡	121
A7	340	C1D7	161	$\overline{\text{CE1}}$	42	CV_{SS}†	349	DV_{DD}‡	135
A8	339	C2D0	131	$\overline{\text{CRDY0}}$	151	D0	41	DV_{DD}‡	146
A9	338	C2D1	130	$\overline{\text{CRDY1}}$	147	D1	40	DV_{DD}‡	160
A10	337	C2D2	129	$\overline{\text{CRDY2}}$	142	D2	39	DV_{DD}‡	169
A11	336	C2D3	128	$\overline{\text{CRDY3}}$	136	D3	38	DV_{DD}‡	179
A12	335	C2D4	127	$\overline{\text{CRDY4}}$	84	D4	37	DV_{DD}‡	195
A13	334	C2D5	126	$\overline{\text{CRDY5}}$	80	D5	35	DV_{DD}‡	219
A14	333	C2D6	125	$\overline{\text{CREQ0}}$	154	D6	34	DV_{SS}§	23
A15	332	C2D7	124	$\overline{\text{CREQ1}}$	150	D7	33	DV_{SS}§	24
A16	331	C3D0	120	$\overline{\text{CREQ2}}$	145	D8	32	DV_{SS}§	44
A17	324	C3D1	119	$\overline{\text{CREQ3}}$	139	D9	31	DV_{SS}§	45
A18	323	C3D2	118	$\overline{\text{CREQ4}}$	87	D10	30	DV_{SS}§	61
A19	322	C3D3	117	$\overline{\text{CREQ5}}$	83	D11	29	DV_{SS}§	62
A20	321	C3D4	116	$\overline{\text{CSTRB0}}$	152	D12	28	DV_{SS}§	89
A21	320	C3D5	115	$\overline{\text{CSTRB1}}$	148	D13	27	DV_{SS}§	90
A22	319	C3D6	114	$\overline{\text{CSTRB2}}$	143	D14	26	DV_{SS}§	110
A23	318	C3D7	113	$\overline{\text{CSTRB3}}$	137	D15	25	DV_{SS}§	111
A24	317	C4D0	108	$\overline{\text{CSTRB4}}$	85	D16	17	DV_{SS}§	133
A25	316	C4D1	107	$\overline{\text{CSTRB5}}$	81	D17	16	DV_{SS}§	134
A26	315	C4D2	106	CV_{SS}†	18	D18	15	DV_{SS}§	157
A27	314	C4D3	105	CV_{SS}†	19	D19	14	DV_{SS}§	158
A28	312	C4D4	104	CV_{SS}†	46	D20	13	DV_{SS}§	182
A29	311	C4D5	103	CV_{SS}†	47	D21	12	DV_{SS}§	183
A30	310	C4D6	102	CV_{SS}†	88	D22	11	DV_{SS}§	220
$\overline{\text{AE}}$	75	C4D7	101	CV_{SS}†	109	D23	10	DV_{SS}§	221
C0D0	177	C5D0	99	CV_{SS}†	132	D24	9	DV_{SS}§	242
C0D1	176	C5D1	98	CV_{SS}†	155	D25	8	DV_{SS}§	243
C0D2	175	C5D2	97	CV_{SS}†	156	D26	6	DV_{SS}§	261
C0D3	174	C5D3	96	CV_{SS}†	178	D27	5	DV_{SS}§	262
C0D4	173	C5D4	95	CV_{SS}†	196	D28	4	DV_{SS}§	283
C0D5	172	C5D5	94	CV_{SS}†	217	D29	3	DV_{SS}§	284
C0D6	171	C5D6	93	CV_{SS}†	218	D30	2	DV_{SS}§	308
C0D7	170	C5D7	92	CV_{SS}†	240	D31	1	DV_{SS}§	309

† CV_{SS} and IV_{SS} pins are connected internally.
‡ DV_{DD}, $LADV_{DD}$, $LDDV_{DD}$, $GDDV_{DD}$, and $GADV_{DD}$ pins are connected internally.
§ DV_{SS} pins are connected internally.
¶ V_{DDL} pins are connected internally.
# V_{SSL} pins are connected internally.

HFH package pin assignments — alphabetical listing (continued)

NAME	NO.	NAME	NO.	NAME	NO.	NAME	NO.
DV_{SS}§	329	LA12	247	LD14	288	$\overline{RDY0}$	52
DV_{SS}§	330	LA13	246	LD15	287	$\overline{RDY1}$	43
DV_{SS}§	350	LA14	245	LD16	286	$\overline{RESET}$	79
DV_{SS}§	351	LA15	244	LD17	279	RESETLOC0	78
EMU0	59	LA16	237	LD18	278	RESETLOC1	76
EMU1	60	LA17	236	LD19	277	ROMEN	180
$GADV_{DD}$‡	313	LA18	235	LD20	276	R/$\overline{W}$0	73
$GADV_{DD}$‡	325	LA19	234	LD21	275	R/$\overline{W}$1	65
$GADV_{DD}$‡	326	LA20	233	LD22	274	STAT0	67
$GADV_{DD}$‡	344	LA21	232	LD23	273	STAT1	68
$GDDV_{DD}$‡	7	LA22	231	LD24	272	STAT2	70
$GDDV_{DD}$‡	21	LA23	230	LD25	271	STAT3	71
$GDDV_{DD}$‡	22	LA24	229	LD26	270	$\overline{STRB0}$	74
$GDDV_{DD}$‡	36	LA25	228	LD27	269	$\overline{STRB1}$	66
H1	204	LA26	227	LD28	267	SUBS	352
H3	203	LA27	225	LD29	266	TCK	54
$\overline{IACK}$	212	LA28	224	LD30	265	TCLK0	201
$\overline{IIOF0}$	181	LA29	223	LD31	264	TCLK1	202
$\overline{IIOF1}$	184	LA30	222	$LDDV_{DD}$‡	268	TDO	55
$\overline{IIOF2}$	185	$LADV_{DD}$‡	226	$LDDV_{DD}$‡	280	TDI	56
$\overline{IIOF3}$	186	$LADV_{DD}$‡	238	$LDDV_{DD}$‡	281	TMS	57
IV_{SS}†	20	$LADV_{DD}$‡	239	$LDDV_{DD}$‡	298	$\overline{TRST}$	58
IV_{SS}†	69	$LADV_{DD}$‡	256	$\overline{LDE}$	200	V_{DDL}¶	49
IV_{SS}†	122	$\overline{LAE}$	205	$\overline{LLOCK}$	207	V_{DDL}¶	140
IV_{SS}†	123	$\overline{LCE0}$	192	$\overline{LOCK}$	48	V_{DDL}¶	213
IV_{SS}†	159	$\overline{LCE1}$	199	LPAGE0	190	V_{DDL}¶	304
IV_{SS}†	206	LD0	303	LPAGE1	197	V_{SSL}#	50
IV_{SS}†	285	LD1	302	$\overline{LRDY0}$	191	V_{SSL}#	141
LA0	260	LD2	301	$\overline{LRDY1}$	198	V_{SSL}#	214
LA1	259	LD3	300	LR/$\overline{W}$0	189	V_{SSL}#	305
LA2	258	LD4	299	LR/$\overline{W}$1	194	X1	215
LA3	257	LD5	297	LSTAT0	208	X2/CLKIN	216
LA4	255	LD6	296	LSTAT1	209		
LA5	254	LD7	295	LSTAT2	210		
LA6	253	LD8	294	LSTAT3	211		
LA7	252	LD9	293	$\overline{LSTRB0}$	188		
LA8	251	LD10	292	$\overline{LSTRB1}$	193		
LA9	250	LD11	291	$\overline{NMI}$	187		
LA10	249	LD12	290	PAGE0	72		
LA11	248	LD13	289	PAGE1	64		

† CV_{SS} and IV_{SS} pins are connected internally.
‡ DV_{DD}, $LADV_{DD}$, $LDDV_{DD}$, $GDDV_{DD}$, and $GADV_{DD}$ pins are connected internally.
§ DV_{SS} pins are connected internally.
¶ V_{DDL} pins are connected internally.
# V_{SSL} pins are connected internally.

HFH package pin assignments — numerical listing

NO.	NAME	NO.	NAME	NO.	NAME	NO.	NAME	NO.	NAME
1	D31	41	D0	81	$\overline{\text{CSTRB5}}$	121	DV_{DD}‡	161	C1D7
2	D30	42	$\overline{\text{CE1}}$	82	$\overline{\text{CACK5}}$	122	IV_{SS}†	162	C1D6
3	D29	43	$\overline{\text{RDY1}}$	83	$\overline{\text{CREQ5}}$	123	IV_{SS}†	163	C1D5
4	D28	44	DV_{SS}§	84	$\overline{\text{CRDY4}}$	124	C2D7	164	C1D4
5	D27	45	DV_{SS}§	85	$\overline{\text{CSTRB4}}$	125	C2D6	165	C1D3
6	D26	46	CV_{SS}†	86	$\overline{\text{CACK4}}$	126	C2D5	166	C1D2
7	$GDDV_{DD}$‡	47	CV_{SS}†	87	$\overline{\text{CREQ4}}$	127	C2D4	167	C1D1
8	D25	48	$\overline{\text{LOCK}}$	88	CV_{SS}†	128	C2D3	168	C1D0
9	D24	49	V_{DDL}¶	89	DV_{SS}§	129	C2D2	169	DV_{DD}‡
10	D23	50	V_{SSL}#	90	DV_{SS}§	130	C2D1	170	C0D7
11	D22	51	$\overline{\text{CE0}}$	91	DV_{DD}‡	131	C2D0	171	C0D6
12	D21	52	$\overline{\text{RDY0}}$	92	C5D7	132	CV_{SS}†	172	C0D5
13	D20	53	$\overline{\text{DE}}$	93	C5D6	133	DV_{SS}§	173	C0D4
14	D19	54	TCK	94	C5D5	134	DV_{SS}§	174	C0D3
15	D18	55	TDO	95	C5D4	135	DV_{DD}‡	175	C0D2
16	D17	56	TDI	96	C5D3	136	$\overline{\text{CRDY3}}$	176	C0D1
17	D16	57	TMS	97	C5D2	137	$\overline{\text{CSTRB3}}$	177	C0D0
18	CV_{SS}†	58	$\overline{\text{TRST}}$	98	C5D1	138	$\overline{\text{CACK3}}$	178	CV_{SS}†
19	CV_{SS}†	59	EMU0	99	C5D0	139	$\overline{\text{CREQ3}}$	179	DV_{DD}‡
20	IV_{SS}†	60	EMU1	100	DV_{DD}‡	140	V_{DDL}¶	180	ROMEN
21	$GDDV_{DD}$‡	61	DV_{SS}§	101	C4D7	141	V_{SSL}#	181	$\overline{\text{IIOF0}}$
22	$GDDV_{DD}$‡	62	DV_{SS}§	102	C4D6	142	$\overline{\text{CRDY2}}$	182	DV_{SS}§
23	DV_{SS}§	63	DV_{DD}‡	103	C4D5	143	$\overline{\text{CSTRB2}}$	183	DV_{SS}§
24	DV_{SS}§	64	PAGE1	104	C4D4	144	$\overline{\text{CACK2}}$	184	$\overline{\text{IIOF1}}$
25	D15	65	R/$\overline{\text{W1}}$	105	C4D3	145	$\overline{\text{CREQ2}}$	185	$\overline{\text{IIOF2}}$
26	D14	66	$\overline{\text{STRB1}}$	106	C4D2	146	DV_{DD}‡	186	$\overline{\text{IIOF3}}$
27	D13	67	STAT0	107	C4D1	147	$\overline{\text{CRDY1}}$	187	$\overline{\text{NMI}}$
28	D12	68	STAT1	108	C4D0	148	$\overline{\text{CSTRB1}}$	188	$\overline{\text{LSTRB0}}$
29	D11	69	IV_{SS}†	109	CV_{SS}†	149	$\overline{\text{CACK1}}$	189	LR/$\overline{\text{W0}}$
30	D10	70	STAT2	110	DV_{SS}§	150	$\overline{\text{CREQ1}}$	190	LPAGE0
31	D9	71	STAT3	111	DV_{SS}§	151	$\overline{\text{CRDY0}}$	191	$\overline{\text{LRDY0}}$
32	D8	72	PAGE0	112	DV_{DD}‡	152	$\overline{\text{CSTRB0}}$	192	$\overline{\text{LCE0}}$
33	D7	73	R/$\overline{\text{W0}}$	113	C3D7	153	$\overline{\text{CACK0}}$	193	$\overline{\text{LSTRB1}}$
34	D6	74	$\overline{\text{STRB0}}$	114	C3D6	154	$\overline{\text{CREQ0}}$	194	LR/$\overline{\text{W1}}$
35	D5	75	$\overline{\text{AE}}$	115	C3D5	155	CV_{SS}†	195	DV_{DD}‡
36	$GDDV_{DD}$‡	76	RESETLOC1	116	C3D4	156	CV_{SS}†	196	CV_{SS}†
37	D4	77	DV_{DD}‡	117	C3D3	157	DV_{SS}§	197	LPAGE1
38	D3	78	RESETLOC0	118	C3D2	158	DV_{SS}§	198	$\overline{\text{LRDY1}}$
39	D2	79	$\overline{\text{RESET}}$	119	C3D1	159	IV_{SS}†	199	$\overline{\text{LCE1}}$
40	D1	80	$\overline{\text{CRDY5}}$	120	C3D0	160	DV_{DD}‡	200	$\overline{\text{LDE}}$

† CV_{SS} and IV_{SS} pins are connected internally.
‡ DV_{DD}, $LADV_{DD}$, $LDDV_{DD}$, $GDDV_{DD}$, and $GADV_{DD}$ pins are connected internally.
§ DV_{SS} pins are connected internally.
¶ V_{DDL} pins are connected internally.
# V_{SSL} pins are connected internally.

HFH package pin assignments — numerical listing (continued)

NO.	NAME	NO.	NAME	NO.	NAME	NO.	NAME
201	TCLK0	241	CV_{SS}†	281	$LDDV_{DD}$‡	321	A20
202	TCLK1	242	DV_{SS}§	282	CV_{SS}†	322	A19
203	H3	243	DV_{SS}§	283	DV_{SS}§	323	A18
204	H1	244	LA15	284	DV_{SS}§	324	A17
205	$\overline{LAE}$	245	LA14	285	IV_{SS}†	325	$GADV_{DD}$‡
206	IV_{SS}†	246	LA13	286	LD16	326	$GADV_{DD}$‡
207	$\overline{LLOCK}$	247	LA12	287	LD15	327	CV_{SS}†
208	LSTAT0	248	LA11	288	LD14	328	CV_{SS}†
209	LSTAT1	249	LA10	289	LD13	329	DV_{SS}§
210	LSTAT2	250	LA9	290	LD12	330	DV_{SS}§
211	LSTAT3	251	LA8	291	LD11	331	A16
212	$\overline{IACK}$	252	LA7	292	LD10	332	A15
213	V_{DDL}¶	253	LA6	293	LD9	333	A14
214	V_{SSL}#	254	LA5	294	LD8	334	A13
215	X1	255	LA4	295	LD7	335	A12
216	X2/CLKIN	256	$LADV_{DD}$‡	296	LD6	336	A11
217	CV_{SS}†	257	LA3	297	LD5	337	A10
218	CV_{SS}†	258	LA2	298	$LDDV_{DD}$‡	338	A9
219	DV_{DD}‡	259	LA1	299	LD4	339	A8
220	DV_{SS}§	260	LA0	300	LD3	340	A7
221	DV_{SS}§	261	DV_{SS}§	301	LD2	341	A6
222	LA30	262	DV_{SS}§	302	LD1	342	A5
223	LA29	263	CV_{SS}†	303	LD0	343	A4
224	LA28	264	LD31	304	V_{DDL}¶	344	$GADV_{DD}$‡
225	LA27	265	LD30	305	V_{SSL}#	345	A3
226	$LADV_{DD}$‡	266	LD29	306	CV_{SS}†	346	A2
227	LA26	267	LD28	307	CV_{SS}†	347	A1
228	LA25	268	$LDDV_{DD}$‡	308	DV_{SS}§	348	A0
229	LA24	269	LD27	309	DV_{SS}§	349	CV_{SS}†
230	LA23	270	LD26	310	A30	350	DV_{SS}§
231	LA22	271	LD25	311	A29	351	DV_{SS}§
232	LA21	272	LD24	312	A28	352	SUBS
233	LA20	273	LD23	313	$GADV_{DD}$‡		
234	LA19	274	LD22	314	A27		
235	LA18	275	LD21	315	A26		
236	LA17	276	LD20	316	A25		
237	LA16	277	LD19	317	A24		
238	$LADV_{DD}$‡	278	LD18	318	A23		
239	$LADV_{DD}$‡	279	LD17	319	A22		
240	CV_{SS}†	280	$LDDV_{DD}$‡	320	A21		

† CV_{SS} and IV_{SS} pins are connected internally.
‡ DV_{DD}, $LADV_{DD}$, $LDDV_{DD}$, $GDDV_{DD}$, and $GADV_{DD}$ pins are connected internally.
§ DV_{SS} pins are connected internally.
¶ V_{DDL} pins are connected internally.
# V_{SSL} pins are connected internally.

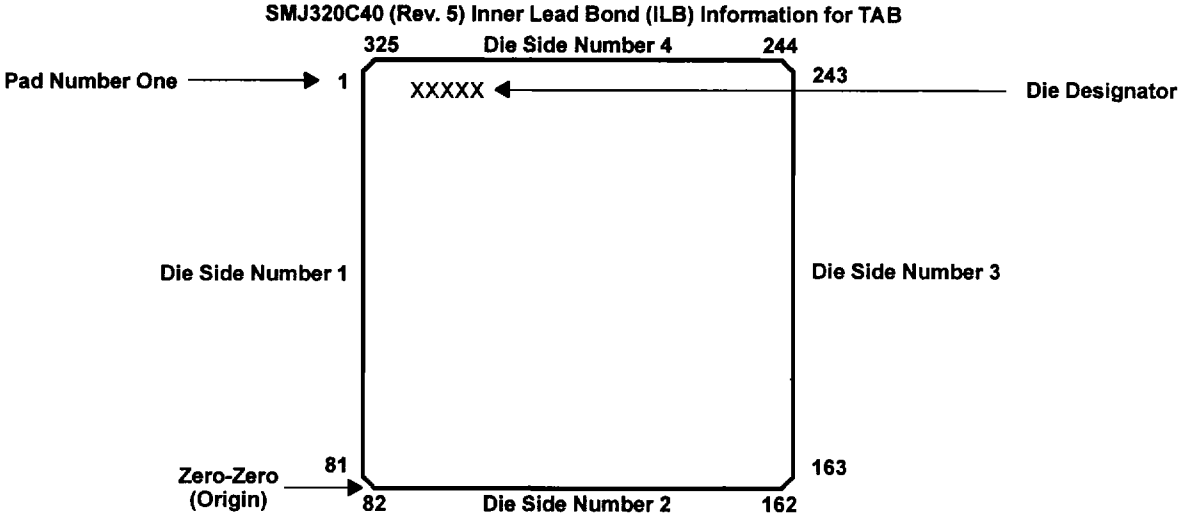


Figure 4. SMJ320C40 Die Numbering Format (Refer to Table 2)

The inner lead bond (ILB) pitch for the TAB leadframe is the same as the die bond pad pitch. Table 2 provides a reference for the following:

A. The TAB lead numbers. The TAB lead numbers are the same as the die bond pad numbers.

B. The 'C40 signal identities in relation to the pad numbers

C. There are 325 bond pad locations, 325 TAB leads, and 324 test pad locations.

D. The 'C40 X-,Y-coordinates, where bond pad 82 serves as the origin, (0,0)

E. The inner lead bond pitch (ILB) is the same as the die bond pitch.

F. The outer lead pitch is 0.25 ± 0.01 mm.

G. The test pad pitch is 0.40 ± 0.01 mm.

H. The tape width is 48 mm.

I. Outer lead bond (OLB) 18, 19 connect to test pad 18.

In addition, the following notes are significant:

J. X,Y coordinate data is in microns.

K. Average pitch is 126 µm (4.96 mils).

L. Smallest pitch value is 126 µm (4.96 mils).

M. The active silicon dimensions are 12424.86 µm × 12035.52 µm (489.16 mils × 473.83 mils).

N. The die size is approximately 12598.40 µm × 12192.00 µm (496.00 mils × 480.00 mils).

O. Distance from diced silicon to polyimide support ring is 889 µm (35.0 mils).

P. Bond pad dimensions are 108.00 µm × 108.00 µm (4.25 mils × 4.25 mils).

Q. Center of bond pad to edge of die minimum (without scribe) = 107.80 µm (4.24 mils).

R. The nominal die thickness is 381 ± 50.8 µm (15 ± 2 mils).

S. The polyimide encapsulant thickness is approximately 304.8 µm (12 mils).

Table 2. SMJ320C40 Die Pad/TAB Lead Information : Rev. 5 (0,72 μm)

DIE SIDE #1				
C40 DIE BOND PAD LOCATIONS	DIE/TAB BOND PAD IDENTITY	X-COORDINATE OF THE DIE BOND PAD	Y-COORDINATE OF THE DIE BOND PAD	PITCH OF LEAD (#, #) REFERENCES WHICH DIE BOND PADS
1	D31		11368.44	126.00 (1, 2)
2	D30		11242.44	126.00 (2, 3)
3	D29		11116.44	126.00 (3, 4)
4	D28		10990.44	126.00 (4, 5)
5	D27		10864.44	126.00 (5, 6)
6	D26		10738.44	126.00 (6, 7)
7	$GDDV_{DD}$		10612.44	126.00 (7, 8)
8	D25		10486.44	126.00 (8, 9)
9	D24		10360.44	126.00 (9, 10)
10	D23		10234.44	126.00 (10, 11)
11	D22		10108.44	126.00 (11, 12)
12	D21		9982.44	126.00 (12, 13)
13	D20		9856.44	126.00 (13, 14)
14	D19		9730.44	126.00 (14, 15)
15	D18		9604.44	126.00 (15, 16)
16	D17		9478.44	126.00 (16, 17)
17	D16		9352.44	126.00 (17, 18)
18	CV_{SS}		9226.44	126.00 (18, 19)
19	IV_{SS}		9100.44	126.00 (19, 20)
20	$GDDV_{DD}$		8974.44	126.00 (20, 21)
21	D_{VSS}		8848.44	126.00 (21, 22)
22	D15	– 429.48	8722.44	126.00 (22, 23)
23	D14		8596.44	126.00 (23, 24)
24	D13		8470.44	126.00 (24, 25)
25	D12		8344.44	126.00 (25, 26)
26	D11		8218.44	126.00 (26, 27)
27	D10		8092.44	126.00 (27, 28)
28	D9		7966.44	126.00 (28, 29)
29	D8		7840.44	126.00 (29, 30)
30	D7		7714.44	126.00 (30, 31)
31	D6		7588.44	126.00 (31, 32)
32	D5		7462.44	126.00 (32, 33)
33	$GDDV_{DD}$		7336.44	126.00 (33, 34)
34	D4		7210.44	126.00 (34, 35)
35	D3		7084.44	126.00 (35, 36)
36	D2		6958.44	126.00 (36, 37)
37	D1		6832.44	126.00 (37, 38)
38	D0		6706.44	156.42 (38, 39)
39	$\overline{CE1}$		6550.02	172.80 (39, 40)
40	$\overline{RDY1}$		6377.22	152.10 (40, 41)
41	DV_{SS}		6225.12	126.00 (41, 42)
42	CV_{SS}		6099.12	126.00 (42, 43)

Table 2. SMJ320C40 Die Pad/TAB Lead Information : Rev. 5 (0,72 μm) (Continued)

DIE SIDE #1 (CONTINUED)				
C40 DIE BOND PAD LOCATIONS	DIE/TAB BOND PAD IDENTITY	X-COORDINATE OF THE DIE BOND PAD	Y-COORDINATE OF THE DIE BOND PAD	PITCH OF LEAD (#, #) REFERENCES WHICH DIE BOND PADS
43	$\overline{\text{LOCK}}$		5973.12	126.00 (43, 44)
44	V_{DDL}		5847.12	126.00 (44, 45)
45	V_{SSL}		5721.12	156.42 (45, 46)
46	$\overline{\text{CE0}}$		5564.70	172.80 (46, 47)
47	$\overline{\text{RDY0}}$		5391.90	172.80 (47, 48)
48	$\overline{\text{DE}}$		5219.10	172.80 (48, 49)
49	TCK		5046.30	152.10 (49, 50)
50	TDO		4894.20	156.42 (50, 51)
51	TDI		4737.78	172.80 (51, 52)
52	TMS		4564.98	172.80 (52, 53)
53	$\overline{\text{TRST}}$		4392.18	151.10 (53, 54)
54	EMU0		4240.08	126.00 (54, 55)
55	EMU1		4114.08	126.00 (55, 56)
56	DV_{SS}		3988.08	126.00 (56, 57)
57	DV_{DD}		3962.08	126.00 (57, 58)
58	PAGE1		3736.08	126.00 (58, 59)
59	R/$\overline{\text{W1}}$		3610.08	126.00 (59, 60)
60	$\overline{\text{STRB1}}$		3484.08	126.00 (60, 61)
61	STAT0		3358.08	126.00 (61, 62)
62	STAT1	– 429.48	3232.08	126.00 (62, 63)
63	IV_{SS}		3106.08	126.00 (63, 64)
64	STAT2		2980.08	126.00 (64, 65)
65	STAT3		2854.08	127.44 (65, 66)
66	PAGE0		2726.64	126.00 (66, 67)
67	R/$\overline{\text{W0}}$		2600.64	126.00 (67, 68)
68	$\overline{\text{STRB0}}$		2474.64	156.42 (68, 69)
69	$\overline{\text{AE}}$		2318.22	174.24 (69, 70)
70	RESETLOC 1		2143.98	152.10 (70, 71)
71	DV_{DD}		1991.88	156.42 (71, 72)
72	RESETLOC 0		1835.46	172.80 (72, 73)
73	$\overline{\text{RESET}}$		1662.66	172.80 (73, 74)
74	$\overline{\text{CRDY5}}$		1510.56	126.00 (74, 75)
75	$\overline{\text{CSTRB5}}$		1384.56	126.00 (75, 76)
76	$\overline{\text{CACK5}}$		1258.56	126.00 (76, 77)
77	$\overline{\text{CREQ5}}$		1132.56	126.00 (77, 78)
78	$\overline{\text{CRDY4}}$		1006.56	126.00 (78, 79)
79	$\overline{\text{CSTRB4}}$		880.56	126.00 (79, 80)
80	$\overline{\text{CACK4}}$		754.56	126.00 (80, 81)
81	$\overline{\text{CREQ4}}$		628.56	

Table 2. SMJ320C40 Die Pad/TAB Lead Information : Rev. 5 (0,72 μm) (Continued)

DIE SIDE #2				
C40 DIE BOND PAD LOCATIONS	DIE/TAB BOND PAD IDENTITY	X-COORDINATE OF THE DIE BOND PAD	Y-COORDINATE OF THE DIE BOND PAD	PITCH OF LEAD (#, #) REFERENCES WHICH DIE BOND PADS
82	CV_{SS}	0.00		1062.00 (82, 83)
83	DV_{SS}	1062.00		126.00 (83, 84)
84	DV_{DD}	1188.00		126.00 (84, 85)
85	C5D7	1314.00		126.00 (85, 86)
86	C5D6	1440.00		126.00 (86, 87)
87	C5D5	1566.00		126.00 (87, 88)
88	C5D4	1692.00		126.00 (88, 89)
89	C5D3	1818.00		126.00 (89, 90)
90	C5D2	1944.00		126.00 (90, 91)
91	C5D1	2070.00		126.00 (91, 92)
92	C5D0	2196.00		126.00 (92, 93)
93	DV_{DD}	2322.00		126.00 (93, 94)
94	C4D7	2448.00		126.00 (94, 95)
95	C4D6	2574.00		126.00 (95, 96)
96	C4D5	2700.00		126.00 (96, 97)
97	C4D4	2813.40		126.00 (97, 98)
98	C4D3	2952.00		126.00 (98, 99)
99	C4D2	3078.00		126.00 (99, 100)
100	C4D1	3204.00		126.00 (100, 101)
101	C4D0	3330.00		126.00 (101, 102)
102	CV_{SS}	3456.00	0.00	126.00 (102, 103)
103	DV_{SS}	3582.00		126.00 (103, 104)
104	DV_{DD}	3708.00		126.00 (104, 105)
105	C3D7	3834.00		126.00 (105, 106)
106	C3D6	3960.00		126.00 (106, 107)
107	C3D5	4086.00		126.00 (107, 108)
108	C3D4	4212.00		126.00 (108, 109)
109	C3D3	4338.00		126.00 (109, 110)
110	C3D2	4464.00		126.00 (110, 111)
111	C3D1	4590.00		126.00 (111, 112)
112	C3D0	4716.00		126.00 (112, 113)
113	DV_{DD}	4842.00		126.00 (113, 114)
114	IV_{SS}	4968.00		126.00 (114, 115)
115	C2D7	5094.00		126.00 (115, 116)
116	C2D6	5220.00		126.00 (116, 117)
117	C2D5	5346.00		126.00 (117, 118)
118	C2D4	5472.00		126.00 (118, 119)
119	C2D3	5598.00		126.00 (119, 120)
120	C2D2	5724.00		126.00 (120, 121)
121	C2D1	5850.00		126.00 (121, 122)
122	C2D0	5976.00		126.00 (122, 123)
123	CV_{SS}	6102.00		126.00 (123, 124)

Table 2. SMJ320C40 Die Pad/TAB Lead Information : Rev. 5 (0,72 μm) (Continued)

DIE SIDE #2 (CONTINUED)				
C40 DIE BOND PAD LOCATIONS	DIE/TAB BOND PAD IDENTITY	X-COORDINATE OF THE DIE BOND PAD	Y-COORDINATE OF THE DIE BOND PAD	PITCH OF LEAD (#, #) REFERENCES WHICH DIE BOND PADS
124	DV_{SS}	6228.00		126.00 (124, 125)
125	DV_{DD}	6354.00		126.00 (125, 126)
126	$\overline{CRDY3}$	6480.00		126.00 (126, 127)
127	$\overline{CSTRB3}$	6606.00		126.00 (127, 128)
128	$\overline{CACK3}$	6732.00		126.00 (128, 129)
129	$\overline{CREQ3}$	6858.00		126.00 (129, 130)
130	V_{DDL}	6984.00		126.00 (130, 131)
131	V_{SSL}	7110.00		126.00 (131, 132)
132	$\overline{CRDY2}$	7236.00		126.00 (132, 133)
133	$\overline{CSTRB2}$	7362.00		126.00 (133, 134)
134	$\overline{CACK2}$	7488.00		126.00 (134, 135)
135	$\overline{CREQ2}$	7614.00		126.00 (135, 136)
136	DV_{DD}	7740.00		126.00 (136, 137)
137	$\overline{CRDY1}$	7866.00		126.00 (137, 138)
138	$\overline{CSTRB1}$	7992.00		126.00 (138, 139)
139	$\overline{CACK1}$	8118.00		126.00 (139, 140)
140	$\overline{CREQ1}$	8244.00		126.00 (140, 141)
141	$\overline{CRDY0}$	8370.00		126.00 (141, 142)
142	$\overline{CSTRB0}$	8496.00		126.00 (142, 143)
143	$\overline{CACK0}$	8622.00	0.00	126.00 (143, 144)
144	$\overline{CREQ0}$	8748.00		126.00 (144, 145)
145	CV_{SS}	8874.00		126.00 (145, 146)
146	DV_{SS}	9000.00		126.00 (146, 147)
147	IV_{SS}	9126.00		126.00 (147, 148)
148	DV_{DD}	9252.00		126.00 (148, 149)
149	C1D7	9378.00		126.00 (149, 150)
150	C1D6	9504.00		126.00 (150, 151)
151	C1D5	9630.00		126.00 (151, 152)
152	C1D4	9756.00		126.00 (152, 153)
153	C1D3	9882.00		126.00 (153, 154)
154	C1D2	10008.00		126.00 (154, 155)
155	C1D1	10134.00		126.00 (155, 156)
156	C1D0	10260.00		126.00 (156, 157)
157	DV_{DD}	10386.00		126.00 (157, 158)
158	C0D7	10512.00		126.00 (158, 159)
159	C0D6	10638.00		126.00 (159, 160)
160	C0D5	10764.00		126.00 (160, 161)
161	C0D4	10890.00		126.00 (161, 162)
162	C0D3	11016.00		

Table 2. SMJ320C40 Die Pad/TAB Lead Information : Rev. 5 (0,72 μm) (Continued)

DIE SIDE #3				
C40 DIE BOND PAD LOCATIONS	DIE/TAB BOND PAD IDENTITY	X-COORDINATE OF THE DIE BOND PAD	Y-COORDINATE OF THE DIE BOND PAD	PITCH OF LEAD (#, #) REFERENCES WHICH DIE BOND PADS
163	C0D2	11779.74	810.00	126.00 (163, 164)
164	C0D1		936.00	126.00 (164, 165)
165	C0D0		1062.00	126.00 (165, 166)
166	CV_{SS}		1188.00	126.00 (166, 167)
167	DV_{DD}		1314.00	156.42 (167, 168)
168	ROMEN		1470.42	152.46 (168, 169)
169	$\overline{IIOF0}$		1622.88	126.00 (169, 170)
170	DV_{SS}		1748.88	126.00 (170, 171)
171	$\overline{IIOF1}$		1874.88	126.00 (171, 172)
172	$\overline{IIOF2}$		2000.88	126.00 (172, 173)
173	$\overline{IIOF3}$		2126.88	156.42 (173, 174)
174	$\overline{NMI}$		2283.30	152.10 (174, 175)
175	$\overline{LSTRB0}$		2435.40	126.00 (175, 176)
176	LR/$\overline{W0}$		2561.40	126.00 (176, 177)
177	LPAGE0		2687.40	156.42 (177, 178)
178	$\overline{LRDY0}$		2843.82	172.80 (178, 179)
179	$\overline{LCE0}$		3016.62	152.10 (179, 180)
180	$\overline{LSTRB1}$		3168.72	126.00 (180, 181)
181	LR/$\overline{W1}$		3294.72	126.00 (181, 182)
182	DV_{DD}		3420.72	126.00 (182, 183)
183	CV_{SS}		3546.72	126.00 (183, 184)
184	LPAGE1		3672.72	156.42 (184, 185)
185	$\overline{LRDY1}$		3829.14	172.80 (185, 186)
186	$\overline{LCE1}$		4001.94	172.80 (186, 187)
187	$\overline{LDE}$		4174.74	152.10 (187, 188)
188	TCLK0		4326.84	126.00 (188, 189)
189	TCLK1		4452.84	126.00 (189, 190)
190	H3		4578.84	126.00 (190, 191)
191	H1		4704.84	156.42 (191, 192)
192	$\overline{LAE}$		4861.26	152.10 (192, 193)
193	IV_{SS}		5013.36	126.00 (193, 194)
194	$\overline{LLOCK}$		5139.36	126.00 (194, 195)
195	LSTAT0		5265.36	126.00 (195, 196)
196	LSTAT1		5391.36	126.00 (196, 197)
197	LSTAT2		5517.36	126.00 (197, 198)
198	LSTAT3		5643.36	127.44 (198, 199)
199	$\overline{IACK}$		5770.80	126.00 (199, 200)
200	V_{DDL}		5896.80	126.00 (200, 201)
201	V_{SSL}		6022.80	131.94 (201, 202)
202	X1		6154.74	171.58 (202, 203)
203	X2/CLKIN		6326.28	168.12 (203, 204)
204	CV_{SS}		6494.40	126.00 (204, 205)

Table 2. SMJ320C40 Die Pad/TAB Lead Information : Rev. 5 (0,72 μm) (Continued)

DIE SIDE #3 (CONTINUED)				
C40 DIE BOND PAD LOCATIONS	DIE/TAB BOND PAD IDENTITY	X-COORDINATE OF THE DIE BOND PAD	Y-COORDINATE OF THE DIE BOND PAD	PITCH OF LEAD (#, #) REFERENCES WHICH DIE BOND PADS
205	DV_{DD}		6620.40	126.00 (205, 206)
206	DV_{SS}		6746.40	127.44 (206, 207)
207	LA30		6873.84	126.00 (207, 208)
208	LA29		6999.84	126.00 (208, 209)
209	LA28		7125.84	126.00 (209, 210)
210	LA27		7251.84	126.00 (210, 211)
211	$LADV_{DD}$		7377.84	126.00 (211, 212)
212	LA26		7503.84	126.00 (212, 213)
213	LA25		7629.84	126.00 (213, 214)
214	LA24		7755.84	126.00 (214, 215)
215	LA23		7881.84	126.00 (215, 216)
216	LA22		8007.84	126.00 (216, 217)
217	LA21		8133.84	126.00 (217, 218)
218	LA20		8259.84	126.00 (218, 219)
219	LA19		8385.84	126.00 (219, 220)
220	LA18		8511.84	126.00 (220, 221)
221	LA17		8637.84	126.00 (221, 222)
222	LA16		8763.84	126.00 (222, 223)
223	$LADV_{DD}$		8889.84	126.00 (223, 224)
224	CV_{SS}	11779.74	9015.84	126.00 (224, 225)
225	DV_{SS}		9141.84	126.00 (225, 226)
226	LA15		9267.84	126.00 (226, 227)
227	LA14		9393.84	126.00 (227, 228)
228	LA13		9519.84	126.00 (228, 229)
229	LA12		9645.84	126.00 (229, 230)
230	LA11		9771.84	126.00 (230, 231)
231	LA10		9897.84	126.00 (231, 232)
232	LA9		10023.84	126.00 (232, 233)
233	LA8		10149.84	126.00 (233, 234)
234	LA7		10275.84	126.00 (234, 235)
235	LA6		10401.84	126.00 (235, 236)
236	LA5		10527.84	126.00 (236, 237)
237	LA4		10653.84	126.00 (237, 238)
238	$LADV_{DD}$		10779.84	126.00 (238, 239)
239	LA3		10905.84	126.00 (239, 240)
240	LA2		11031.84	126.00 (240, 241)
241	LA1		11157.84	126.00 (241, 242)
242	LA0		11283.84	205.92 (242, 243)
243	DV_{SS}		11489.76	

Table 2. SMJ320C40 Die Pad/TAB Lead Information : Rev. 5 (0,72 μm) (Continued)

DIE SIDE #4				
C40 DIE BOND PAD LOCATIONS	DIE/TAB BOND PAD IDENTITY	X-COORDINATE OF THE DIE BOND PAD	Y-COORDINATE OF THE DIE BOND PAD	PITCH OF LEAD (#, #) REFERENCES WHICH DIE BOND PADS
244	CV_{SS}	10953.72	11819.88	126.00 (244, 245)
245	LD31	10827.72		126.00 (245, 246)
246	LD30	10701.72		126.00 (246, 247)
247	LD29	10575.72		126.00 (247, 248)
248	LD28	10449.72		126.00 (248, 249)
249	$LDDV_{DD}$	10323.72		126.00 (249, 250)
250	LD27	10197.72		126.00 (250, 251)
251	LD26	10071.72		126.00 (251, 252)
252	LD25	9945.72		126.00 (252, 253)
253	LD24	9819.72		126.00 (253, 254)
254	LD23	9693.72		126.00 (254, 255)
255	LD22	9567.72		126.00 (255, 256)
256	LD21	9441.72		126.00 (256, 257)
257	LD20	9315.72		126.00 (257, 258)
258	LD19	9189.72		126.00 (258, 259)
259	LD18	9063.72		126.00 (259, 260)
260	LD17	8937.72		126.00 (260, 261)
261	$LDDV_{DD}$	8811.72		126.00 (261, 262)
262	CV_{SS}	8685.72		126.00 (262, 263)
263	DV_{SS}	8559.72		126.00 (263, 264)
264	IV_{SS}	8433.72		126.00 (264, 265)
265	LD16	8307.72		126.00 (265, 266)
266	LD15	8181.72		126.00 (266, 267)
267	LD14	8055.72		126.00 (267, 268)
268	LD13	7929.72		126.00 (268, 269)
269	LD12	7803.72		126.00 (269, 270)
270	LD11	7677.72		126.00 (270, 271)
271	LD10	7551.72		126.00 (271, 272)
272	LD9	7425.72		126.00 (272, 273)
273	LD8	7299.72		126.00 (273, 274)
274	LD7	7173.72		126.00 (274, 275)
275	LD6	7047.72		126.00 (275, 276)
276	LD5	6921.72		126.00 (276, 277)
277	$LDDV_{DD}$	6795.72		126.00 (277, 278)
278	LD4	6669.72		126.00 (278, 279)
279	LD3	6543.72		126.00 (279, 280)
280	LD2	6417.72		126.00 (280, 281)
281	LD1	6291.72		126.00 (281, 282)
282	LD0	6165.72		127.62 (282, 283)
283	V_{DDL}	6038.10		126.00 (283, 284)
284	V_{SSL}	5912.10		126.00 (284, 285)
285	CV_{SS}	5786.10		126.00 (285, 286)

Table 2. SMJ320C40 Die Pad/TAB Lead Information : Rev. 5 (0,72 μm) (Continued)

DIE SIDE #4 (CONTINUED)				
C40 DIE BOND PAD LOCATIONS	DIE/TAB BOND PAD IDENTITY	X-COORDINATE OF THE DIE BOND PAD	Y-COORDINATE OF THE DIE BOND PAD	PITCH OF LEAD (#, #) REFERENCES WHICH DIE BOND PADS
286	DV_{SS}	5660.10		126.00 (286, 287)
287	A30	5534.10		126.00 (287, 288)
288	A29	5408.10		126.00 (288, 289)
289	A28	5282.10		126.00 (289, 290)
290	$GADV_{DD}$	5156.10		126.00 (290, 291)
291	A27	5030.10		126.00 (291, 292)
292	A26	4904.10		126.00 (292, 293)
293	A25	4778.10		126.00 (293, 294)
294	A24	4652.10		126.00 (294, 295)
295	A23	4526.10		126.00 (295, 296)
296	A22	4400.10		126.00 (296, 297)
297	A21	4274.10		126.00 (297, 298)
298	A20	4148.10		126.00 (298, 299)
299	A19	4022.10		126.00 (299, 300)
300	A18	3896.10		126.00 (300, 301)
301	A17	3770.10		126.00 (301, 302)
302	$GADV_{DD}$	3644.10		126.00 (302, 303)
303	CV_{SS}	3518.10		126.00 (303, 304)
304	DV_{SS}	3392.10		126.00 (304, 305)
305	A16	3266.10		126.00 (305, 306)
306	A15	3140.10	11819.88	126.00 (306, 307)
307	A14	3014.10		126.00 (307, 308)
308	A13	2888.10		126.00 (308, 309)
309	A12	2762.10		126.00 (309, 310)
310	A11	2636.10		126.00 (310, 311)
311	A10	2510.10		126.00 (311, 312)
312	A9	2384.10		126.00 (312, 313)
313	A8	2258.10		126.00 (313, 314)
314	A7	2132.10		126.00 (314, 315)
315	A6	2006.10		126.00 (315, 316)
316	A5	1880.10		126.00 (316, 317)
317	A4	1754.10		126.00 (317, 318)
318	$GADV_{DD}$	1628.10		126.00 (318, 319)
319	A3	1502.10		126.00 (319, 320)
320	A2	1376.10		126.00 (320, 321)
321	A1	1250.10		126.00 (321, 322)
322	A0	1124.10		126.00 (322, 323)
323	CV_{SS}	998.10		558.00 (323, 324)
324	DV_{SS}	440.10		630.00 (324, 325)
325	SUBS	– 189.90		

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{DD} (see Note 1) . . . . . – 0.3 V to 7 V
Input voltage range . . . . . – 0.3 V to 7 V
Output voltage range . . . . . – 0.3 V to 7 V
Operating free-air temperature range, T_A . . . . . – 55°C to 125°C
Storage temperature range, T_{stg} . . . . . – 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions (see Note 2)

			MIN	NOM‡	MAX	UNIT
V_{DD}	Supply voltages (DV_{DD}, etc.)	SMJ320C40-33	4.5	5	5.5	V
		SMJ320C40-40	4.75	5	5.25	
		SMJ320C40-50	4.75	5	5.25	
V_{SS}	Supply voltages (CV_{SS}, etc.)			0		V
V_{IH}	High-level input voltage	X2/CLKIN	2.6		V_{DD} + 0.3§	V
		$\overline{CSTRBx}$, $\overline{CRDYx}$¶, $\overline{CREQx}$, $\overline{CACKx}$	2.2		V_{DD} + 0.3§	
		All other pins	2		V_{DD} + 0.3§	
V_{IL}	Low-level input voltage		– 0.3§		0.8	V
I_{OH}	High-level output current				– 300	µA
I_{OL}	Low-level output current				2	mA
T_A	Operating free-air temperature		–55		125	°C

‡ All nominal values are at V_{DD} = 5 V, T_A = 25°C.
§ This parameter is characterized but not tested.
¶ $\overline{CRDYx}$ is 2.6 V minimum for TAB package only.
NOTE 2: All input and output voltage levels are TTL compatible.

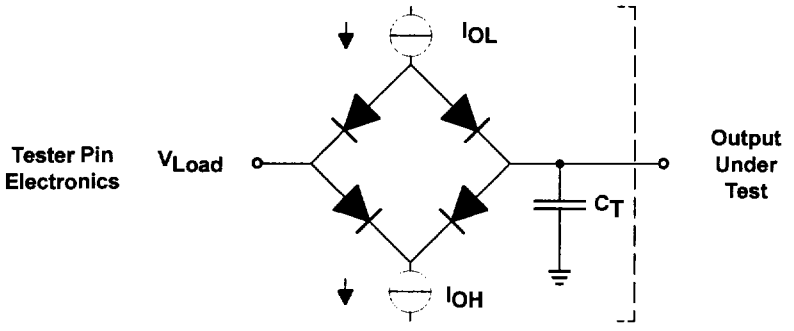
electrical characteristics over specified free-air temperature range (see Note 2)

PARAMETER		TEST CONDITIONS	MIN	TYP#	MAX	UNIT
V_{OH}	High-level output voltage	V_{DD} = MIN, I_{OH} = MAX	2.4	3		V
V_{OL}	Low-level output voltage	V_{DD} = MIN, I_{OL} = MAX		0.3	0.6	V
I_Z	Three-state current	V_{DD} = MAX	–20		20	µA
I_I	Input current	V_I = V_{SS} to V_{DD}	–10		10	µA
I_{IPU}	Input current (TDI, TCK, and TMS)	V_I = V_{SS} to V_{DD} (See Note 3)	–400		20	µA
I_{IPD}	Input current ($\overline{TRST}$)	V_I = V_{SS} to V_{DD} (See Note 3)	– 20		400	µA
I_{IC}	Input current, X2/CLKIN only	V_I = V_{SS} to V_{DD}	– 50		50	µA
I_{CC}	Supply current	V_{DD} = MAX, f_x = MAX (See Note 4), T_A = 25°C		350	850	mA
C_I	Input capacitance				15‖	pF
C_O	Output capacitance				15‖	pF

All nominal values are at V_{DD} = 5 V, T_A = 25°C.
‖ This parameter is specified by design but not tested.

NOTES: 2. All input and output voltage levels are TTL compatible.
3. Pins with internal pullup devices: TDI, TCK, TMS. Pin with internal pulldown device: $\overline{TRST}$.
4. f_x is the input clock frequency. The maximum value is 50 MHz.

PARAMETER MEASUREMENT INFORMATION



Where: I_{OL} = 2 mA (all outputs)
I_{OH} = 300 μA (all outputs)
V_{Load} = 2.15 V
C_T = 80 pF typical load circuit capacitance.

Figure 5. Test Load Circuit

signal transition levels

TTL-level outputs are driven to a minimum logic-high level of 2.4 V and to a maximum logic-low level of 0.6 V. Output transition times are specified as follows:

For a high-to-low transition on a TTL-compatible output signal, the level at which the output is said to be no longer high is 2 V, and the level at which the output is said to be low is 1 V. For a low-to-high transition, the level at which the output is said to be no longer low is 1 V, and the level at which the output is said to be high is 2 V. See Figure 6.

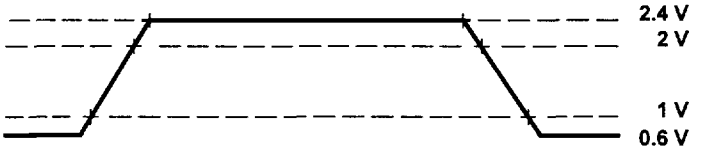
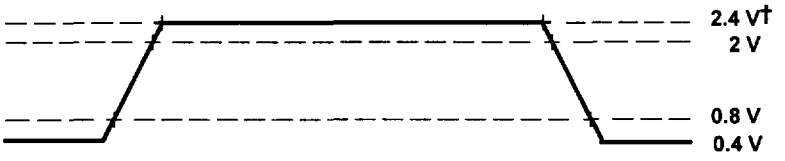


Figure 6. TTL-Level Outputs

Transition times for TTL-compatible inputs are specified as follows:

For a high-to-low transition on an input signal, the level at which the input is said to be no longer high is 2 V, and the level at which the input is said to be low is 0.8 V. For a low-to-high transition on an input signal, the level at which the input is said to be no longer low is 0.8 V, and the level at which the input is said to be high is 2 V. See Figure 7.



† Exceptions: $\frac{X2}{CLKIN}$ V_{IH} = 3.12 V and $\overline{CSTRBx}$, $\overline{CRDYx}$, $\overline{CREQx}$ and $\overline{CACKx}$ V_{IH} = 2.64 V.

Figure 7. TTL-Level Inputs

PARAMETER MEASUREMENT INFORMATION

Timing measurements, excluding TR, TF, and T disable (output going to high impedance or an I/O output becoming an input), are referenced from an input trip point of 1.5 V to an output trip point of 2 V. Timing measurements from H1 and H3 are referenced from 2 V on the rising or falling edges. TR and TF times are referenced from 20% below V_{OH} minimum to 20% above V_{OL} maximum. T disable times are referenced from an input trip point of 1.5 V to 0.1 V below V_{OH} (TPHZ) or above V_{OL} (TPLZ). The I_{OL} and I_{OH} load current can be increased to reduce the RC time constant during TPHZ and TPLZ testing.

timing parameter symbology

Timing parameter symbols used herein were created in accordance with JEDEC Standard 100-A. In order to shorten the symbols, pin names that have both global and local applications generally are represented with (L) immediately preceding the basic signal name [for example, (L)RDY represents both the global term RDY and the local term LRDY]. Other pin names and related terminology have been abbreviated as follows, unless otherwise noted:

A	(L)A30–(L)A0 or (L)Ax	H	H1/H3
AE	$\overline{\text{LAE}}$, $\overline{\text{AE}}$, or $\overline{\text{(L)AE}}$	IACK	$\overline{\text{IACK}}$
ASYNCH	asynchronous reset signals	IIOF	$\overline{\text{IIOF(3–0)}}$ or $\overline{\text{IIOFx}}$
BYTE	byte transfer	LOCK	$\overline{\text{LLOCK}}$, $\overline{\text{LOCK}}$, or $\overline{\text{(L)LOCK}}$
CA	$\overline{\text{CACK(0–5)}}$ or $\overline{\text{CACKx}}$	(L)RDY	$\overline{\text{(L)RDY0}}$, $\overline{\text{(L)RDY1}}$, or $\overline{\text{(L)RDYx}}$
CD	C(0–5)D7–C(0–5)D0 or CxDx	P	$t_{c(H)}$
CE	$\overline{\text{(L)CE0}}$, $\overline{\text{(L)CE1}}$, or $\overline{\text{(L)CEx}}$	PAGE	(L)PAGE0, (L)PAGE1, or (L)PAGEx
CI	X2/CLKIN	RESET	$\overline{\text{RESET}}$
COMM	asynchronous reset signals	RW	(L)R/$\overline{\text{W0}}$, (L)R/$\overline{\text{W1}}$, or (L)R/$\overline{\text{Wx}}$
CONTROL	control signals	S	$\overline{\text{(L)STRB0}}$, $\overline{\text{(L)STRB1}}$, or $\overline{\text{(L)STRBx}}$
CRDY	$\overline{\text{CRDY(0 – 5)}}$ or $\overline{\text{CRDYx}}$	ST	(L)STAT3–(L)STAT0 or (L)STATx
CRQ	$\overline{\text{CREQ(0–5)}}$ or $\overline{\text{CREQx}}$	TCK	TCK
CS	$\overline{\text{CSTRB(0–5)}}$ or $\overline{\text{CSTRBx}}$	TDO	TDO
D	(L)D31–(L)D0 or (L)Dx	TMS	TMS/TDI
DE	$\overline{\text{LDE}}$, $\overline{\text{DE}}$, or $\overline{\text{(L)DE}}$	WORD	word transfer

PARAMETER MEASUREMENT INFORMATION

timing parameters for X2/CLKIN, H1, H3 (see Figure 8 and Figure 9)

NO.			'320C40-33		'320C40-40		'320C40-50		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
1	$t_{f(CI)}$	Fall time, CLKIN		5†		5†		5†	ns
2	$t_{w(CIL)}$	Pulse duration, CLKIN low, $t_{c(CI)}$ = min	10		8.5		7		ns
3	$t_{w(CIH)}$	Pulse duration, CLKIN high, $t_{c(CI)}$ = min	10		8.5		7		ns
4	$t_{r(CI)}$	Rise time, CLKIN		5†		5†		5†	ns
5	$t_{c(CI)}$	Cycle time, CLKIN	30	242.5	25	242.5	20	242.5	ns
6	$t_{f(H)}$	Fall time, H1/H3		3†		3†		3†	ns
7	$t_{w(HL)}$	Pulse duration, H1/H3 low	$t_{c(CI)}-6$	$t_{c(CI)}+6$	$t_{c(CI)}-6$	$t_{c(CI)}+6$	$t_{c(CI)}-6$	$t_{c(CI)}+6$	ns
8	$t_{w(HH)}$	Pulse duration, H1/H3 high	$t_{c(CI)}-6$	$t_{c(CI)}+6$	$t_{c(CI)}-6$	$t_{c(CI)}+6$	$t_{c(CI)}-6$	$t_{c(CI)}+6$	ns
9	$t_{r(H)}$	Rise time, H1/H3		4†		4†		4†	ns
9.1	$t_{d(HL-HH)}$	Delay time, from H1 low to H3 high or from H3 low to H1 high	−1	4	−1	4	−1	4	ns
10	$t_{c(H)}$	Cycle time, H1/H3	60	485	50	485	40	485	ns

† This parameter is specified by design but not tested.

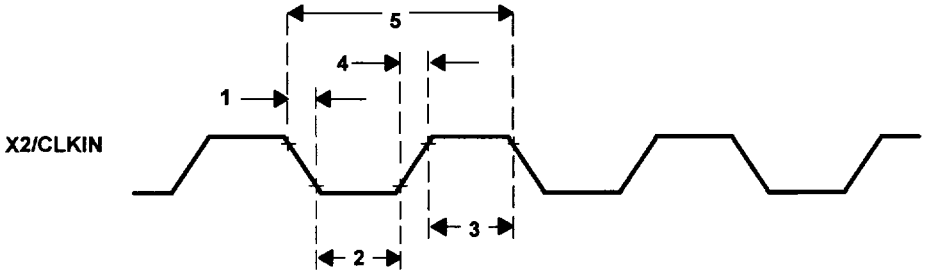


Figure 8. X2/CLKIN Timing

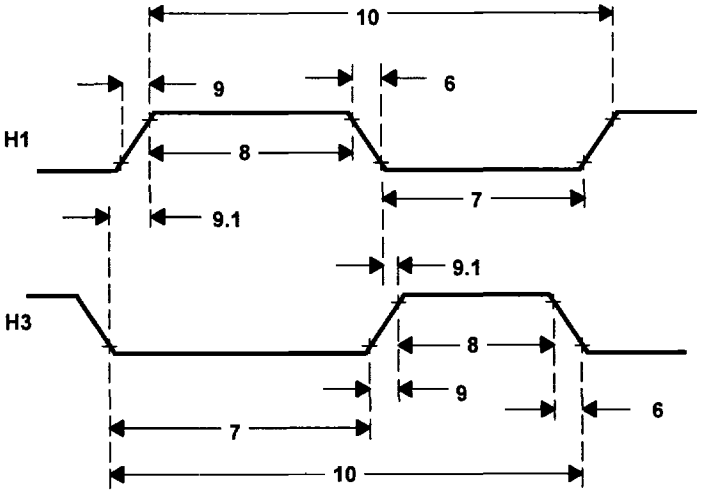


Figure 9. H1/H3 Timings

PARAMETER MEASUREMENT INFORMATION

timing parameters for a memory read/write [$\overline{\text{(L)STRBx}}$ = 0] (see Note 5, Figure 10, and Figure 11)

NO.			'320C40-33 '320C40-40		'320C40-50		UNIT
			MIN	MAX	MIN	MAX	
1	$t_{d(H1L-SL)}$	Delay time, H1 low to $\overline{\text{(L)STRBx}}$ low	0†	10	0†	10	ns
2	$t_{d(H1L-SH)}$	Delay time, H1 low to $\overline{\text{(L)STRBx}}$ high	0†	10	0†	10	ns
3	$t_{d(H1H-RWL)}$	Delay time, H1 high to (L)R/$\overline{\text{W}}$x low	0†	9	0†	9	ns
4	$t_{d(H1L-A)}$	Delay time, H1 low to (L)Ax valid	0†	10	0†	9	ns
5	$t_{su(D-H1L)R}$	Setup time, (L)Dx valid before H1 low (read)	15		15		ns
6	$t_{h(H1L-D)R}$	Hold time, (L)Dx after H1 low (read)	0		0		ns
7	$t_{su[(L)RDY-H1L]}$	Setup time, $\overline{\text{(L)RDYx}}$ valid before H1 low	25		25		ns
8	$t_{h[H1L-(L)RDY]}$	Hold time, $\overline{\text{(L)RDYx}}$ after H1 low	0		0		ns
8.1	$t_{d(H1L-ST)}$	Delay time, H1 low to (L)STAT3–(L)STAT0 valid		10		10	ns
9	$t_{d(H1H-RWH)W}$	Delay time, H1 high to (L)R/$\overline{\text{W}}$x high (write)		9		9	ns
10	$t_{v(H1L-D)W}$	Valid time, (L)Dx after H1 low (write)		16		16	ns
11	$t_{h(H1H-D)W}$	Hold time, (L)Dx after H1 high (write)	0		0		ns
12	$t_{d(H1H-A)}$	Delay time, H1 high to address valid on back-to-back write cycles		13		13	ns

† This parameter is specified by design but not tested.

NOTE 5: For consecutive reads, (L)R/$\overline{\text{W}}$x stays high and $\overline{\text{(L)STRBx}}$ stays low.

PARAMETER MEASUREMENT INFORMATION

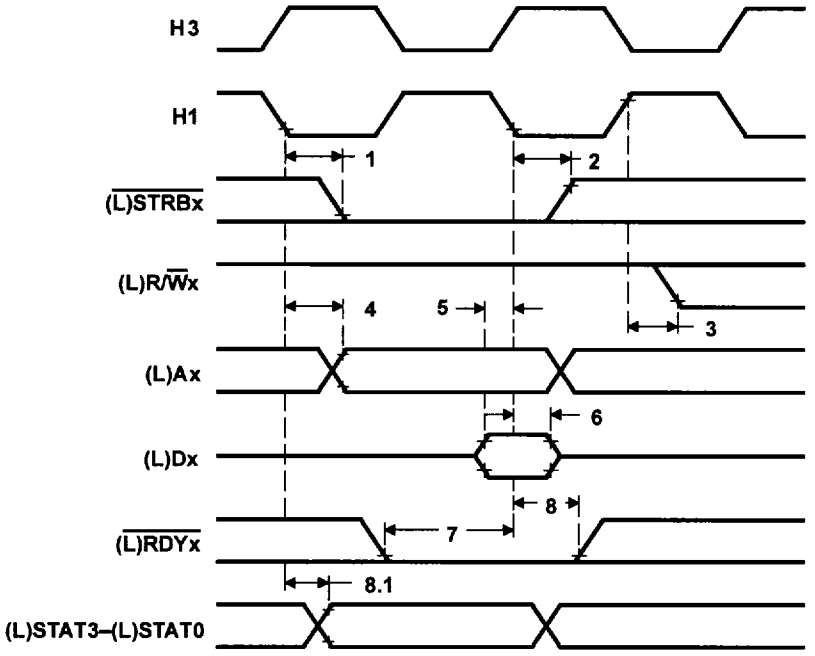


Figure 10. Memory-Read-Cycle Timing [(L)STRBx = 0]

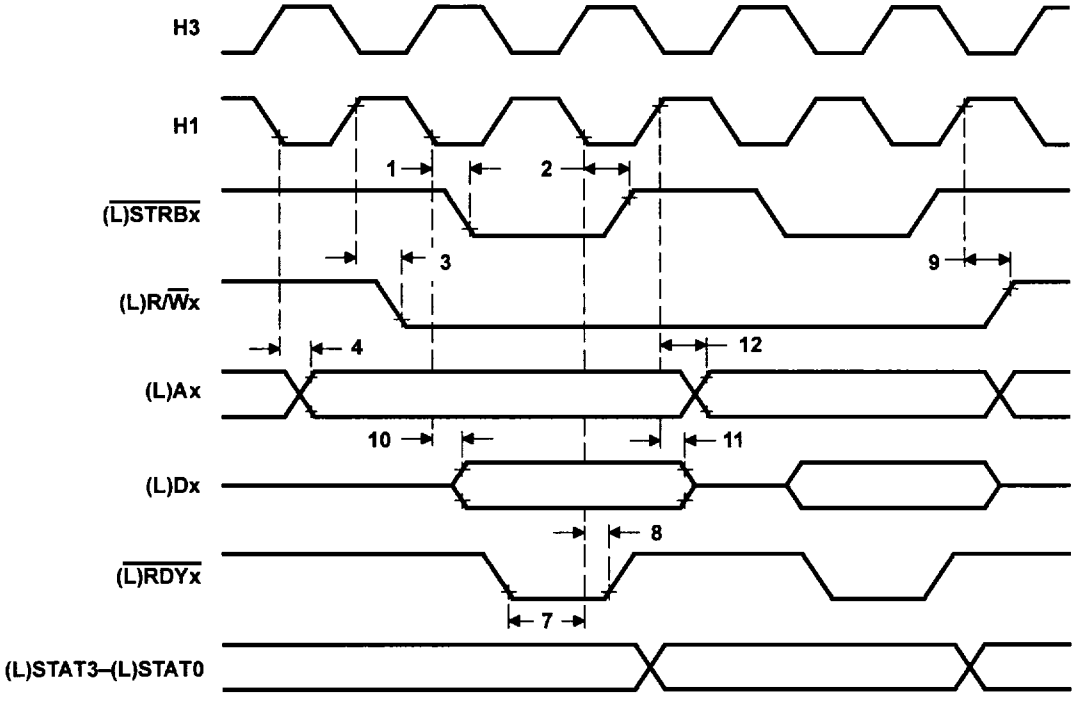


Figure 11. Memory-Write-Cycle Timing [(L)STRBx = 0]

PARAMETER MEASUREMENT INFORMATION

(L)DE, (L)AE, and (L)CEx enable timings (see Figure 12)

NO.			'320C40-33 '320C40-40 '320C40-50		UNIT
			MIN	MAX	
1	$t_{d(DEH-DZ)}$	Delay time, (L)DE high to (L)D0–(L)D31 in the high-impedance state	0†	15‡	ns
2	$t_{d(DEL-DV)}$	Delay time, (L)DE low to (L)D0–(L)D31 valid	0†	22	ns
3	$t_{d(AEH-AZ)}$	Delay time, (L)AE high to (L)A0–(L)A30 in the high-impedance state	0†	15‡	ns
4	$t_{d(AEL-AV)}$	Delay time, (L)AE low to (L)A0–(L)A30 valid	0†	21	ns
5	$t_{d(CEH-RWZ)}$	Delay time, (L)CEx high to (L)R/W0, (L)R/W1 in the high-impedance state	0†	15‡	ns
6	$t_{d(CEL-RWV)}$	Delay time, (L)CEx low to (L)R/W0, (L)R/W1 valid	0†	21	ns
7	$t_{d(CEH-SZ)}$	Delay time, (L)CEx high to (L)STRB0, (L)STRB1 in the high-impedance state	0†	15‡	ns
8	$t_{d(CEL-SV)}$	Delay time, (L)CEx low to (L)STRB0, (L)STRB1 valid	0†	21	ns
9	$t_{d(CEH-PAGEZ)}$	Delay time, (L)CEx high to (L)PAGE0, (L)PAGE1 in the high-impedance state	0†	15‡	ns
10	$t_{d(CEL-PAGEV)}$	Delay time, (L)CEx low to (L)PAGE0, (L)PAGE1 valid	0†	21	ns

† This parameter is specified by design but not tested.
‡ This parameter is characterized but not tested.

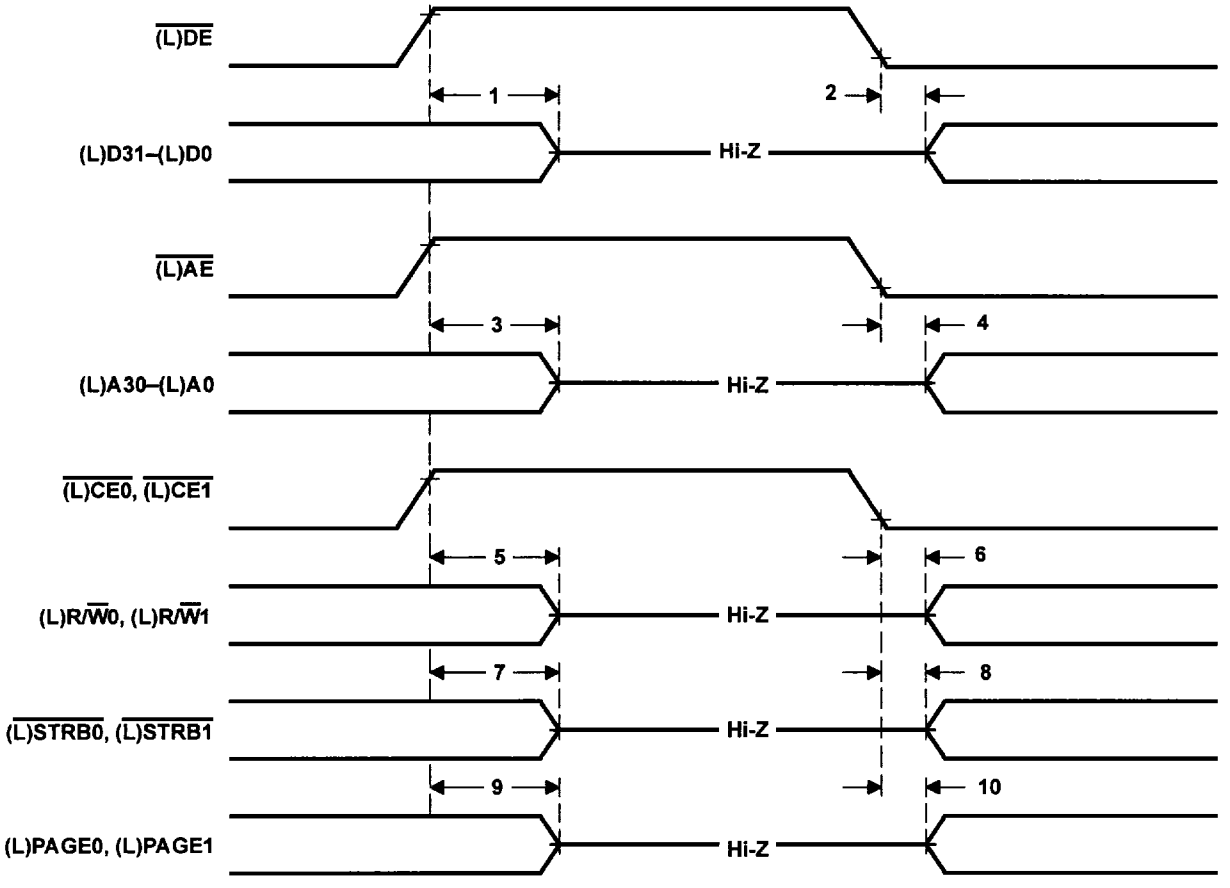


Figure 12. (L)DE, (L)AE, and (L)CEx Enable Timings

PARAMETER MEASUREMENT INFORMATION

timing parameters for (L)$\overline{\text{LOCK}}$ when executing LDFI or LDII (see Figure 13)

NO.		'320C40-33 '320C40-40		'320C40-50		UNIT
		MIN	MAX	MIN	MAX	
1	$t_{d(H1L\text{-}LOCKL)}$ Delay time, H1 low to (L)$\overline{\text{LOCK}}$ low		11		9	ns

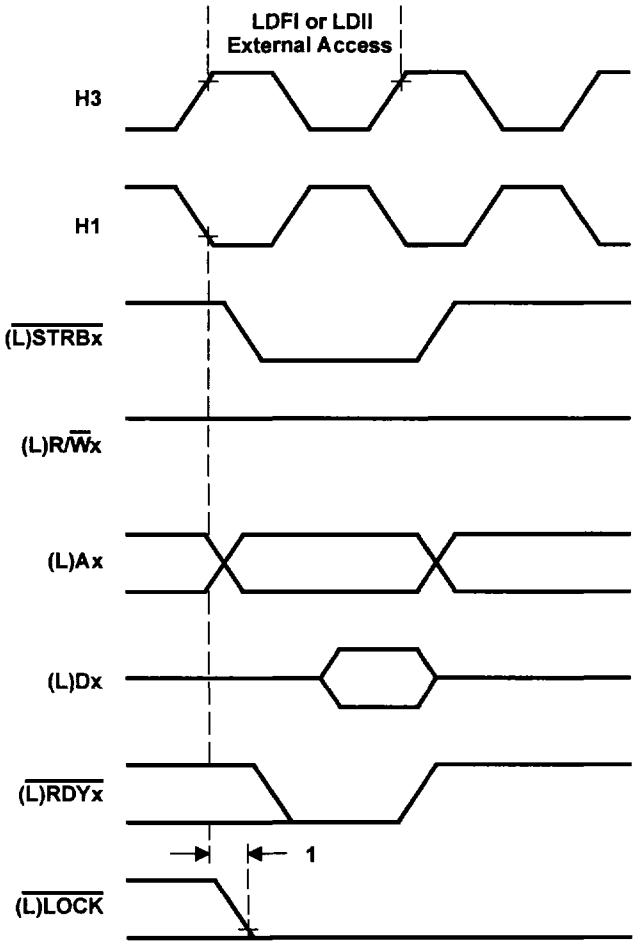


Figure 13. Timing for (L)$\overline{\text{LOCK}}$ When Executing LDFI or LDII

PARAMETER MEASUREMENT INFORMATION

timing parameters for $\overline{\text{(L)LOCK}}$ when executing STFI or STII (see Figure 14)

NO.	PARAMETER		'320C40-33 '320C40-40		'320C40-50		UNIT
			MIN	MAX	MIN	MAX	
1	$t_{d(H1L-LOCKH)}$	Delay time, H1 low to $\overline{\text{(L)LOCK}}$ high		11		9	ns

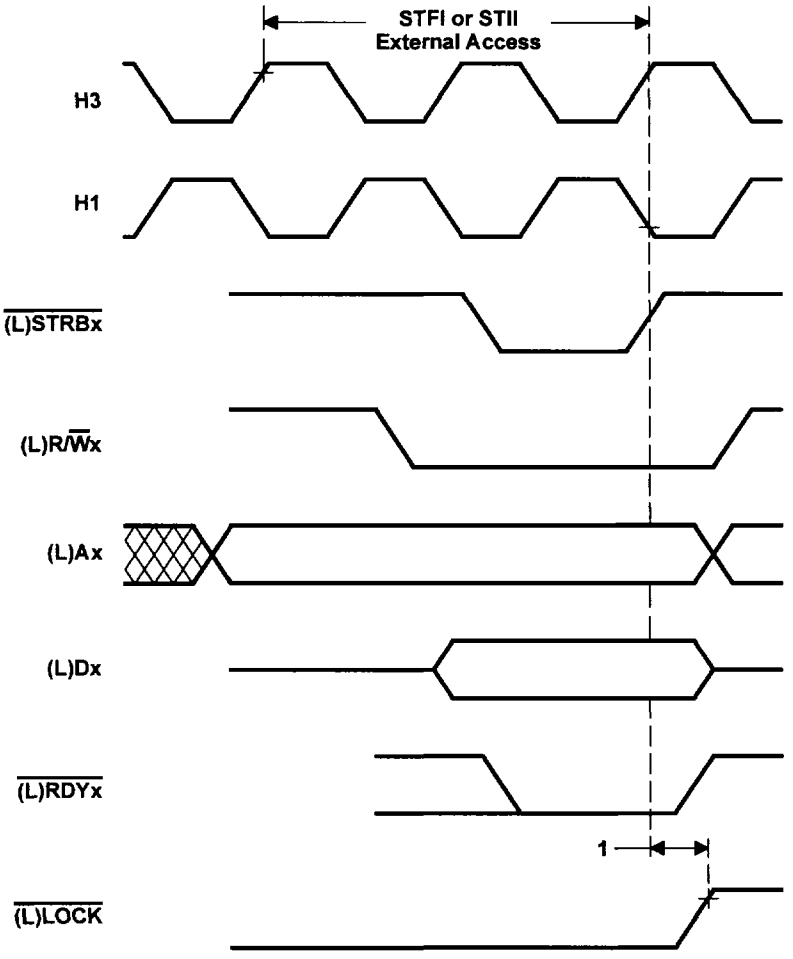


Figure 14. Timing for $\overline{\text{(L)LOCK}}$ When Executing STFI or STII

PARAMETER MEASUREMENT INFORMATION

timing parameters for $\overline{\text{(L)LOCK}}$ when executing SIGI (see Figure 15)

NO.			'320C40-33 '320C40-40		'320C40-50		UNIT
			MIN	MAX	MIN	MAX	
1	$t_{d(H1L\text{-}LOCKL)}$	Delay time, H1 low to $\overline{\text{(L)LOCK}}$ low		11		9	ns
2	$t_{d(H1L\text{-}LOCKH)}$	Delay time, H1 low to $\overline{\text{(L)LOCK}}$ high		11		9	ns

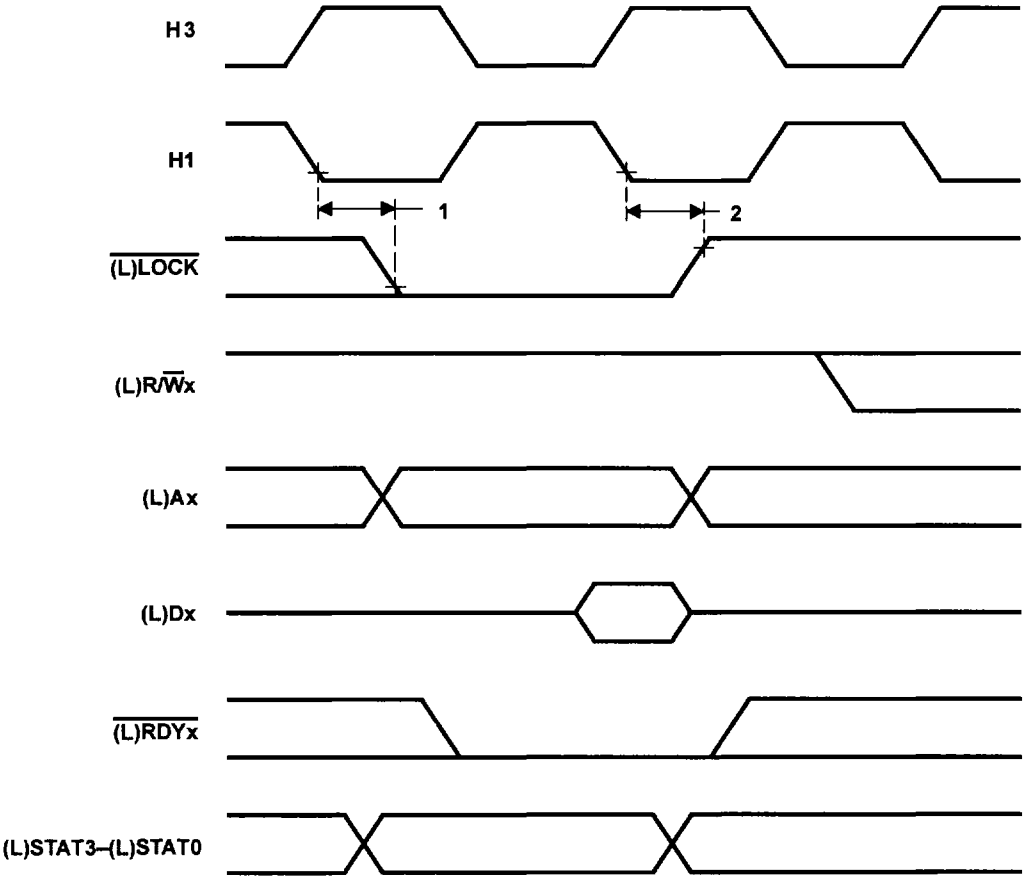


Figure 15. Timing for $\overline{\text{(L)LOCK}}$ When Executing SIGI

PARAMETER MEASUREMENT INFORMATION

timing parameters for (L)PAGE0, (L)PAGE1 during memory access to a different page (see Figure 16)

NO.			'320C40-33 '320C40-40 '320C40-50		UNIT
			MIN	MAX	
1	$t_{d(H1L\text{-}PAGEH)}$	Delay time, H1 low to (L)PAGEx high for access to different page	0	10	ns
2	$t_{d(H1L\text{-}PAGEL)}$	Delay time, H1 low to (L)PAGEx low for access to different page	0	10	ns

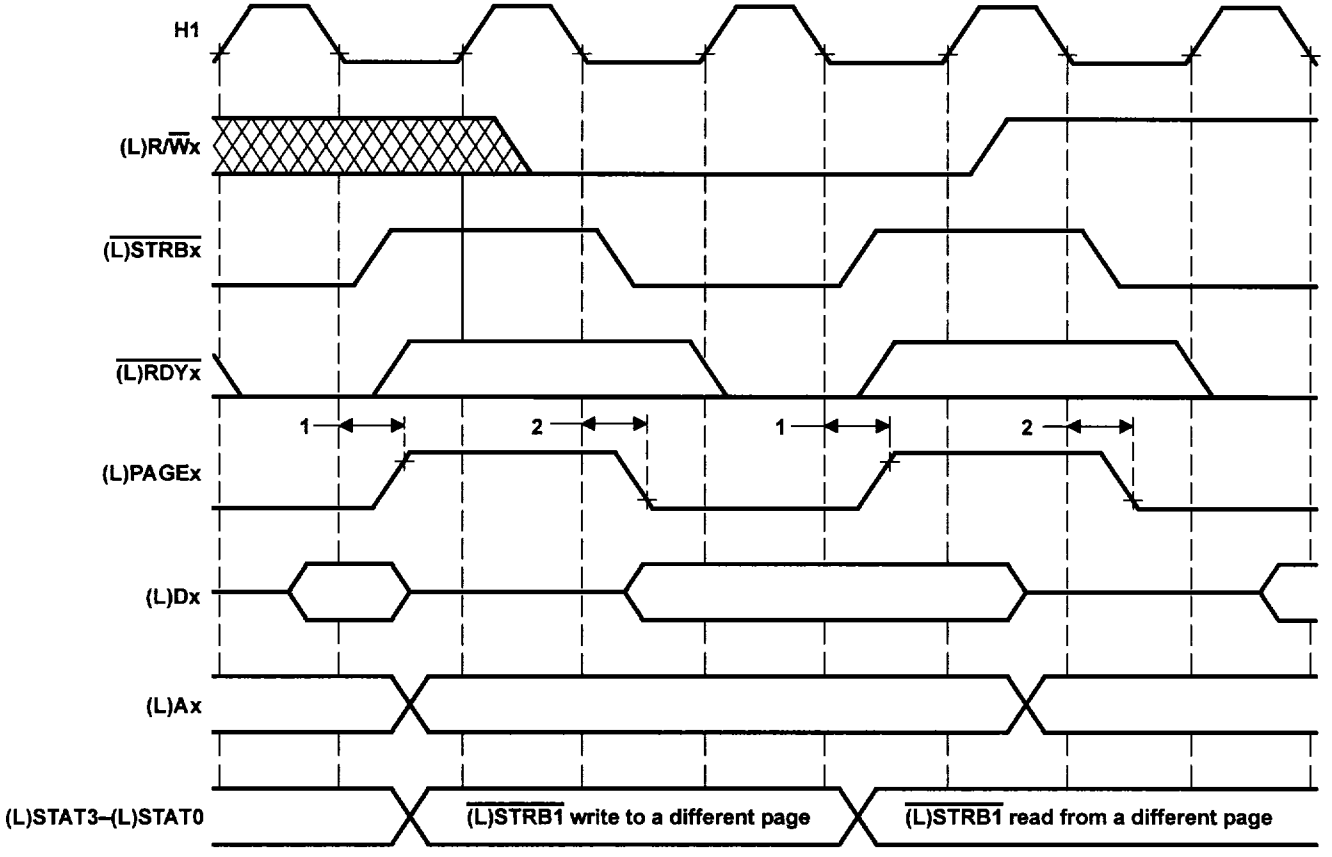


Figure 16. (L)PAGE0, (L)PAGE1 Timing Cycle, Memory Access to a Different Page

PARAMETER MEASUREMENT INFORMATION

timing parameters for loading IIF register ($\overline{\text{IIOFx}}$ pins) when configured as an output pin (see Figure 17)

NO.			'320C40-33 '320C40-40		'320C40-50		UNIT
			MIN	MAX	MIN	MAX	
1	$t_{v(H1L-IIOF)}$	H1 low to $\overline{\text{IIOFx}}$ valid		18		16	ns

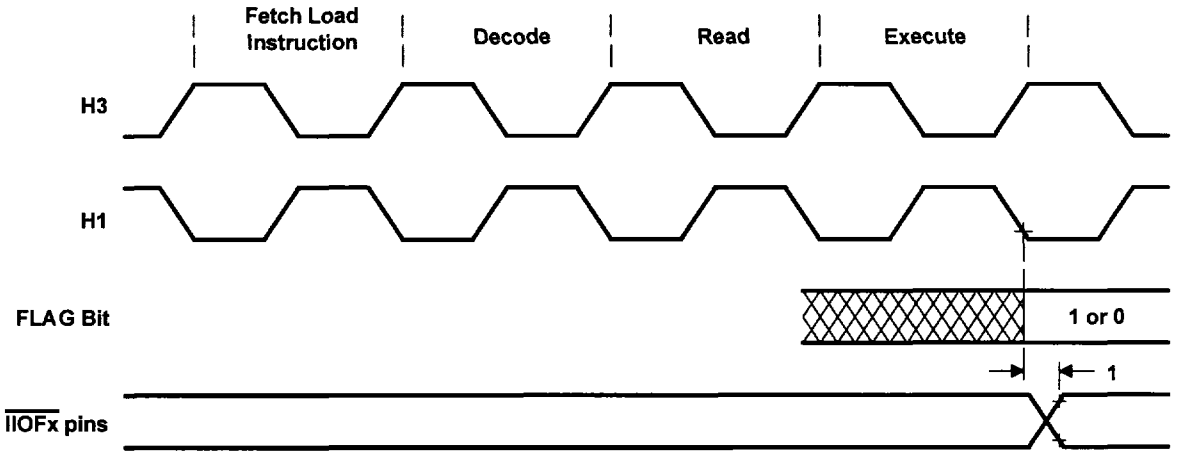


Figure 17. Timing for Loading IIF Register ($\overline{\text{IIOFx}}$ Pins) When Configured as an Output Pin

PARAMETER MEASUREMENT INFORMATION

timing parameters of $\overline{\text{IIOFx}}$ changing from output to input mode (see Figure 18)

NO.			'320C40-33 '320C40-40 '320C40-50		UNIT
			MIN	MAX	
1	$t_{h(H1L\text{-}IIOF)}$	Hold time, $\overline{\text{IIOFx}}$ after H1 low		14†	ns
2	$t_{su(IIOF)}$	Setup time, $\overline{\text{IIOFx}}$ before H1 low	11		ns
3	$t_{h(IIOF)}$	Hold time, $\overline{\text{IIOFx}}$ after H1 low	0		ns

† This parameter is specified by design but not tested.

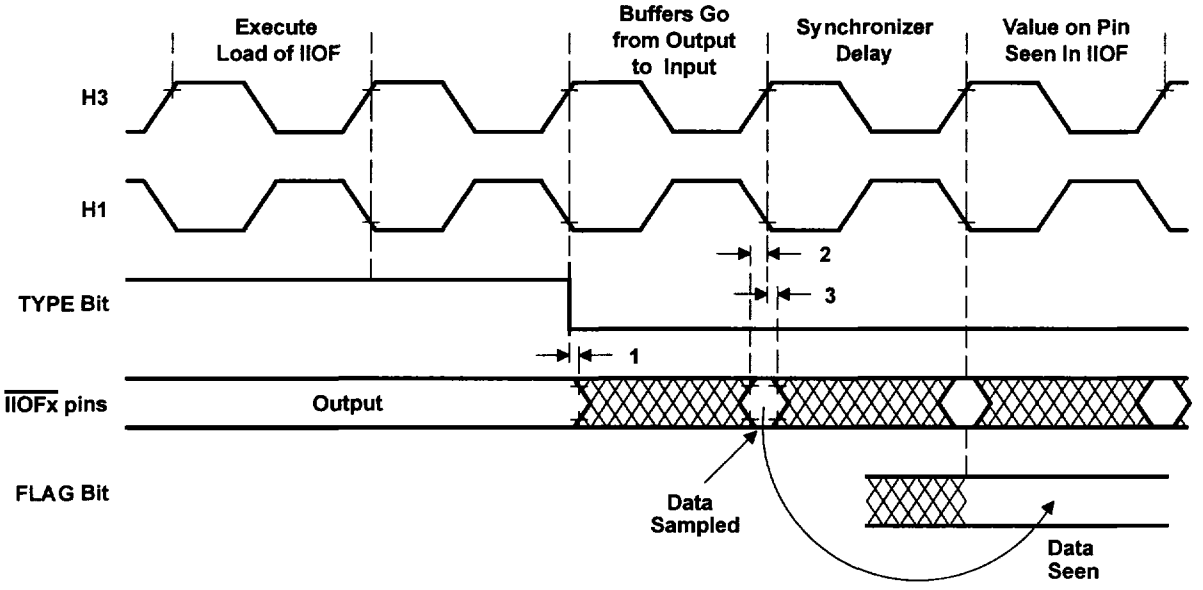


Figure 18. Change of $\overline{\text{IIOFx}}$ From Output to Input Mode

PARAMETER MEASUREMENT INFORMATION

timing parameters of $\overline{\text{IIOF}}x$ changing from input to output mode (see Figure 19)

NO.			'320C40-33 '320C40-40 '320C40-50		UNIT
			MIN	MAX	
1	$t_{d(H1L-IFIO)}$	Delay time, H1 low to $\overline{\text{IIOF}}x$ switching from input to output		16	ns

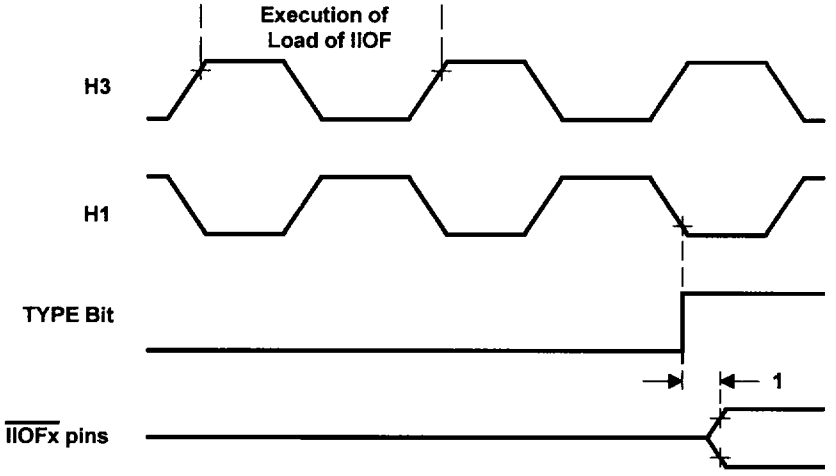


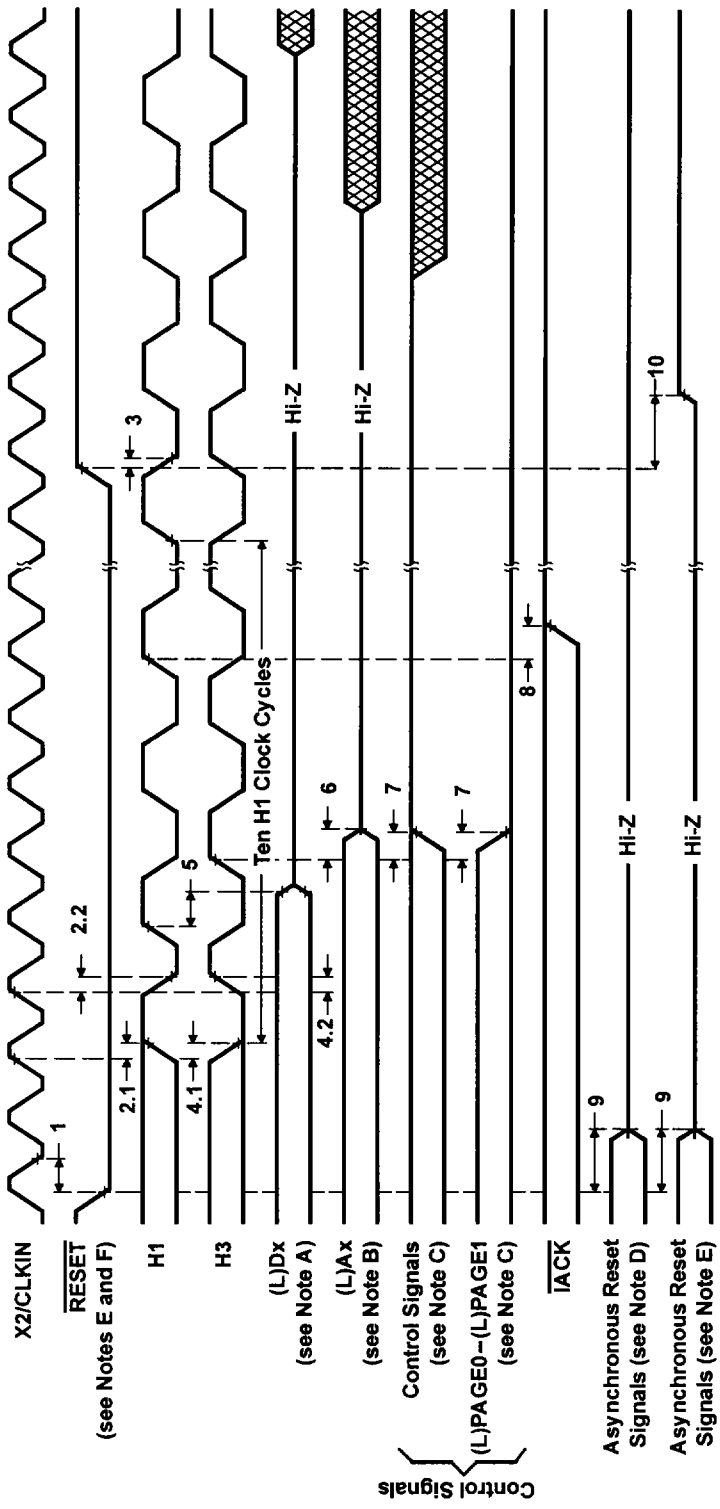
Figure 19. Change of $\overline{\text{IIOF}}x$ From Input to Output Mode

timing parameters for $\overline{\text{RESET}}$ (see Figure 20)

NO.			'320C40-33 '320C40-40		'320C40-50		UNIT
			MIN	MAX	MIN	MAX	
1	$t_{su(RESET-CIL)}$	Setup time, $\overline{\text{RESET}}$ before CLKIN low	11	$t_{c(CI)}$	11	$t_{c(CI)}$†	ns
2.1	$t_{d(CIH-H1H)}$	Delay time, CLKIN high to H1 high	2	12	2	10	ns
2.2	$t_{d(CIH-H1L)}$	Delay time, CLKIN high to H1 low	2	12	2	10	ns
3	$t_{su(RESETH-H1L)}$	Setup time, $\overline{\text{RESET}}$ high before H1 low and after ten H1 clock cycles	13		11		ns
4.1	$t_{d(CIH-H3L)}$	Delay time, CLKIN high to H3 low	2	12	2	10	ns
4.2	$t_{d(CIH-H3H)}$	Delay time, CLKIN high to H3 high	2	12	2	10	ns
5	$t_{dis(H1H-DZ)}$	Disable time, H1 high to (L)Dx in high-impedance state		13†		13†	ns
6	$t_{dis(H3H-AZ)}$	Disable time, H3 high to (L)Ax in high-impedance state		9†		9†	ns
7	$t_{d(H3H-CONTROLH)}$	Delay time, H3 high to control signals high [low for (L)PAGEx]		9†		9†	ns
8	$t_{d(H1H-IACKH)}$	Delay time, H1 high to $\overline{\text{IACK}}$ high		9†		9†	ns
9	$t_{dis(RESETL-ASYNCHZ)}$	Disable time, $\overline{\text{RESET}}$ low to asynchronous reset signals in the high-impedance state		21†		21†	ns
10	$t_{d(RESETL-COMMH)}$	Delay time, $\overline{\text{RESET}}$ high to asynchronous reset signals high		15†		15†	ns

† This parameter is characterized but not tested.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. In this figure, (L)Dx includes D31–D0, LD31–D0, and CxD7–CxD0.
B. (L)Ax includes A30–A0 and LA30–LA0.
C. Control signals LSTRB0, LSTRB1, STRB0, STRB1, (L)STAT3–(L)STAT0, (L)LOCK, (L)R/$\overline{W}$0, and (L)R/$\overline{W}$1 go high while (L)PAGE0 and (L)PAGE1 go low.
D. Asynchronous reset signals that go into high impedance after RESET goes low include TCLK0, TCLK1, IIOF3–IIOF0, and the communication-port control signals CREQx, CACKy, CSTRBy, and CRDYx (where x = 0, 1, or 2, and y = 3, 4, or 5). (At reset, ports 0, 1, and 2 become outputs, and ports 3, 4, and 5 become inputs.)
E. Asynchronous reset signals that go to a high-logic level after RESET goes low include CREQy, CACKx, CSTRBx, and CRDYy (where x = 0, 1, or 2, and y = 3, 4, or 5).
F. RESET is an asynchronous input and can be asserted at any point during a clock cycle. If the specified timings are met, the exact sequence shown will occur; otherwise, an additional delay of one clock cycle can occur.

Figure 20. RESET Timing

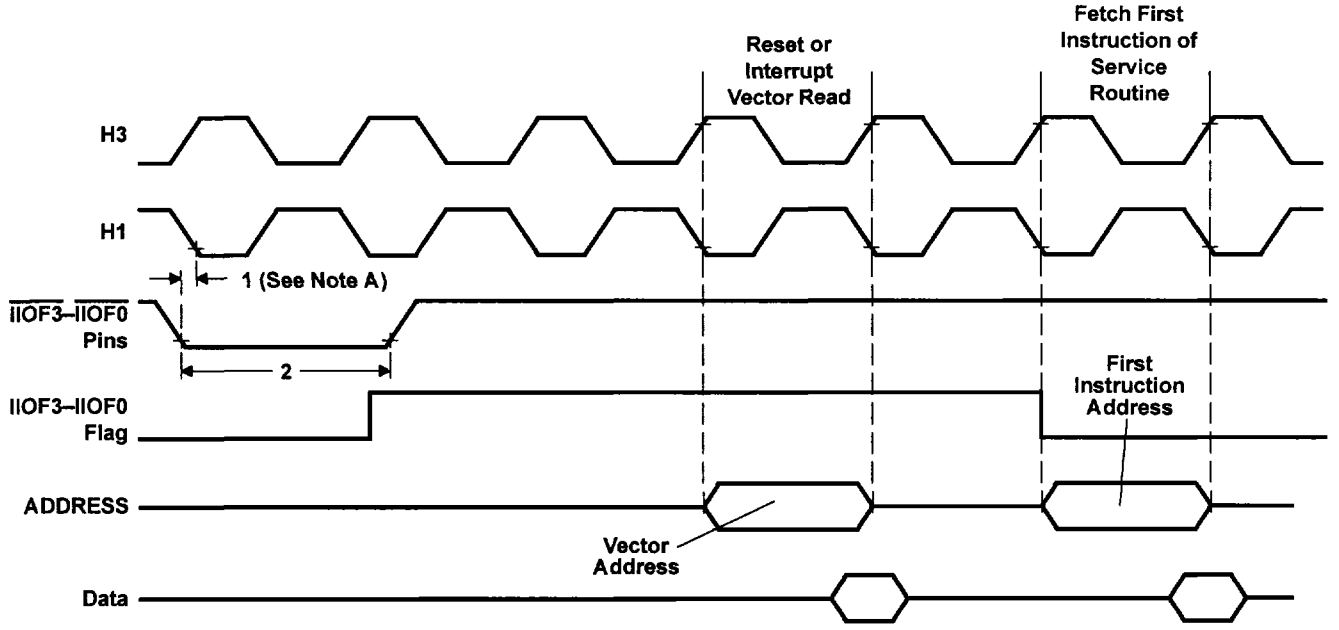
PARAMETER MEASUREMENT INFORMATION

timing parameters for $\overline{\text{IIOF3}}$–$\overline{\text{IIOF0}}$ interrupt response [P = $t_{c(H)}$] (see Figure 21, Note 7, and Note 8)

NO.			'320C40-33			'320C40-40 '320C40-50			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
1	$t_{su(IIOF-H1L)}$	Setup time, $\overline{\text{IIOF3}}$–$\overline{\text{IIOF0}}$ before H1 low	11			11			ns
2	$t_{w(IIOF)}$	Interrupt pulse duration to assure one interrupt seen (see Note 6)	P	1.5P	< 2P†	P	1.5P	< 2P†	ns

† This parameter is specified by design but not tested.

NOTES: 6. Level-triggered interrupts require interrupt pulse duration of at least 1P wide (P = one H1 period) to ensure it is seen. It must be less than 2P wide to assure it is responded to only once. Recommended pulse duration is 1.5P.
7. $\overline{\text{IIOFx}}$ is an asynchronous input and can be asserted at any point during a clock cycle. If the specified timings are met, the exact sequence shown occurs; otherwise, an additional delay of one clock cycle can occur.
8. Edge-triggered interrupts require a setup of time (1) and a minimum duration of P. No maximum duration limit exists.



NOTE A: The 'C40 can accept an interrupt from the same source every two H1 clock cycles.

Figure 21. $\overline{\text{IIOF3}}$–$\overline{\text{IIOF0}}$ Interrupt Response Timing [P=$t_{c(H)}$]

PARAMETER MEASUREMENT INFORMATION

timing parameters for $\overline{\text{IACK}}$ (see Note 9 and Figure 22)

NO.			'320C40-33 '320C40-40 '320C40-50		UNIT
			MIN	MAX	
1	$t_{d(H1H-IACKL)}$	Delay time, H1 high to $\overline{\text{IACK}}$ low		9	ns
2	$t_{d(H1L-IACKH)}$	Delay time, H1 low to $\overline{\text{IACK}}$ high during first cycle of IACK instruction data read		9	ns

NOTE 9: The $\overline{\text{IACK}}$ output is active for the entire duration of the bus cycle and, therefore, is extended if the bus cycle utilizes wait states.

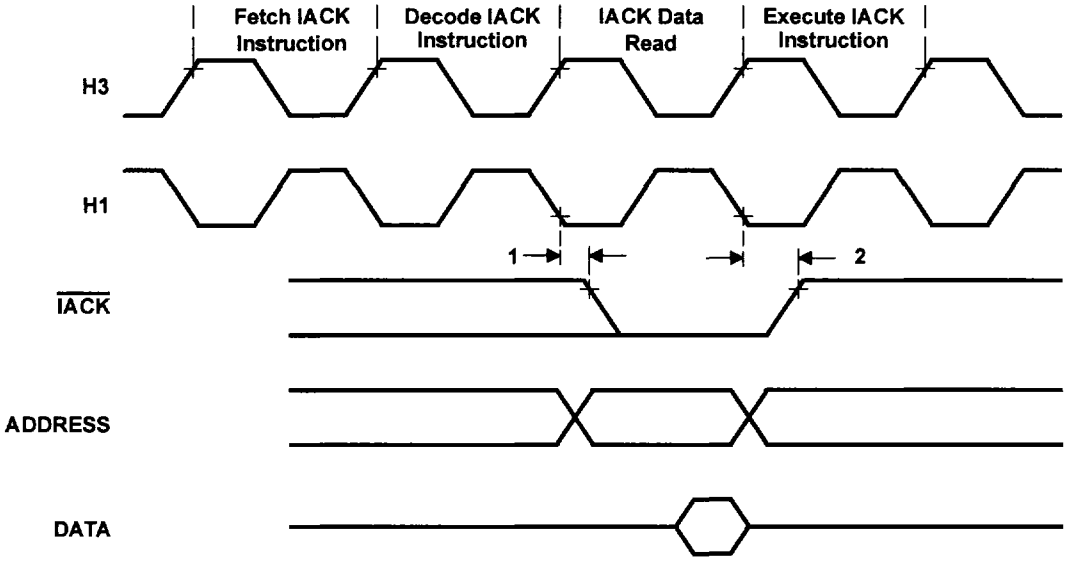


Figure 22. $\overline{\text{IACK}}$ Timing

PARAMETER MEASUREMENT INFORMATION

communication-port word-transfer cycle timing [P=$t_{c(H)}$] (see Note 10 and Figure 23)

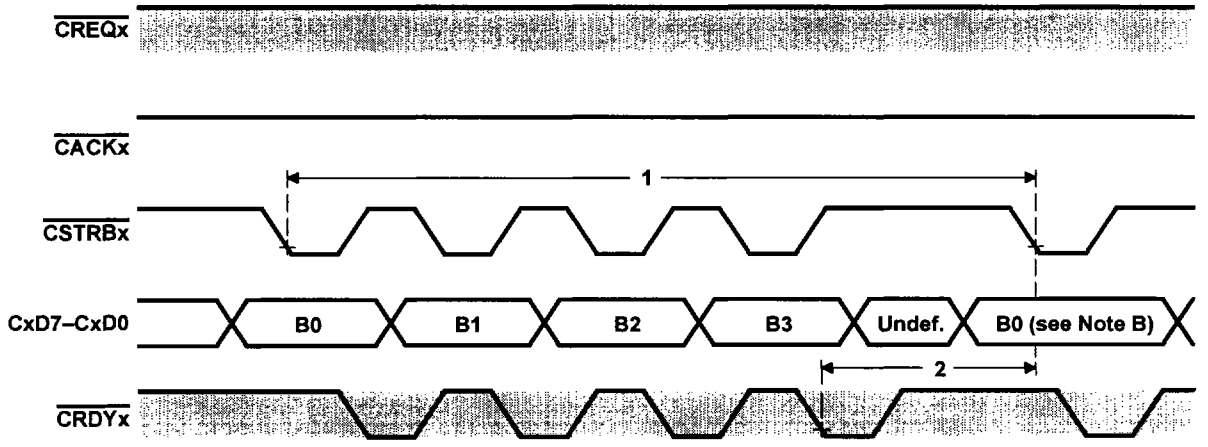
NO.			'320C40-33† '320C40-40† '320C40-50†		UNIT
			MIN	MAX	
1	$t_{c(WORD)}$‡§	Cycle time, word transfer (4 bytes = 1 word)	1.5P+7	2.5P+170	ns
2	$t_{d(CRDYL-CSL)W}$‡	Delay time, $\overline{CRDYx}$ low to $\overline{CSTRBx}$ low between back-to-back write cycles	1.5P+7	2.5P+28	ns

† For these timing values, it is assumed that the SMJ320C40 that is to receive data is ready to receive data.

‡ This parameter is characterized but not tested.

§ $t_{c(WORD)}$ max = 2.5P + 28 ns + 4([6]) + 3([2] + [9] + [4]), where boxed numbers refer to the max values for corresponding parameters in the communication-port byte timing table on the next page (for example, [6] means the value under max for parameter 6 in the table — a value of 10 ns). This timing assumes that two 'C40s are connected.

NOTE 10: These timings apply only to two communicating 'C4xs. When a non-'C4x device communicates with a 'C40, timings can be longer. No restriction exists in this case on how slow the transfer could be except when using early silicon ('C40 P6 1.x or 2.x). See the $\overline{CSTRB}$ width restriction in Section 8.9.1 of the *TMS320C4x User's Guide* (literature number SPRU063).



= when signal is an input (clear = when signal is an output)

NOTES: A. For correct operation during token exchange, the two communicating SMJ320C40s must have CLKIN frequencies within a factor of 2 of each other (in other words, at most, one of the SMJ320C40s can be twice as fast as the other).

B. Begins byte 0 of the next word

Figure 23. Communication-Port Word-Transfer-Cycle Timing [P=$t_{c(H)}$]

PARAMETER MEASUREMENT INFORMATION

communication-port byte timing parameters (write and read) (see Note 11 and Figure 24)

NO.			'320C40-33 '320C40-40 '320C40-50		UNIT
			MIN	MAX	
1	$t_{su(CD-CSL)W}$	Setup time, CxDx data valid before $\overline{CSTRBx}$ low (write)	2		ns
2	$t_{d(CRDYL-CSH)W}$	Delay time, $\overline{CRDYx}$ low to $\overline{CSTRBx}$ high (write)	0†	12	ns
3	$t_{h(CRDYL-CD)W}$	Hold time, CxDx after $\overline{CRDYx}$ low (write)	1		ns
4	$t_{d(CRDYH-CSL)W}$	Delay time, $\overline{CRDYx}$ high to $\overline{CSTRBx}$ low for subsequent bytes (write)	0†	12	ns
5	$t_{c(BYTE)}$‡§	Cycle time, byte transfer		44	ns
6	$t_{d(CSL-CRDYL)R}$	Delay time, $\overline{CSTRBx}$ low to $\overline{CRDYx}$ low (read)	0†	10	ns
7	$t_{su(CSH-CD)R}$	Setup time, CxDx valid after $\overline{CSTRBx}$ high (read)	0		ns
8	$t_{h(CRDYL-CD)R}$	Hold time, CxDx valid after $\overline{CRDYx}$ low (read)	2		ns
9	$t_{d(CSH-CRDYH)R}$	Delay time, $\overline{CSTRBx}$ high to $\overline{CRDYx}$ high (read)	0†	10	ns

† This parameter is specified by design but not tested.
‡ This parameter is characterized but not tested.
§ $t_{c(BYTE)}$ max = ([2] + [4] + [6] + [9]) where boxed numbers refer to the max values for corresponding parameters in the above table (for example, [6] means the value under max for parameter 6 in the table — a value of 10 ns). This assumes that two 'C40s are connected.
NOTE 11: Communication port timing does not include line length delay.

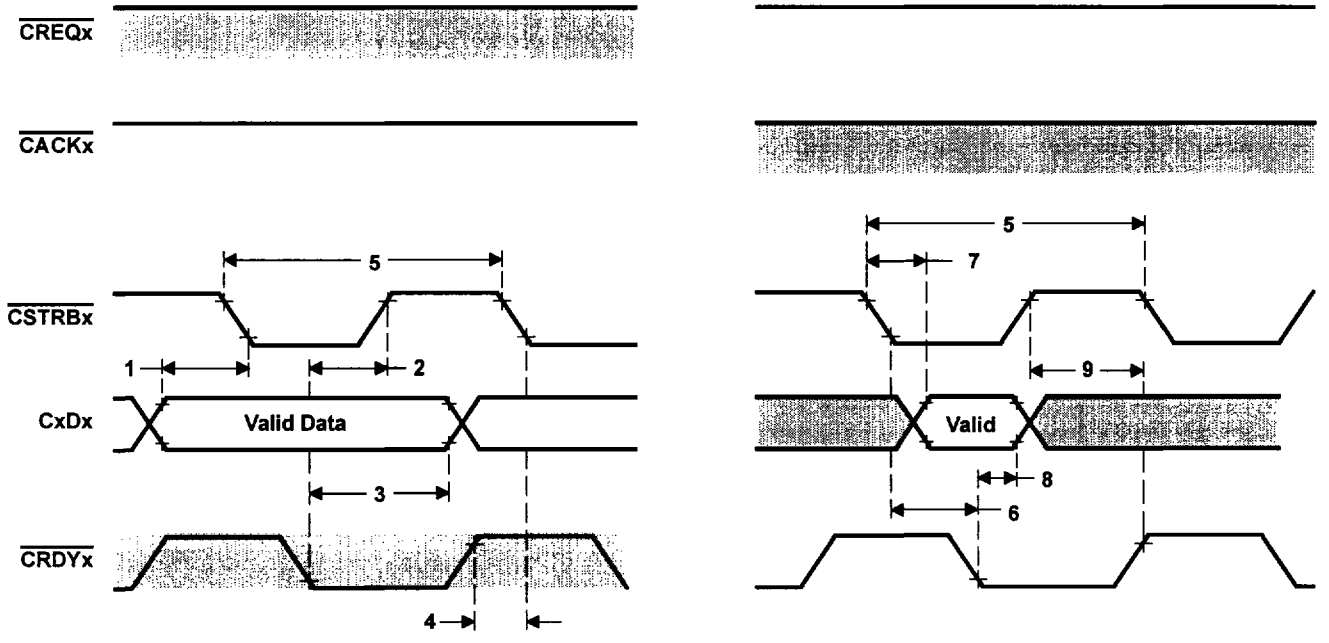


Figure 24. Communication-Port Byte Timing (Write and Read)

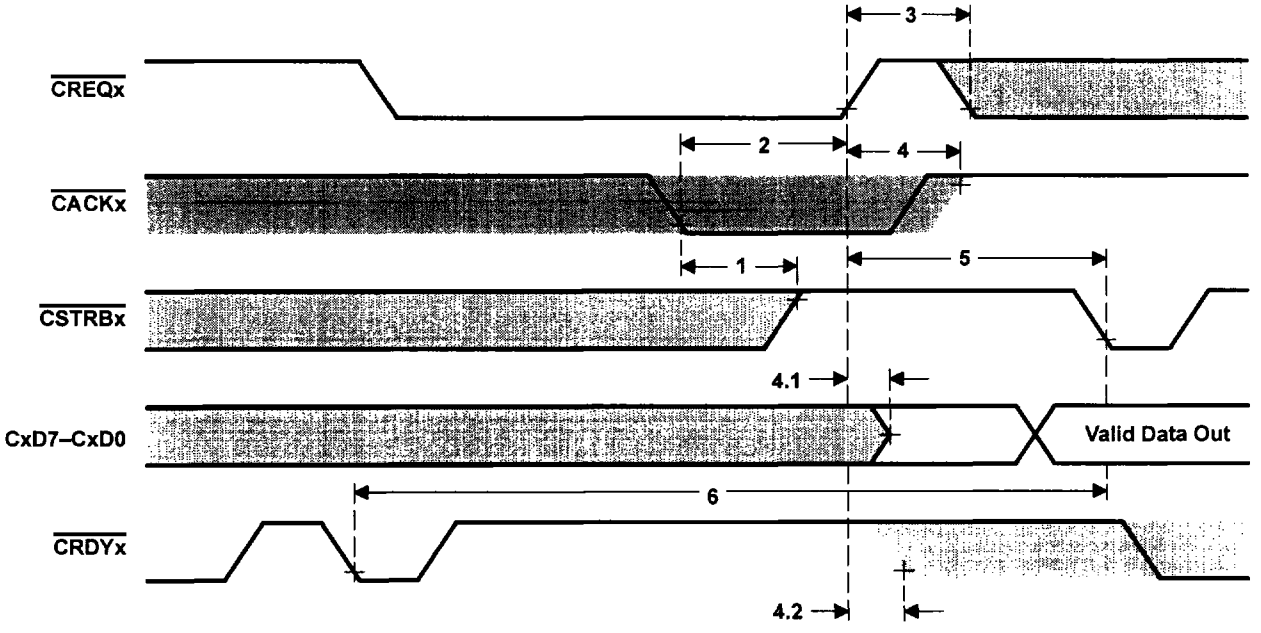
PARAMETER MEASUREMENT INFORMATION

timing parameters for communication-token transfer sequence, input to an output port [P = $t_{c(H)}$]† (see Figure 25)

NO.			'320C40-33† '320C40-40† '320C40-50†		UNIT
			MIN	MAX	
1‡	$t_{d(CAL-CS)T}$	Delay time, $\overline{CACKx}$ low to $\overline{CSTRBx}$ change from input to a high-level output	0.5P+ 6	1.5P+ 22	ns
2‡	$t_{d(CAL-CRQH)T}$	Delay time, $\overline{CACKx}$ low to start of $\overline{CREQx}$ going high for token-request acknowledge	P + 5	2P + 26	ns
3	$t_{d(CRQH-CRQ)T}$	Delay time, start of $\overline{CREQx}$ going high to $\overline{CREQx}$ change from output to an input	0.5P – 5	0.5P+ 13	ns
4	$t_{d(CRQH-CA)T}$	Delay time, start of $\overline{CREQx}$ going high to $\overline{CACKx}$ change from an input to an output level high	0.5P – 5	0.5P+13	ns
4.1	$t_{d(CRQH-CD)T}$	Delay time, start of $\overline{CREQx}$ going high to CxD7–CxD0 change from inputs driven to outputs driven	0.5P – 5	0.5P+13	ns
4.2	$t_{d(CRQH-CRDY)T}$	Delay time, start of $\overline{CREQx}$ going high to $\overline{CRDYx}$ change from an output to an input	0.5P – 5	0.5P+13	ns
5	$t_{d(CRQH-CSL)T}$	Delay time, start of $\overline{CREQx}$ going high to $\overline{CSTRBx}$ low for start of word transfer out	1.5P – 8	1.5P+ 9	ns
6	$t_{d(CRDYL-CSL)T}$	Delay time, $\overline{CRDYx}$ low at end of word input to $\overline{CSTRBx}$ low for word output	3.5P+12	5.5P+ 48	ns

† This parameter is characterized but not tested.

‡ These timing parameters result from synchronizer delays and are referenced from the falling edge of H1. The inputs (that cause the output-signal pins to change values) are sampled on H1 falling. The minimum delay occurs when the input condition occurs just before H1 falling, and the maximum delay occurs when the input condition occurs just after H1 falling.



NOTE A: Before the token exchange, $\overline{CREQx}$ and $\overline{CRDYx}$ are output signals asserted by the SMJ320C40 that is receiving data. $\overline{CACKx}$, $\overline{CSTRBx}$, and CxD7–CxD0 are input signals asserted by the device sending data to the 'C40; these are asynchronous with respect to the H1 clock of the receiving SMJ320C40. After token exchange, $\overline{CACKx}$, $\overline{CSTRBx}$, and CxD7–CxD0 become output signals, and $\overline{CREQx}$ and $\overline{CRDYx}$ become inputs.

Figure 25. Communication-Token Transfer Sequence, Input to an Output Port [P=$t_{c(H)}$]

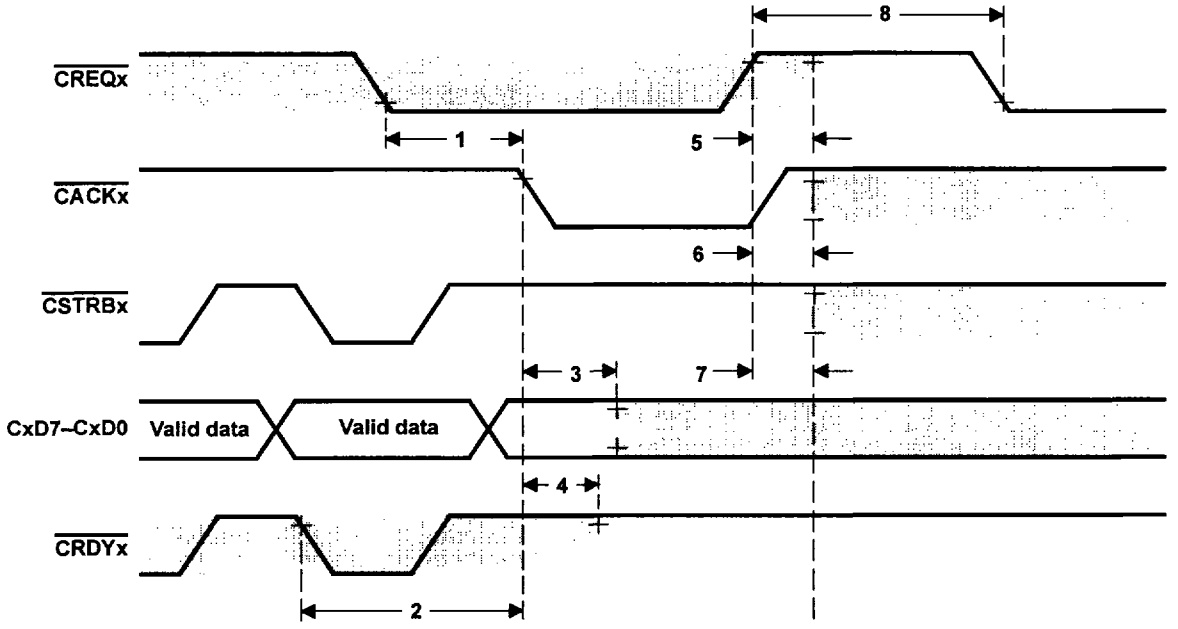
PARAMETER MEASUREMENT INFORMATION

timing parameters for communication-token transfer sequence, output to an input port [P = $t_{c(H)}$]† (see Figure 26)

NO.			'320C40-33† '320C40-40† '320C40-50†		UNIT
			MIN	MAX	
1‡	$t_{d(CRQL-CAL)T}$	Delay time, $\overline{CREQx}$ low to start of $\overline{CACKx}$ going low for token-request acknowledge	P+5	2P+26	ns
2‡	$t_{d(CRDYL-CAL)T}$	Delay time, start of $\overline{CRDYx}$ low at end of word transfer out to start of $\overline{CACKx}$ going low	P+6	2P+27	ns
3	$t_{d(CAL-CD)I}$	Delay time, start of $\overline{CACKx}$ going low to CxD7–CxD0 change from outputs to inputs	0.5P–8	0.5P+8	ns
4	$t_{d(CAL-CRDY)T}$	Delay time, start of $\overline{CACKx}$ going low to $\overline{CRDYx}$ change from an input to output, high level	0.5P–8	0.5P+8	ns
5‡	$t_{d(CRQH-CRQ)T}$	Delay time, $\overline{CREQx}$ high to $\overline{CREQx}$ change from an input to output, high level	4	22	ns
6‡	$t_{d(CRQH-CA)T}$	Delay time, start of $\overline{CREQx}$ high to $\overline{CACKx}$ change from output to an input	4	22	ns
7‡	$t_{d(CRQH-CS)T}$	Delay time, start of $\overline{CREQx}$ high to $\overline{CSTRBx}$ change from output to an input	4	22	ns
8‡	$t_{d(CRQH-CRQL)T}$	Delay time, $\overline{CREQx}$ high to $\overline{CREQx}$ low for the next token request	P–4	2P+8	ns

† This parameter is characterized but not tested.

‡ These timing parameters result from synchronizer delays and are referenced from the falling edge of H1. The inputs (that cause the output-signal pins to change values) are sampled on H1 falling. The minimum delay occurs when the input condition occurs just before H1 falling, and the maximum delay occurs when the input condition occurs just after H1 falling.



NOTE A: Before the token exchange, $\overline{CACKx}$, $\overline{CSTRBx}$, and CxD7–CxD0 are asserted by the 'C40 sending data. $\overline{CREQx}$ and $\overline{CRDYx}$ are input signals asserted by the 'C40 receiving data and are asynchronous with respect to the H1 clock of the sending 'C40. After token exchange, $\overline{CREQx}$ and $\overline{CRDYx}$ become outputs, and $\overline{CSTRBx}$, $\overline{CACKx}$, and CxD7–CxD0 become inputs.

Figure 26. Communication-Token Transfer Sequence, Output to an Input Port [P = $t_{c(H)}$]

PARAMETER MEASUREMENT INFORMATION

timing parameters for timer pin (see Note 12 and Figure 27)

NO.			'320C40-33 '320C40-40 '320C40-50		UNIT
			MIN	MAX	
1	$t_{su(TCLK-H1L)}$	Setup time, TCLK before H1 low	10		ns
2	$t_{h(H1L-TCLK)}$	Hold time, TCLK after H1 low	0		ns
3	$t_{d(H1H-TCLK)}$	Delay time, TCLK valid after H1 high		13	ns

NOTE 12: Period and polarity of valid logic level are specified by contents of internal control registers.

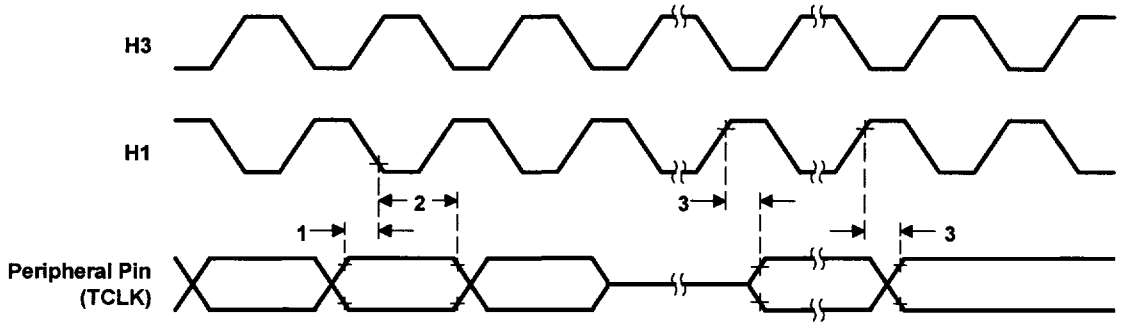


Figure 27. Timer Pin Timing Cycle

timing for IEEE 1149.1 test-access port (see Figure 28)

NO.			'320C40-33 '320C40-40 '320C40-50		UNIT
			MIN	MAX	
1	$t_{su(TMS-TCKH)}$	Setup time, TMS/TDI before TCK high	10		ns
2	$t_{h(TCKH-TMS)}$	Hold time, TMS/TDI after TCK high	5		ns
3	$t_{d(TCKL-TDOV)}$	Delay time, TCK low to TDO valid	0	15	ns

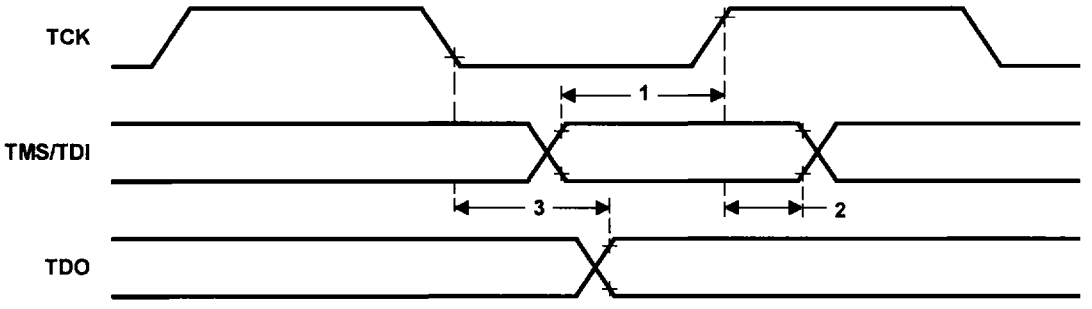
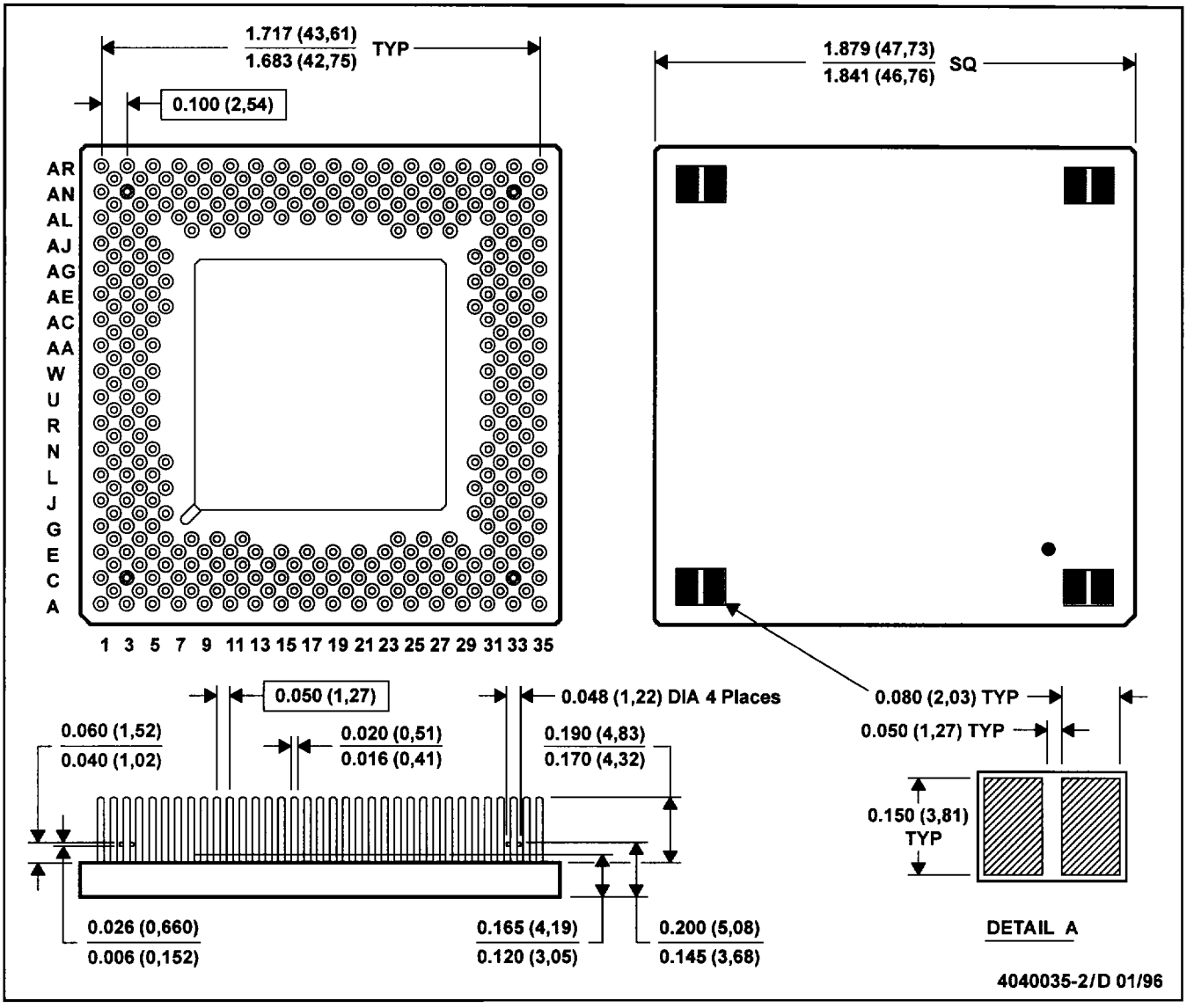


Figure 28. JTAG Emulation Timings

MECHANICAL DATA

GF (S-CPGA-P325) **CERAMIC PIN GRID ARRAY PACKAGE**

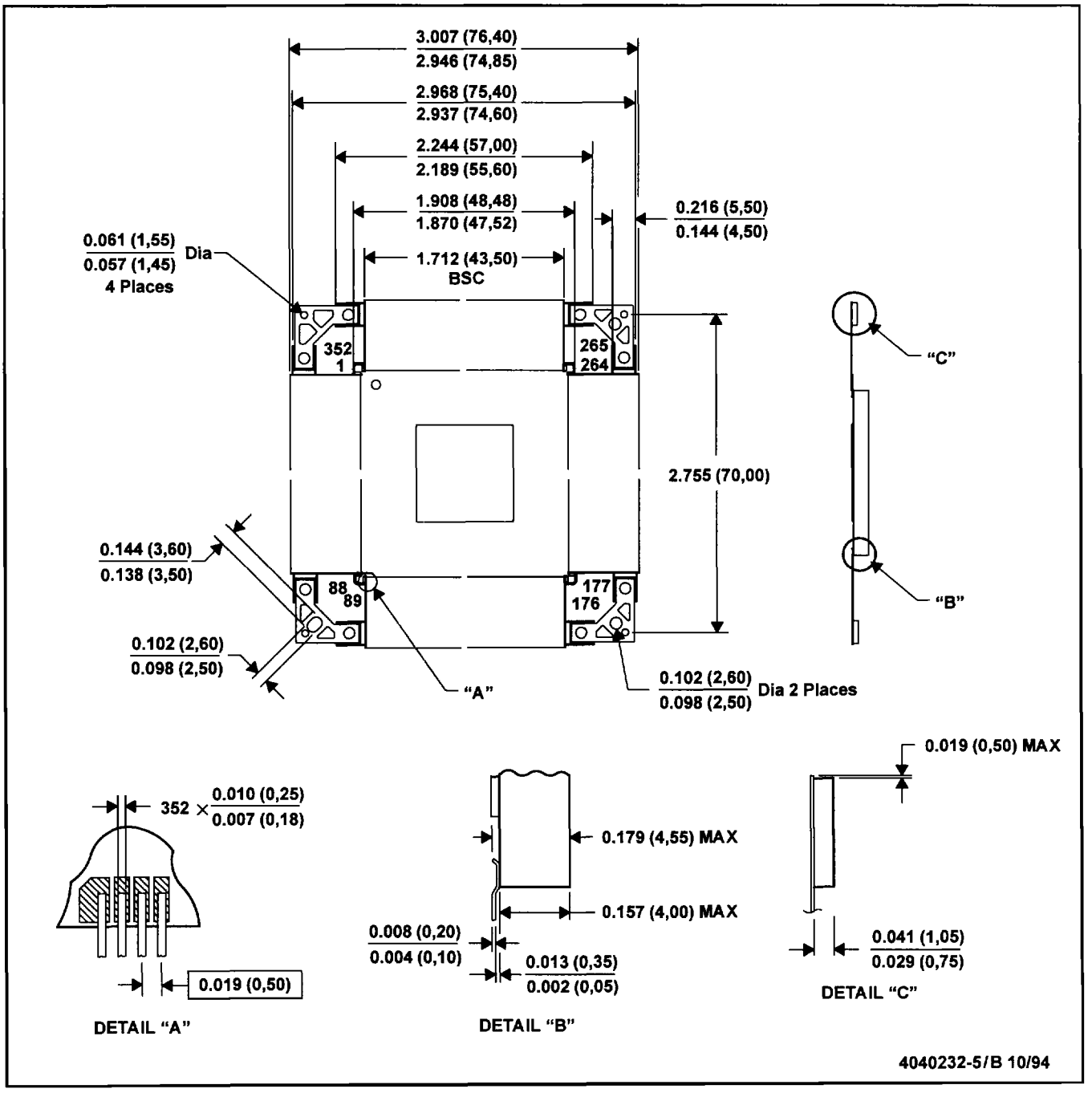


NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Package thickness of 0.165 (4,19) / 0.120 (3,05) includes package body and lid.

Thermal Resistance Characteristics		
Parameter	**°C/W**	**Air Flow LFPM**
$R\Theta_{JC}$	1.7	N/A
$R\Theta_{JA}$	10.9	0
RΘJA	9.8	200
$R\Theta_{JA}$	7.0	400
$R\Theta_{JA}$	6.4	600
$R\Theta_{JA}$	5.6	800
$R\Theta_{JA}$	5.5	1000

MECHANICAL DATA

HFH (S-CQFP-F352) **CERAMIC QUAD FLATPACK WITH TIE BAR**



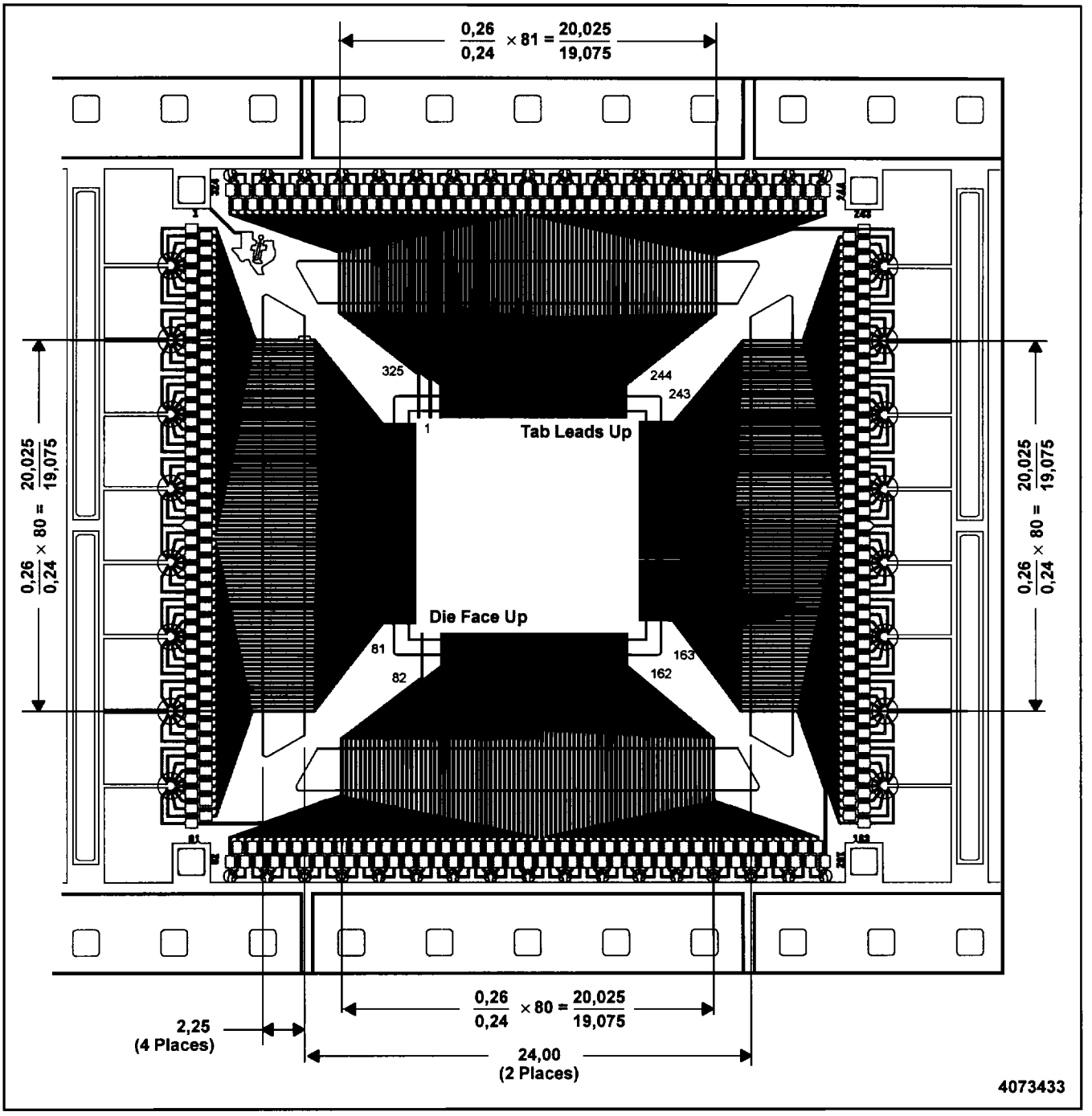
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within JEDEC MO-134 AE

THERMAL RESISTANCE CHARACTERISTICS	
Parameter	° C/W
$R\Theta_{JC}$	1.28
$R\Theta_{JA}$	28.70

MECHANICAL DATA

TAB (48 mm WITH PROTECTIVE FILM)

SMJ320C40 324-PIN TAB FRAME SOCKET (PG 5.1)
325 OLB/ILB 0.25 mm OLB PITCH

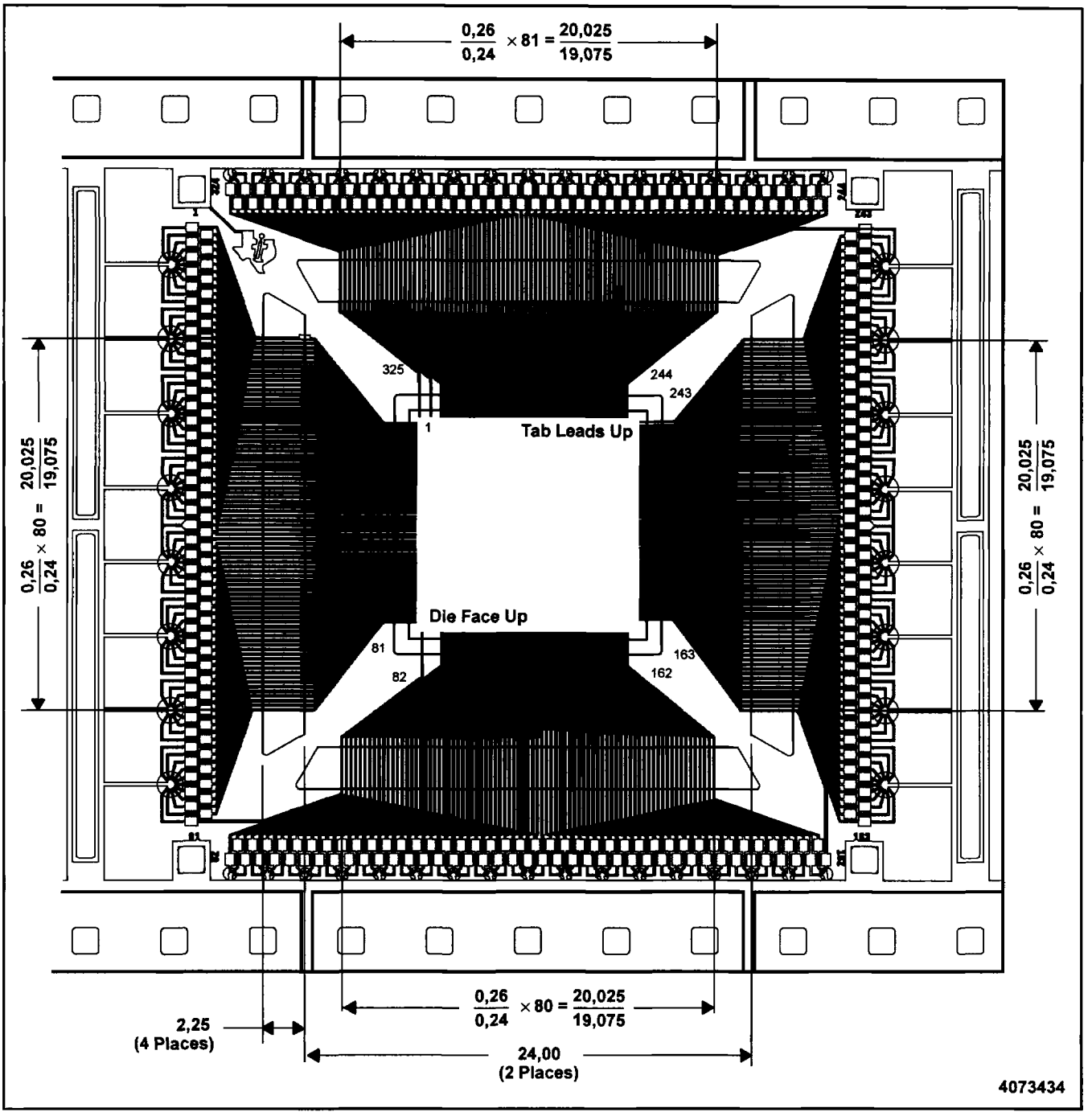


NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. The OLB lead width is 0,10 ± 0,02 mm.
D. The ILB lead width is 0,05 ± 0,01 mm.
E. The tape width is 48 mm.
F. The TAB is encapsulated die with polyimide overcoat.

MECHANICAL DATA

TBB (48 mm WITHOUT PROTECTIVE FILM)

SMJ320C40 324-PIN TAB FRAME SOCKET (PG 5.1)
325 OLB/ILB 0.25 mm OLB PITCH



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. The OLB lead width is 0,10 ± 0,02 mm.
D. The ILB lead width is 0,05 ± 0,01 mm.
E. The tape width is 48 mm.
F. The TBB is bare die.

PRODUCT ORDERING INFORMATION

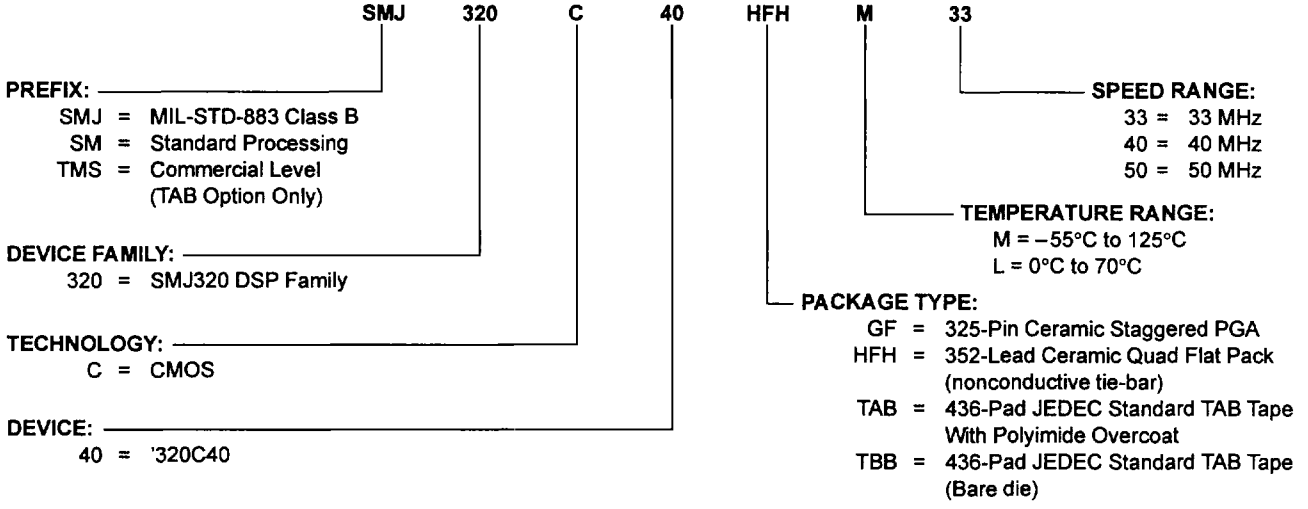
SMJ320C40 standard package ordering information

DEVICE	POWER SUPPLY	OPERATING FREQUENCY	PACKAGE TYPE	PROCESSING LEVEL
SMJ320C40GFM33	5 V ± 10%	33 MHz	Ceramic 325-pin staggered PGA (GF)	QML
SM320C40GFM33	5 V ± 10%	33 MHz	Ceramic 325-pin staggered PGA (GF)	Standard
SMJ320C40GFM40	5 V ± 5%	40 MHz	Ceramic 325-pin staggered PGA (GF)	QML
SM320C40GFM40	5 V ± 5%	40 MHz	Ceramic 325-pin staggered PGA (GF)	Standard
SMJ320C40GFM50	5 V ± 5%	50 MHz	Ceramic 325-pin staggered PGA	QML
SM320C40GFM50	5 V ± 5%	50 MHz	Ceramic 325-pin staggered PGA	Standard
SMJ320C40HFHM33	5 V ± 10%	33 MHz	Ceramic 352-pin quad flatpack (HFH)	QML
SM320C40HFHM33	5 V ± 10%	33 MHz	Ceramic 352-pin quad flatpack (HFH)	Standard
SMJ320C40HFHM40	5 V ± 5%	40 MHz	Ceramic 352-pin quad flatpack (HFH)	QML
SM320C40HFHM40	5 V ± 5%	40 MHz	Ceramic 352-pin quad flatpack (HFH)	Standard
SMJ320C40HFHM50	5 V ± 5%	50 MHz	Ceramic 352-pin quad flatpack	QML
SM320C40HFHM50	5 V ± 5%	50 MHz	Ceramic 352-pin quad flatpack	Standard

SMJ320C40 TAB ordering information

DEVICE	POWER SUPPLY	OPERATING FREQUENCY	PACKAGE TYPE	PROCESSING LEVEL
SMJ320C40TABM40	5 V ± 5%	40 MHz	325 ILB/OLB TAB tape (encapsulated)	QML
SMJ320C40TBBM40	5 V ± 5%	40 MHz	325 ILB/OLB TAB tape (bare die)	QML
TMS320C40TABL40	5 V ± 5%	40 MHz	325 ILB/OLB TAB tape (encapsulated)	Commercial (No Burn-In)
SMJ320C40TABM50	5 V ± 5%	50 MHz	325 ILB/OLB TAB tape (encapsulated)	QML
SMJ320C40TBBM50	5 V ± 5%	50 MHz	325 ILB/OLB TAB tape (bare die)	QML
TMS320C40TABL50	5 V ± 5%	50 MHz	325 ILB/OLB TAB tape (encapsulated)	Commercial (No Burn-In)
TMS320C40TABL60	5 V ± 5%	60 MHz	325 ILB/OLB TAB tape (encapsulated)	Commercial (No Burn-In)

SMJ320C40 device nomenclature



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