REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																			
SHEET																			
REV																			
SHEET	15	16	17	18	19	20	21	22											

REV STATUS OF SHEETS	REV														
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
95-02-10

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL, CMOS, QUAD ELECTRICALLY ERASABLE PROGRAMMABLE POTENTIOMETER, MONOLITHIC SILICON

SIZE	CAGE CODE	5962-95525
A	67268	

SHEET 1 OF 22

DESC FORM 193
JUL 94

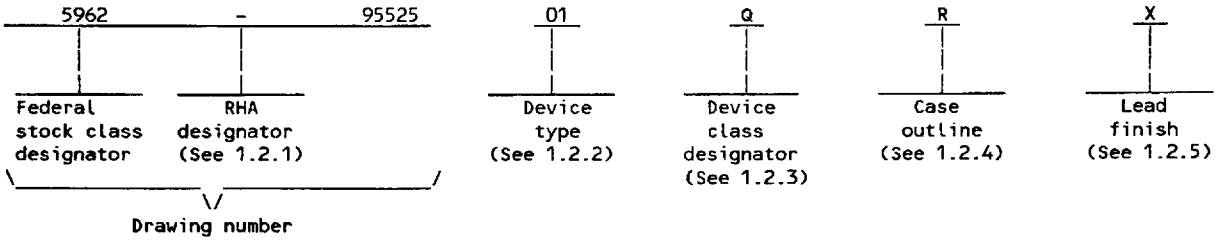
5962-E040-95

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes Q and M) and space application (device class V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device class M RHA marked devices shall meet the MIL-I-38535 appendix A specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number 1/	Circuit function	Potentiometer Organization (ohms) Pot 0	Pot 1	Pot 2	Pot 3	Endurance (writes per register)
01	9241Y	Quad EEPOT	2.0K	2.0K	2.0K	2.0K	100,000
02	9241W	Quad EEPOT	10K	10K	10K	10K	100,000
03	9241U	Quad EEPOT	50K	50K	50K	50K	100,000
04	9241M	Quad EEPOT	2.0K	10K	10K	50K	100,000

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
R	GDIP1-T20	20	Dual-in-line

1.2.5 Lead finish. The lead finish shall be as specified in MIL-STD-883 (see 3.1 herein) for class M or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1/ Generic numbers are also listed in the Standard Microcircuit Drawing Source Approval Bulletin and in MIL-BUL-103.

1.3 Absolute maximum ratings. 2/

Supply voltage range with respect to ground (V_{CC})	-1.0 V dc to +7.0 V dc
Voltage on SCL, SDA, or A0 - A3 with respect to ground	-1.0 V dc to +7.0 V dc
Voltage on any V_H or V_L pin referenced to ground	±8.0 V dc
Diferential voltage ($\Delta V = V_H - V_L$)	16 V dc
Storage temperature range (T_{stg})	-65°C to +150°C
Maximum power dissipation (P_D)	225 mW
Lead temperature (soldering, 10 seconds)	+300°C
Junction temperature (T_J) 3/	+175°C
Thermal resistance, junction-to-case (Θ_{JC}) (case outline R)	See MIL-STD-1835
Data retention	100 years, minimum
Endurance (all device types)	100,000 writes per register, minimum

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Case operating temperature range (T_C)	-55°C to +125°C
Low level input voltage range (V_{IL})	-1.0 V dc to +0.8 V dc
High level input voltage range (V_{IH})	+2.0 V dc to V_{CC} + 1.0 V dc

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	XX percent 4/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, bulletin, and handbook. Unless otherwise specified, the following specification, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standard Microcircuit Drawings (SMD's).

2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
3/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.
4/ When a Qualified Manufacturers' List (QML) source exists, a value will be provided.

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specification, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

ELECTRONICS INDUSTRIES ASSOCIATION (EIA)

JEDEC Standard No. 17 - A Standardized Test Procedure for the Characterization of LATCH-UP in CMOS Integrated Circuits.

(Applications for copies should be addressed to the Electronic Industries Association, 2001 Pennsylvania Avenue, N.W., Washington, DC 20006.)

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM Standard F1192-88 - Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to the American Society for Testing and Materials, 1916 Race Street, Philadelphia, Pennsylvania 19103).

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Block diagram. The block diagram shall be as specified on figure 3.

3.2.5 Switching test circuits and waveforms. The switching test circuits and waveforms shall be as specified on figure 4.

3.2.5.1 Unprogrammed devices. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 2 herein. When required, in screening (see 4.2 herein), or quality conformance inspection groups A, B, C, or D (see 4.4 herein), the devices shall be programmed by the manufacturer prior to test in a checkerboard or similar pattern (a minimum of 50 percent of the total number of bits programmed).

3.2.5.2 Programmed devices. The requirements for supplying programmed devices are not part of this document.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.2 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.1 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 42 (see MIL-I-38535, appendix A).

3.11 Processing of EEPOTs. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.11.1 Conditions of the supplied devices. Devices will be supplied in an unprogrammed or clear state. No provision will be made for supplying programmed devices.

3.11.2 Erasure of EEPOTs. When specified, devices shall be erased in accordance with procedures and characteristics specified in 4.5.1.

3.11.3 Programming of EEPOTs. When specified, devices shall be programmed in accordance with procedures and characteristics specified in 4.5.2.

3.11.4 Verification of state of EEPROMs. When specified, devices shall be verified as either written to the specified pattern or cleared. As a minimum, verification shall consist of performing a read of the entire memory array to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure and the device shall be removed from the lot or sample.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Units
					Min	Max	
V_{CC} supply current, active	I_{CC}	f_{SCL} = 100 KHz, SDA = open, all other inputs = GND	1, 2, 3	All		3.0	mA
V_{CC} supply current, standby	I_{SB}	SCL = SDA = V_{CC}, A0 - A3 = GND	1, 2, 3	All		500	µA
Input leakage current	I_{LI}	V_{IN} = GND to V_{CC}	1, 2, 3	All		10	µA
Output leakage current	I_{LO}	V_{OUT} = GND to V_{CC}	1, 2, 3	All		10	µA
High level input voltage	V_{IH}		1, 2, 3	All	2.0	V_{CC}+1.0 1/	V
Low level input voltage	V_{IL}		1, 2, 3	All	-1.0 1/	0.8	V
Low level output voltage	V_{OL}	I_{OL} = 3.0 mA	1, 2, 3	All		0.4	V
Input/output capacitance (SDA)	$C_{I/O}$	$V_{I/O}$ = 0 V, T_A = +25°C, see 4.4.1b	4	All		8.0	pF
Input capacitance	C_{IN}	V_{IN} = 0 V, T_A = +25°C, see 4.4.1b	4	All		6.0	pF
End to end resistance tolerance	R_{E-E}		4, 5, 6	All	-20	+20	%
Power rating, each potentiometer 2/	P_{IN}	T_A = +25°C	4	All		50	mW
Wiper current	I_W		4, 5, 6	All	-1.0	+1.0	mA
Wiper resistance	R_W	I_W = ±1.0 mA	4, 5, 6	All		100	Ω
Voltage on any V_H or V_L pin	V_{TERM}		4, 5, 6	All	-5.0	+5.0	V
Noise figure 3/	NF	V_{REF} = 1.0 V	4, 5, 6	All		≤120	dB/√Hz
Resolution 1/	RES	Individual array resolution	4, 5, 6	All		1.6	%
		All four arrays cascaded together				0.4	
Absolute linearity, each potentiometer 4/	AL	$V_{W(n)(actual)} - V_{W(n)(expected)}$	4, 5, 6	All	-1.0	+1.0	MI 5/
Relative linearity, each potentiometer 6/	RL	$V_{W(n+1)} - [V_{W(n)} + MI]$ 5/	4, 5, 6	All	-0.2	+0.2	MI 5/

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Units
					Min	Max	
Temperature coefficient of resistance 3/	TC_R		4, 5, 6	All		±300	ppm/°C
Functional tests		see 4.4.1c	7, 8A, 8B	All			
Power-up to initiation of read operation 3/ 7/	t_{PUR}	C_L = 100 pF, see figure 4	9, 10, 11	All		1.0	ms
Power-up to initiation of write operation 3/ 7/	t_{PUW}		9, 10, 11	All		5.0	ms
SCL clock frequency	f_{SCL}		9, 10, 11	All	0 1/	100	KHz
Noise suppression time constant (glitch filter) 1/	t_{NSTC}	C_L = 100 pF, see figure 4	9, 10, 11	All		100	ns
Clock low period	t_{LOW}		9, 10, 11	All	4700		ns
Clock high period	t_{HIGH}		9, 10, 11	All	4000		ns
SCL and SDA rise time 1/	t_R		9, 10, 11	All		1000	ns
SCL and SDA fall time 1/	t_F		9, 10, 11	All		300	ns
Start condition setup time (for a repeated start condition)	t_{SUSTA}		9, 10, 11	All	4700		ns
Start condition hold time	t_{HDSTA}		9, 10, 11	All	4000		ns
Data in setup time	t_{SUDAT}		9, 10, 11	All	250		ns
Data in hold time	t_{HDDAT}		9, 10, 11	All	0		ns
SCL low to SDA data out valid 1/	t_{AA}		9, 10, 11	All	300	3500	ns
Data out hold time	t_{DH}		9, 10, 11	All	300		ns
Stop condition setup time	t_{SUSTO}		9, 10, 11	All	4700		ns
Bus free time prior to new transmission 1/	t_{BUF}		9, 10, 11	All	4700		ns
Write cycle time (nonvolatile write operation)	t_{WR}		9, 10, 11	All		10	ms

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Units
					Min	Max	
Wiper response time from stop generation	t_{STPWV}	C_L = 100 pF, see figure 4	9, 10, 11	All		500	µs
Wiper response from clock low	t_{CLWV}		9, 10, 11	All		1	ms

1/ V_{IL} (min), V_{IH} (max), RES, f_{SCL} (min), t_{NSTC}, t_R, t_F, t_{AA} (min), and t_{BUF}, are for reference only and are not tested.
2/ If not tested, shall be guaranteed to the limits specified in table I.
3/ Parameters shall be tested as part of device initial characterization and after design and process change. Parameters shall be guaranteed to the limits of table I for all lots not specifically tested.
4/ Absolute linearity is utilized to determine actual wiper voltage versus expected voltage as determined by wiper position when used as a potentiometer.
5/ MI = $R_{TOT}/63$ or $(V_H - V_L)/63$, single pot.
6/ Relative linearity is utilized to determine the actual change in voltage between two successive tap positions when used as a potentiometer. It is a measure of the error in step size.
7/ t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated.

Device type	All
Case outline	R
Terminal number	Terminal symbol
1	V_{WO}
2	V_{LO}
3	V_{HO}
4	A0
5	A2
6	V_{W1}
7	V_{L1}
8	V_{H1}
9	SDA
10	V_{SS}
11	V_{H2}
12	V_{L2}
13	V_{W2}
14	SCL
15	A3
16	A1
17	V_{H3}
18	V_{L3}
19	V_{W3}
20	V_{CC}

FIGURE 1. Terminal connections.

Instruction	Instruction format								Operation
	I_3	I_2	I_1	I_0	P_1	P_0	R_1	R_0	
Read WCR	1	0	0	1	1/0	1/0	N/A	N/A	Read the contents of the wiper counter register pointed to by P_1 - P_0
Write WCR	1	0	1	0	1/0	1/0	N/A	N/A	Write new value to the wiper counter register pointed to by P_1 - P_0
Read data register	1	0	1	1	1/0	1/0	1/0	1/0	Read the contents of the register pointed to by P_1 - P_0 and R_1 - R_0
Write data register	1	1	0	0	1/0	1/0	1/0	1/0	Write new value to the register pointed to by P_1 - P_0 and R_1 - R_0
XFR data register to WCR	1	1	0	1	1/0	1/0	1/0	1/0	Transfer the contents of the WCR pointed to by P_1 - P_0 and R_1 - R_0 to it's associated WCR
XFR WCR to data register	1	1	1	0	1/0	1/0	1/0	1/0	Transfer the contents of the WCR pointed to by P_1 - P_0 to the register pointed to by R_1 - R_0
Global XFR data register to WCR	0	0	0	1	N/A	N/A	1/0	1/0	Transfer the contents of all four data registers pointed to by R_1 - R_0 to their respective WCR
Global XFR WCR to data register	1	0	0	0	N/A	N/A	1/0	1/0	Transfer the contents of all WCR's to their respective data registers pointed to by R_1 - R_0
Increment/decrement wiper	0	0	1	0	1/0	1/0	N/A	N/A	Enable increment/decrement of the WCR pointed to by P_1 - P_0

1 = Logic "1" voltage level
0 = Logic "0" voltage level
1/0 = Logic "1" or logic "0" voltage level
N/A = Not applicable or don't care; that is, a data register is not involved in the operation and need not be addressed

FIGURE 2. Truth table.

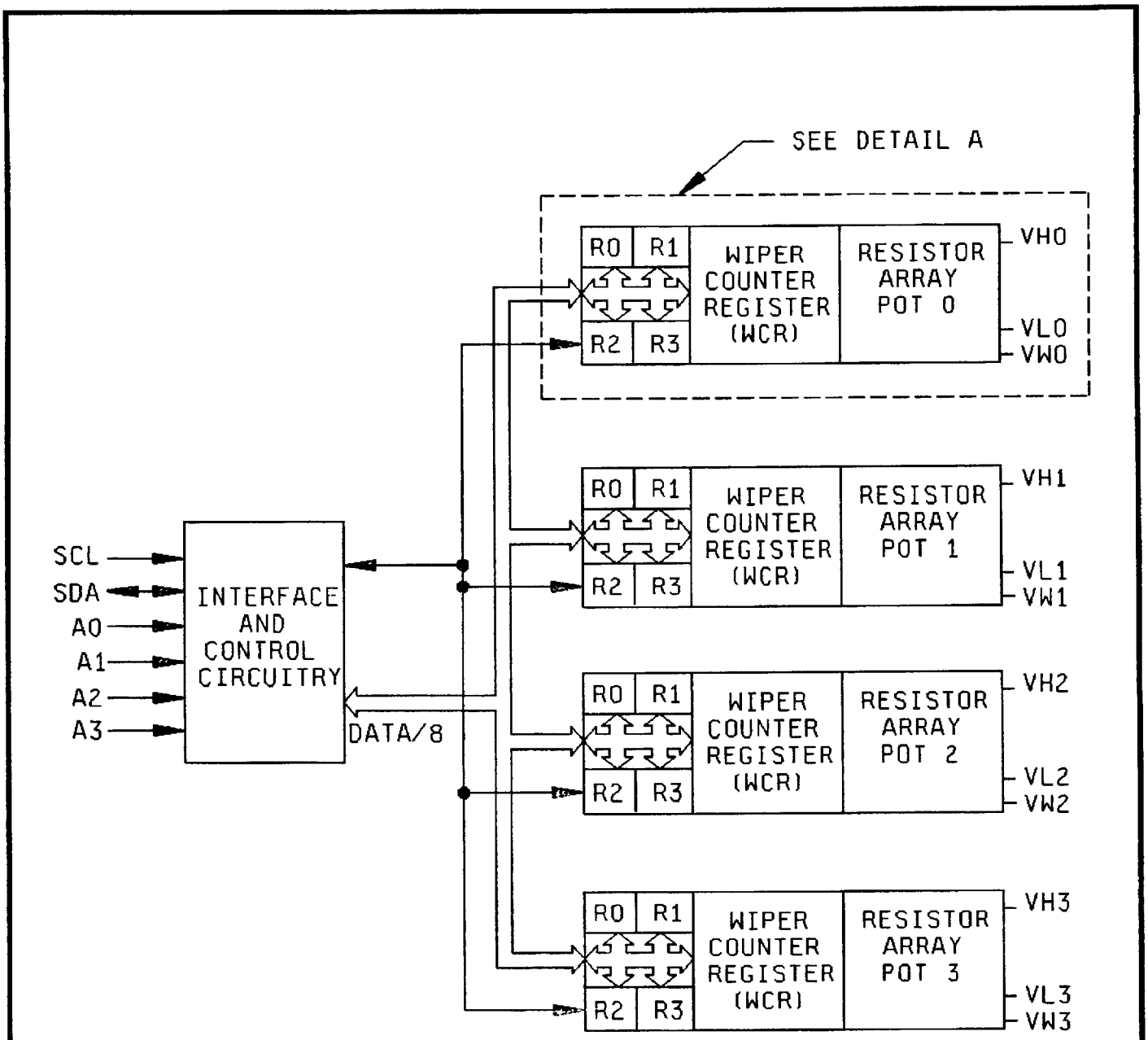
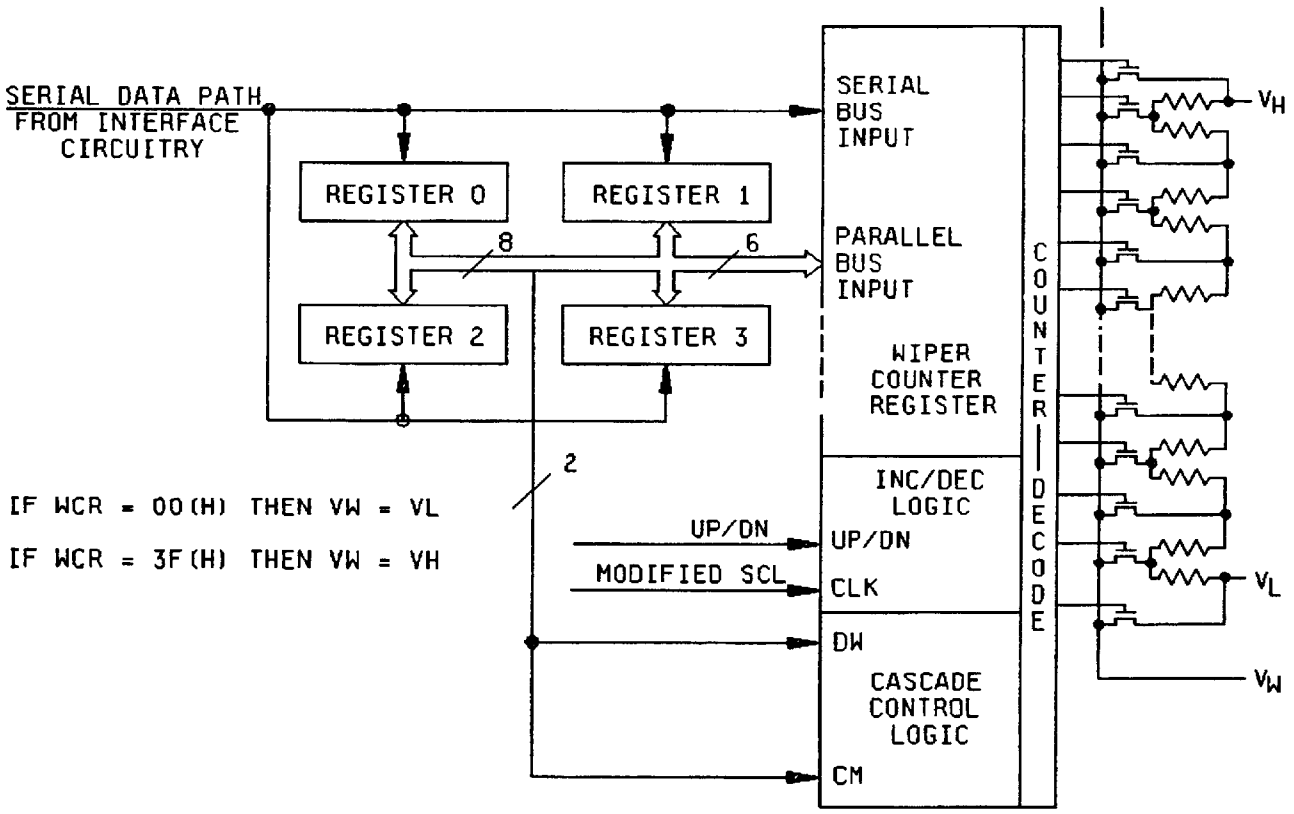


FIGURE 3. Block diagram.

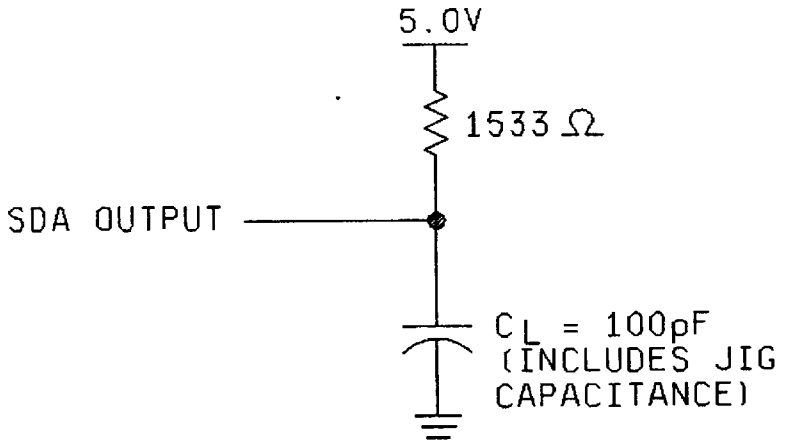


DETAIL A

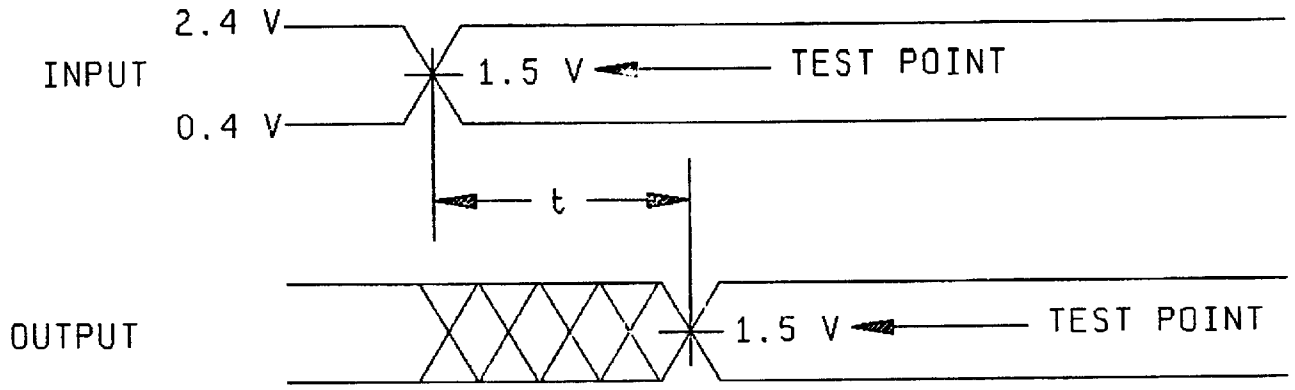
DETAILED POTENTIOMETER BLOCK DIAGRAM
1 OF 4 POTENTIOMETERS SHOWN

FIGURE 3. Block diagram - continued.

SWITCHING TEST CIRCUIT (OR EQUIVALENT)



INPUT/OUTPUT TIMING LEVELS



AC testing: Inputs are driven at 2.4 V for a logic "1" and 0.4 V for a logic "0". Input pulse rise and fall times are ≤ 10 ns.

FIGURE 4. Switching test circuit and waveforms.

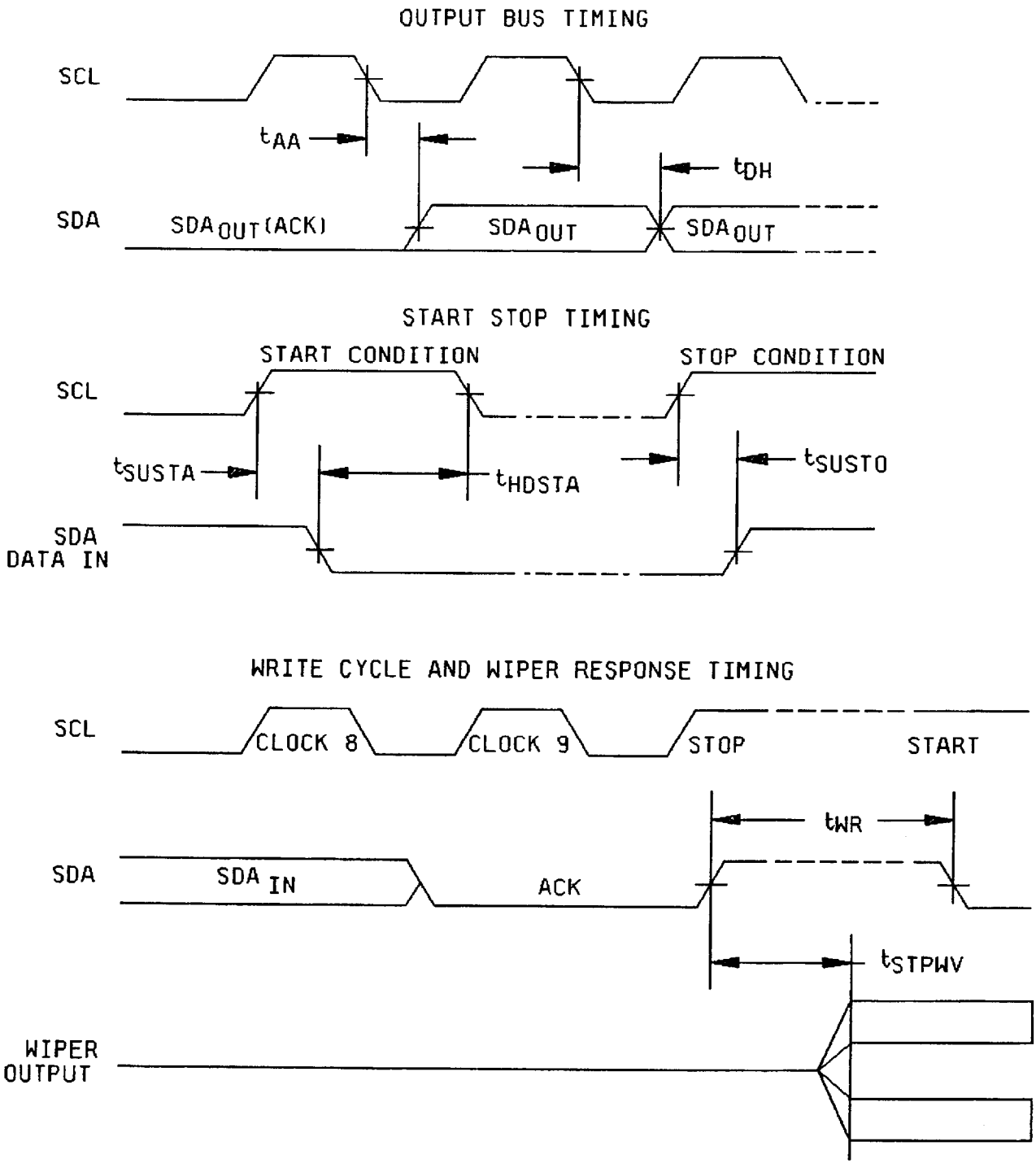
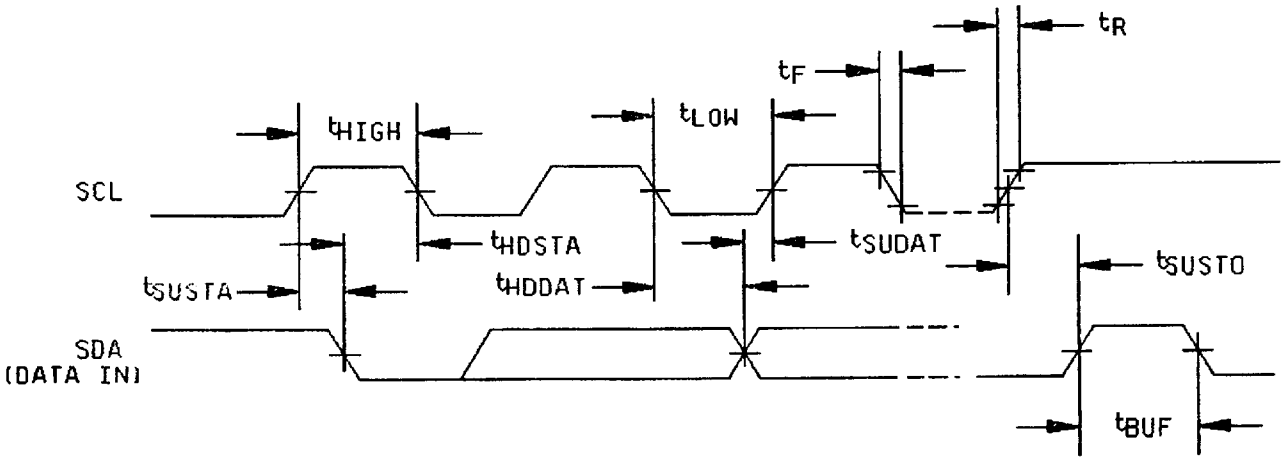


FIGURE 4. Switching test circuit and waveforms - Continued.

INPUT BUS TIMING



INCREMENT/DECREMENT TIMING LIMITS

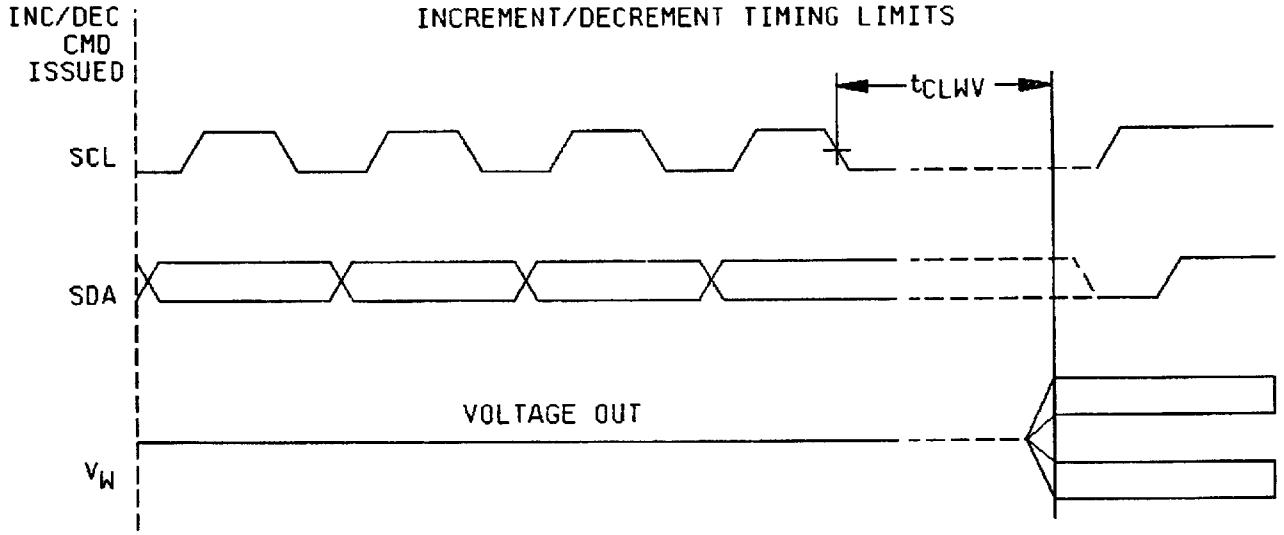


FIGURE 4. Switching test circuit and waveforms - Continued.

3.12 Endurance. A reprogrammability test shall be completed as part of the vendor's reliability monitors. This reprogrammability test shall be done for initial characterization and after any design or process changes which may affect the reprogrammability of the device. The methods and procedures may be vendor specific, but shall guarantee the number of program/erase endurance cycles listed in section 1.3 herein over the full military temperature range. The vendor's procedure shall be kept under document control and shall be made available upon request of the acquiring or preparing activity, along with test data.

3.13 Data retention. A data retention stress test shall be completed as part of the vendor's reliability monitors. This test shall be done for initial characterization and after any design or process change which may affect data retention. The methods and procedures may be vendor specific, but shall guarantee the number of years listed in section 1.3 herein over the full military temperature range. The vendor's procedure shall be kept under document control and shall be made available upon request of the acquiring or preparing activity, along with test data.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein). For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device class M.

a. Delete the sequence specified as initial (preburn-in) electrical parameters through interim (postburn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table IIA herein.

b. Prior to burn-in, the devices shall be programmed (see 4.5.2 herein) with a checkerboard pattern or equivalent (manufacturers at their option may employ an equivalent pattern provided it is a topologically true alternating bit pattern). The pattern shall be read before and after burn-in. Devices having bits not in the proper state after burn-in shall constitute a device failure and shall be included in the PDA calculation and shall be removed from the lot.

c. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(1) Dynamic burn-in (method 1015 of MIL-STD-883, test condition D) using the circuit referenced (see 4.2.1c herein).

d. Interim and final electrical parameters shall be as specified in table IIA herein.

e. After the completion of all screening, the device shall be erased and verified prior to delivery.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535 and as detailed in table IIA herein.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroup 4 (C_{IN} and $C_{I/O}$ measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 15 devices with no failures and all input and output terminals tested.

c. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

d. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device class M, procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes Q and V, performance of O/V (latch-up) testing shall be as specified in the manufacturer's QM plan, the procedures and circuits shall be under the control of the device manufacturer's TRB in accordance with MIL-I-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JEDEC Standard number 17 may be used for reference.

e. All devices selected for testing shall be programmed with a checkerboard pattern or equivalent. After completion of all testing, the devices shall be erased and verified, (except devices submitted for groups C and D testing and devices to be archived, i.e., devices not to be sold).

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein. Delta limits shall apply only to subgroup 1 of group C and shall consist of test specified in table IIB herein.

TABLE IIA. Elecrtical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line no.	Test requirements	Subgroups (per method 5005, table I)	Subgroups (per MIL-I-38535, table III)	
		Device class M	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)			1,7,9
2	Static burn-in I method 1015	Not required	Not required	Not required
3	Same as line 1			1*,7* Δ
4	Dynamic burn-in (method 1015)	Required	Required	Required
5	Same as line 1			1*,7* Δ
6	Final electrical parameters	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9,10, 11
7	Group A test requirements	1,2,3,4**,7, 8A,8B,9,10, 11	1,2,3,4**,7, 8A,8B,9,10, 11	1,2,3,4**,7, 8A,8B,9,10, 11
8	Group C end-point electrical parameters	2,3,7, 8A,8B	1,2,3,7, 8A,8B	1,2,3,7, 8A,8B,9,10, 11 Δ
9	Group D end-point electrical parameters	2,3,8A,8B	2,3,8A,8B	2,3,8A,8B
10	Group E end-point electrical parameters	1,7,9	1,7,9	1,7,9

1/ Blank spaces indicate test are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7, 8A, and 8B functional tests shall verify the truth table.
4/ * Indicates PDA applies to subgroups 1 and 7.
5/ ** See 4.4.1b.
6/ Δ Indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1). For device class V, performance of delta tests and limits shall be as specified in the manufacturer's QM plan.
7/ See 4.4.1d.

4.4.2.1 Additional criteria for device class M.

a. Steady-state life test conditions, method 1005 of MIL-STD-883:

(1) The device selected for testing shall be programmed with a checkerboard pattern or equivalent.

(2) Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

(3) T_A = +125°C, minimum.

(4) Test duration: 1,000 hours, except as specified in method 1005 of MIL-STD-883.

b. All devices requiring end-point electrical testing shall be programmed with a checkerboard or equivalent alternating bit pattern.

c. After the completion of all testing, the devices shall be cleared and verified prior to delivery (except devices submitted for group D testing and devices to be archived, i.e., devices not to be sold).

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-I-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein. The devices selected for testing shall be programmed with a checkerboard pattern or equivalent. After completion of all testing, the devices shall be erased and verified (except devices to be archived, i.e., devices not to be sold).

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes Q and V shall be M, D, L, R, F, G, and H and for device class M shall be M and D.

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-I-38535, appendix A, for the RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-I-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

TABLE IIB. Delta limits at 25°C.

Test 1/	All device types
I_{SB}	±10 percent of specified value in table I.
I_{LI}	±10 percent of specified value in table I.
I_{LO}	±10 percent of specified value in table I.

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine delta.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate figures and tables herein.

4.5.1 Erasing procedures. The erasing procedures shall be as specified by the device manufacturer and shall be available upon request.

4.5.2 Programming procedure. The programming procedures shall be as specified by the device manufacturer and shall be made available upon request.

4.6 Delta measurements for device class V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter tests, subgroups 1, 7, and 9.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444, or telephone (513) 296-5377.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-I-38535 and MIL-STD-1331.

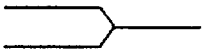
AL	Absolute linearity,
C_{IN}	Input capacitance
$C_{I/O}$	Input/output capacitance each potentiometer
C_L	Load capacitance
f_{SCL}	SCL clock frequency
I_{CC}	V_{CC} supply current, active
I_{LI}	Input leakage current
I_{LO}	Output leakage current
I_{OL}	Low level output current
I_{SB}	V_{CC} supply current, standby
I_W	Wiper current
NF	Noise figure
P_{IN}	Power rating, each potentiometer
R_{E-E}	End to end resistance tolerance
RES	Resolution
RL	Relative linearity, each potentiometer
R_W	Wiper resistance

6.5 Abbreviations, symbols, and definitions - continued.

t_A	Ambient temperature
t_{AA}	SCL low to SDA data out valid
t_{BUF}	Bus free time prior to new transmission
T_C	Case temperature
t_{CLWV}	Wiper response from clock low
TC_R	Temperature coefficient of resistance
t_{DH}	Data out hold time
t_F	SCL and SDA fall time
t_{HDDAT}	Data in hold time
t_{HDSTA}	Start condition hold time
t_{HIGH}	Clock high period
t_{LOW}	Clock low period
t_{NSTC}	Noise suppression time constant (glitch filter)
t_{PUR}	Power-up to initiation of read operation
t_{PUW}	Power-up to initiation of write operation
t_R	SCL and SDA rise time
T_{stg}	Storage temperature
t_{STPWV}	Wiper response time from stop generation
t_{SUDAT}	Data in setup time
t_{SUSTA}	Start condition setup time (for a repeated start condition)
t_{SUSTO}	Stop condition setup time
t_{WR}	Write cycle time (nonvolatile write operation)
V_{CC}	V_{CC} supply voltage
V_H, V_L	Equivalent to the terminal connections on either end of a mechanical potentiometer
V_{IH}	High level input voltage
V_{IL}	Low level input voltage
V_{IN}	Input voltage
$V_{I/O}$	Input/output voltage
V_{OL}	Low level output voltage
V_{REF}	Reference voltage
V_{SS}	V_{SS} supply voltage
V_{TERM}	Voltage on any V_H or V_L pin
V_W	Equivalent to the wiper output of a mechanical potentiometer
ΔV	Differential voltage

6.5.1 Timing limits. The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

6.5.2 Waveforms.

WAVEFORM SYMBOL	INPUT	OUTPUT
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WIIL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
		HIGH IMPEDANCE

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the three major microcircuit requirements documents (MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The three military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all three documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-H-38534 Standard Microcircuit Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standard Microcircuit Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standard Microcircuit Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.