REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																				
SHEET																				
REV																				
SHEET	15	16																		

REV STATUS OF SHEETS	REV														
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
96-03-27

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, LINEAR, 8-CHANNEL, 12-BIT SERIAL, DATA ACQUISITION SYSTEM, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-95615

SHEET 1 OF 16

DESC FORM 193
JUL 94

9004708 0020549 726

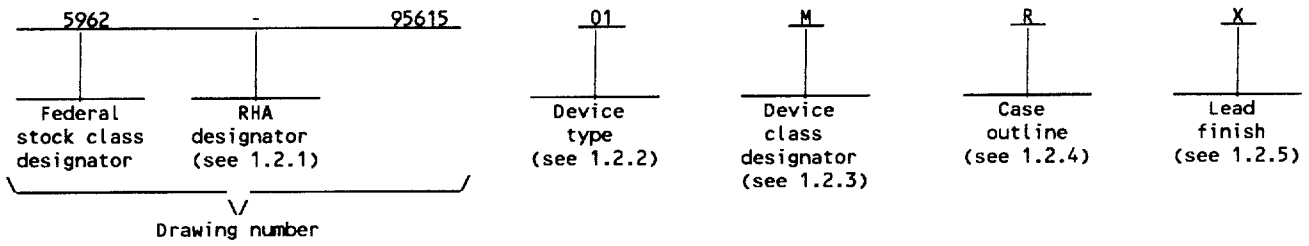
5962-E078-96

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes Q and M) and space application (device class V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device class M RHA marked devices shall meet the MIL-I-38535 appendix A specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	AD7890-10	8-Channel, 12-Bit Serial, Data Acquisition System

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
J	GDIP1-T24 or CDIP2-T24	24	Dual-in-line

1.2.5 Lead finish. The lead finish shall be as specified in MIL-STD-883 (see 3.1 herein) for class M or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 1/

V_{DD} to AGND	-0.3 V dc to +7 V dc
V_{DD} to DGND	-0.3 V dc to +7 V dc
Analog input voltage to AGND	±17 V dc
Reference input voltage to AGND	-0.3 V dc to V_{DD} + 0.3 V dc
Digital input voltage to DGND	-0.3 V dc to V_{DD} + 0.3 V dc
Digital output voltage to DGND	-0.3 V dc to V_{DD} + 0.3 V dc
Junction temperature (T_J)	+150°C
Power dissipation (P_D)	450 mW
Thermal resistance, junction-to-ambient (θ_{JA})	70°C/W
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Lead temperature (soldering, 10 secs)	+300°C

1.4 Recommended operating conditions.

Ambient operating temperature range	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, bulletin, and handbook. Unless otherwise specified, the following specification, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standard Microcircuit Drawings (SMD's).

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specification, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit, or function as described herein.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Ideal input/output code table(s). The ideal input/output code table(s) shall be as specified on figure 2.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.2 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.1 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M, the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 81 (see MIL-I-38535, appendix A).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Signal to noise + distortion ratio	SNR	f_{IN} = 10 kHz sine wave, f_{SAMPLE} = 100 kHz	1, 2, 3	01	70		dB
Total harmonic distortion	THD	f_{IN} = 10 kHz sine wave, f_{SAMPLE} = 100 kHz	1, 2, 3	01		77	dB
Peak harmonic or spurious noise	PHN	f_{IN} = 10 kHz sine wave, f_{SAMPLE} = 100 kHz	1, 2, 3	01		78	dB
Channel-to-channel isolation	CI	f_{IN} = 1 kHz sine wave, V_{DD} = +4.75 V dc	1, 2, 3	01		80	dB
Resolution	RES		1, 2, 3	01		12	Bits
Minimum resolution for which no missing codes are guaranteed	MRES		1, 2, 3	01		12	Bits
Relative accuracy	RA		1, 2, 3	01		±1	LSB
Differential nonlinearity	DNL		1, 2, 3	01		±1	LSB
Positive full-scale error	PFSE		1, 2, 3	01		±2.5	LSB
Full-scale error match 2/	FSE		1, 2, 3	01		2	LSB
Negative full-scale error	NFSE	V_{DD} = +4.75 V dc	1, 2, 3	01		±2	LSB
Bipolar zero error	BZE		1, 2, 3	01		±4	LSB
Bipolar zero error match	BZEM		1, 2, 3	01		2	LSB
Input voltage range	V_{IN}		1, 2, 3	01	-10	+10	V
Input resistance	R_{IN}		1, 2, 3	01	20		kΩ
Mux out output voltage range	V_{OUT}		1, 2, 3	01	0	2.5	V

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Mux out output resistance	R_{OUT}		1, 2, 3	01	3	5	kΩ
SHA IN input voltage range	V_{SIN}		1, 2, 3	01	0	2.5	V
SHA IN input current	I_{SIN}	V_{SIN} = 2.49 V	1, 2, 3	01	-50	+50	nA
REF IN input voltage range	V_{RIN}		1, 2, 3	01	2.375	2.625	V
Input impedance	R_{RIN}	Resistor connected to internal reference node	1, 2, 3	01	1.6	1.6	kΩ
REF OUT output voltage	V_{ROUT}		1, 2, 3	01		2.5	V
REF OUT error	ROE		1 2, 3	01	-10 -25	+10 +25	mV
Logic input high voltage	V_{INH}	V_{DD} = 5 V ± 5%	1, 2, 3	01	2.4		V
Input low voltage	V_{INL}	V_{DD} = 5 V ± 5%	1, 2, 3	01		0.8	V
Input current	I_{IN}	V_{IN} = 0 V to V_{DD}	1, 2, 3	01	-10	+10	µA
Output high voltage	V_{OH}	I_{SOURCE} = 200 µA	1, 2, 3	01	4		V
Output low voltage	V_{OH}	I_{SINK} = 1.6 mA	1, 2, 3	01		0.4	V
Conversion time 3/	t_{CONV}	f_{CLKIN} = 2.5 MHz, V_{DD} = 4.75 V, MUX OUT connected to SHA IN	9, 10, 11	01		5.9	µs
Supply voltage	V_{DD}	±5% for specified performance	1, 2, 3	01		5	V
Supply current 4/	I_{DD}	Logic inputs = 0 V or V_{DD}	1, 2, 3	01		10	mA
Power dissipation	P_D		1, 2, 3	01		50	mW

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/, 3/, 5/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Master clock frequency 6/	f_{CLKIN}		9, 10, 11	01	0.1	2.5	MHz
Master clock input low time	t_{CLKINL}		9, 10, 11	01	0.3 x t_{CLKIN}		ns
Master clock input high time	t_{CLKINH}		9, 10, 11	01	0.3 x t_{CLKIN}		ns
Digital output rise time 7/	t_R		9, 10, 11	01		25	ns
Digital output fall time 7/	t_F		9, 10, 11	01		25	ns
Conversion time	$t_{CONVERT}$		9, 10, 11	01		5.9	µs
$\overline{\text{CONVST}}$ pulse width	t_{CST}		9, 10, 11	01	100		ns
$\overline{\text{RFS}}$ low to SCLK falling edge	t_1		9, 10, 11	01		t_{CLKINH} + 50	ns
$\overline{\text{RFS}}$ low to data valid delay 8/	t_2		9, 10, 11	01		25	ns
SCLK high pulse width	t_3		9, 10, 11	01		t_{CLKINH}	ns
SCLK low pulse width	t_4		9, 10, 11	01		t_{CLKINL}	ns
SCLK rising edge to data valid delay 8/	t_5		9, 10, 11	01		20	ns
SCLK rising edge to $\overline{\text{RFS}}$ delay	t_6		9, 10, 11	01		40	ns
Bus relinquish time after rising edge of SCLK 9/	t_7		9, 10, 11	01		50	ns
$\overline{\text{TFS}}$ low to SCLK falling edge	t_8		9, 10, 11	01	0	t_{CLKIN} +50	ns
Data valid to TFS falling edge setup time (A2 address bit)	t_9		9, 10, 11	01	0		ns
Data valid to SCLK falling edge setup time	t_{10}		9, 10, 11	01	20		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/, 3/, 5/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Data valid to SCLK falling edge hold time	t_{11}		9, 10, 11	01	10		ns
$\overline{\text{TFS}}$ to SCLK falling edge hold time	t_{12}		9, 10, 11	01	20		ns
$\overline{\text{RFS}}$ low to SCLK falling edge setup time	t_{13}		9, 10, 11	01	20		ns
$\overline{\text{RFS}}$ low to data valid delay 8/	t_{14}		9, 10, 11	01		40	ns
SCLK high pulse width	t_{15}		9, 10, 11	01	50		ns
SCLK low pulse width	t_{16}		9, 10, 11	01	50		ns
SCLK rising edge to data valid delay 8/	t_{17}		9, 10, 11	01		35	ns
$\overline{\text{RFS}}$ to SCLK falling edge hold time	t_{18}		9, 10, 11	01	20		ns
Bus relinquish time after rising edge of $\overline{\text{RFS}}$	t_{19}		9, 10, 11	01		50	ns
Bus relinquish time after rising edge of SCLK 9/	t_{19A}		9, 10, 11	01		90	ns
$\overline{\text{TFS}}$ low to SCLK falling edge setup time	t_{20}		9, 10, 11	01	20		ns
Data valid to SCLK falling edge setup time	t_{21}		9, 10, 11	01	10		ns
Data valid to SCLK falling edge hold time	t_{22}		9, 10, 11	01	15		ns
$\overline{\text{TFS}}$ to SCLK falling edge hold time	t_{23}		9, 10, 11	01	40		ns

1/ V_{DD} = +5.25 V, AGND = DGND = 0 V, REF IN = +2.5 V, $f_{CLK\ IN}$ = 2.5 MHz external, MUX OUT connected to SHA IN.
2/ Full-scale error match applied to both positive and negative full scale.
3/ Subgroups 9, 10, and 11 are tested initially and after any changes which may affect these parameters. See figures 3 and 4.
4/ Analog inputs must be at 0 V to achieve correct power-down current.
5/ All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V. Tested initially and after any design changes which may affect these parameters.
6/ Production tested with f_{CLKIN} at 2.5 MHz. It is guaranteed by characterization to operate at 100 kHz.
7/ Specified using 10% and 90% points on waveform of interest.
8/ These numbers are measured with the load circuit of Figure 3 and defined as the time required for the output to cross 0.8 V or 2.4 V.
9/ These numbers are derived from the measured time taken by the data output to change 0.5 V when loaded with the circuit of Figure 3. The measured number is then extrapolated back to remove effects of charging or discharging the 50 pF capacitor. This means that the times quoted in the timing characteristics are the true bus relinquish times of the part and as such are independent of external bus loading capacitances.

Device type	01
Case outlines	J and X
Terminal number	Terminal symbols
1	AGND
2	SMODE
3	DGND
4	C_{EXT}
5	$\overline{CONVST}$
6	CLK IN
7	SCLK
8	$\overline{TFS}$
9	$\overline{RFS}$
10	DATA OUT
11	DATA IN
12	V_{DD}
13	MUX OUT
14	SHA IN
15	AGND
16	V_{IN1}
17	V_{IN2}
18	V_{IN3}
19	V_{IN4}
20	V_{IN5}
21	V_{IN6}
22	V_{IN7}
23	V_{IN8}
24	REF OUT/REF IN

FIGURE 1. Terminal connections.

Analog input	Digital output code transition
+FSR/2 - 1 LSB (9.995117 V)	011 ... 110 to 011 ... 111
+FSR/2 - 2 LSBs (9.990234 V)	011 ... 101 to 011 ... 110
+FSR/2 - 3 LSBs (9.985352 V)	011 ... 100 to 011 ... 101
AGND + 1 LSB (0.004883 V)	000 ... 000 to 000 ... 000
AGND (0.000000 V)	111 ... 111 to 000 ... 000
AGND - 1 LSB (-0.004883 V)	111 ... 110 to 111 ... 111
-FSR/2 + 3 LSBs (-9.985352 V)	100 ... 010 to 100 ... 011
-FSR/3 + 2 LSBs (-9.990234 V)	100 ... 001 to 100 ... 010
-FSR/2 + 1 LSB (-9.995117 V)	100 ... 000 to 000 ... 000

FIGURE 2. Ideal in/output code tables.

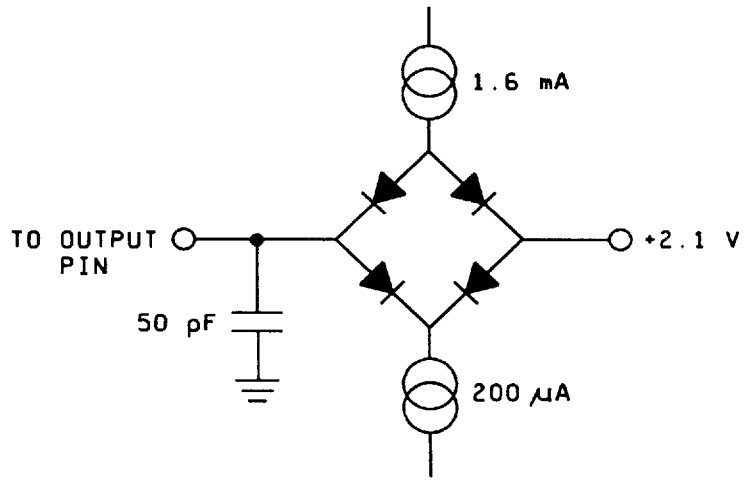
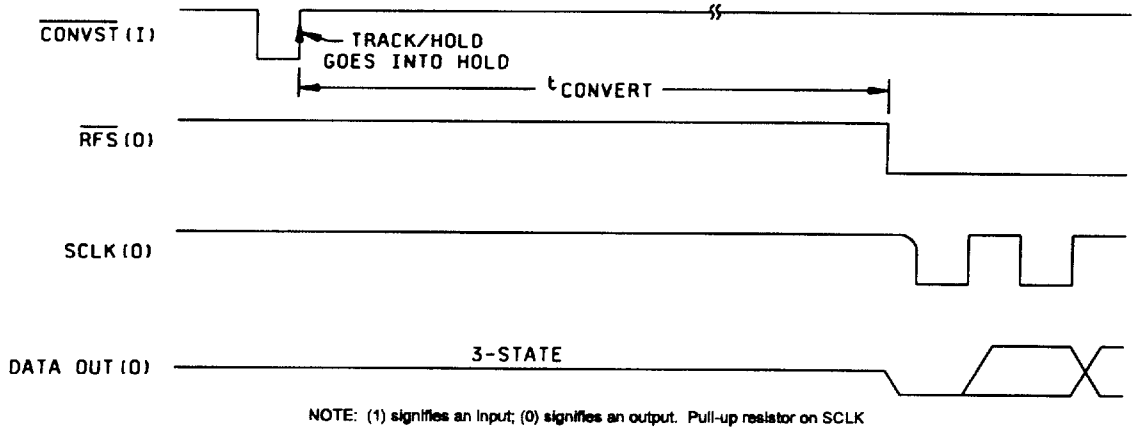
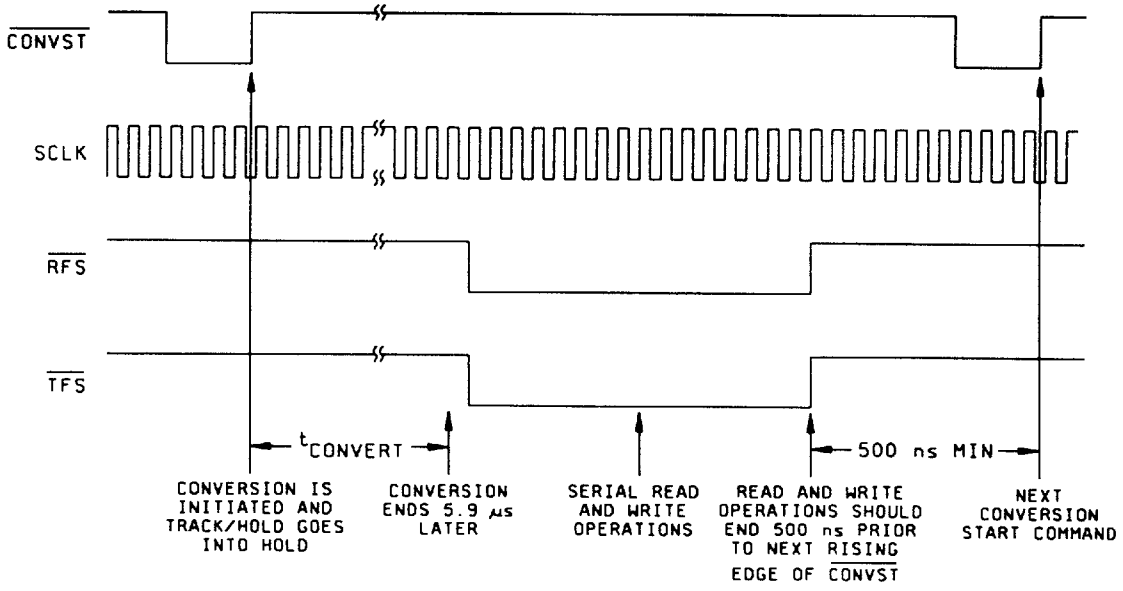


FIGURE 3. Load circuit for access time and bus relinquish time.



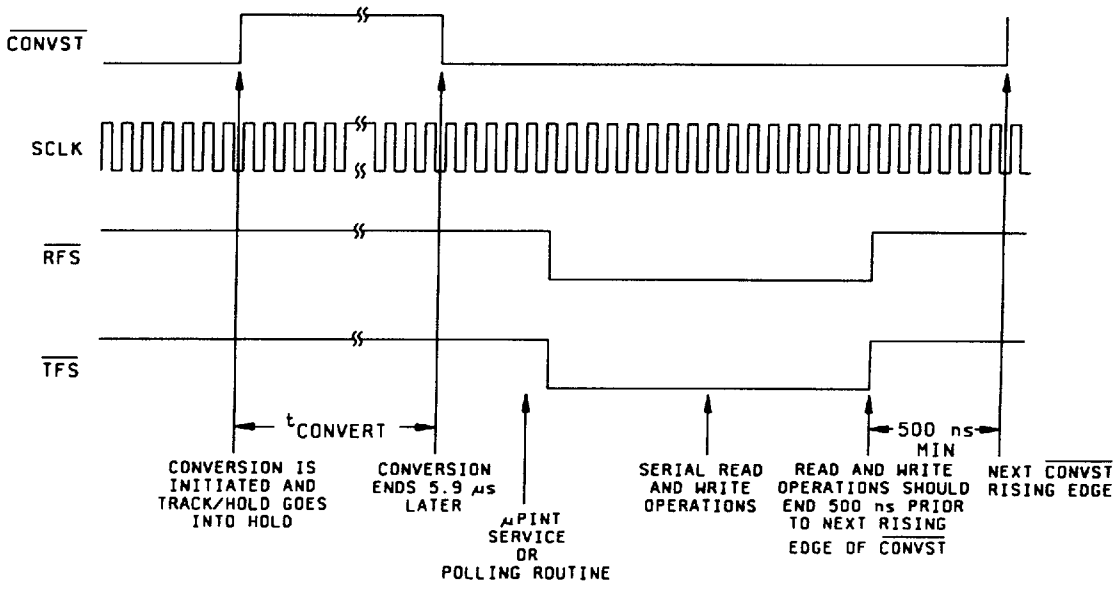
NOTE: (1) signifies an input; (0) signifies an output. Pull-up resistor on SCLK

SELF-CLOCKING (MASTER) MODE CONVERSION SEQUENCE

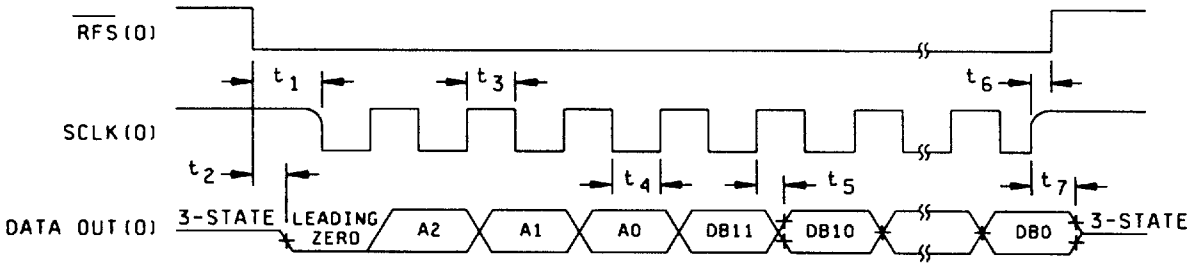


EXTERNAL CLOCKING (SLAVE) MODE TIMING SEQUENCE FOR OPTIMUM PERFORMANCE

FIGURE 4. Timing waveforms.



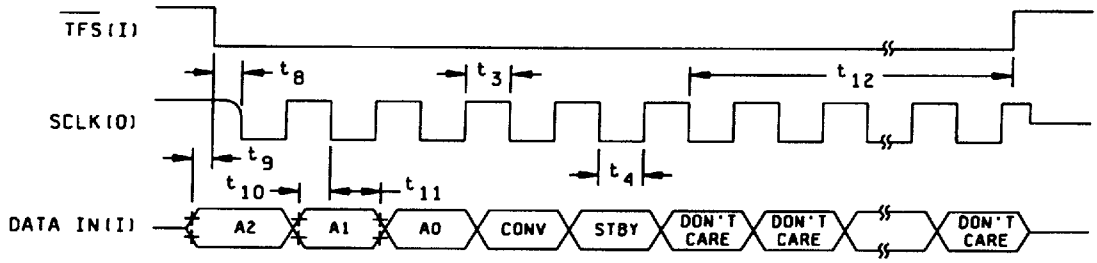
CONVST USED STATUS SIGNAL IN EXTERNAL CLOCKING MODE



NOTE: (1) signifies an input; (0) signifies an output. Pull-up resistor on SCLK

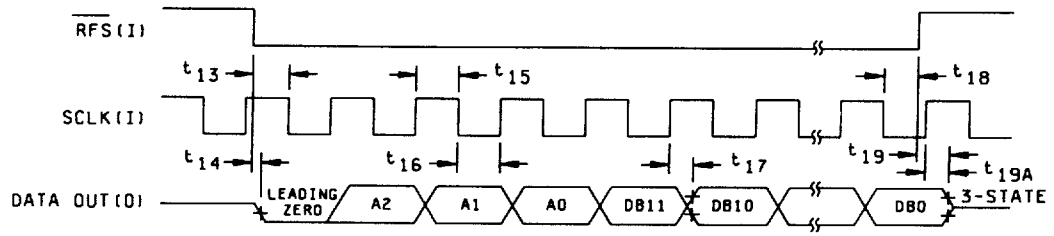
SELF-CLOCKING (MASTER) MODE OUTPUT REGISTER READ

FIGURE 4. Timing waveforms - continued.



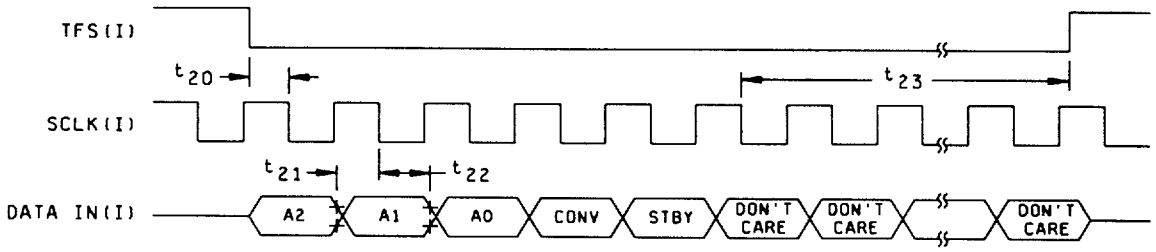
NOTE: (1) signifies an input; (0) siignifies an output. Pull-up resistor on SCLK.

SELF-CLOCKING (MASTER) MODE CONTROL REGISTER WRITE



NOTE: (1) signifies an input; (0) signifies an output .

EXTERNAL CLOCKING (SLAVE) MODE OUTPUT REGISTER READ



NOTE: (1) signifies an input; (0) signifies an output.

EXTERNAL CLOCKING (SLAVE) MODE CONTROL REGISTER WRITE

FIGURE 4. Timing waveforms - continued.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein). For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit, or function as described herein.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, D, or E. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, 6, 7, and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 9, 10, and 11 are tested initially and after any design changes which may affect the parameters in these subgroups.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, TM 5005, table I)	Subgroups (in accordance with MIL-I-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1, 2, 3	1, 2, 3	1, 2, 3
Final electriacl parameters (see 4.2)	1, 2, 3, 1/ 2/ 9, 10, 11	1, 2, 3, 1/ 9, 10, 11 2/	1, 2, 3, 1/ 9, 10, 11 2/
Group A test requirements (see 4.4)	1, 2, 3, 2/ 9, 10, 11	1, 2, 3, 2/ 9, 10, 11	1, 2, 3, 2/ 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3
Group E end-point electrical parameters (see 4.4)	---	---	---

1/ PDA applies to subgroup 1.
2/ Subgroups 9, 10, 11 are tested initially and after any design changes which may affect the parameters in those subgroups.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, D, or E. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-I-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes Q and V shall be M, D, L, R, F, G, and H and for device class M shall be M and D.

a. End-point electrical parameters shall be as specified in table II herein.

b. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-I-38535, appendix A, for the RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-I-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444-5270, or telephone (513) 296-5377.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-I-38535 and MIL-STD-1331.

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the three major microcircuit requirements documents (MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The three military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all three documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-H-38534 Standard Microcircuit Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standard Microcircuit Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standard Microcircuit Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.