T-42-31

FEATURES

- All devices use an advanced, small geometry process resulting in smaller chip size, increased complexity, and higher frequency (ft 800MHz). All devices operate from 1 to 20 volts despite their smaller size.
- You will find the 700 Series the easiest to route of all the semicustom chips on the market. Twenty years of experience and attention to detail have resulted in an architecture which allows nearly 100% of the components to be used.
- Thin film resistors and second level metal can be added on each chip. No space has to be reserved (and wasted) to make these options possible.
- All critical components, such as resistors and small transistors have identical size and identical orientation for the best possible matching.
- Large 200 mA transistors, 6 mA PNP transistors and Schottky diodes are available.
- Most transistors are multipurpose, they can be NPN or PNP with no degradation in performance.
- You can perform design analysis and layout entirely on a Personal Computer. The required software programs are proven and inexpensive.
- The ECI 700 Series Design Manual contains models and patterns with complete device information and an easy introduction to linear design.

THE CHIP SERIES

There are eight chips in the 700 Series. The smallest one fits into any surface-mounted package. The remaining seven chips form a smooth progression in size; each chip is approximately 30% larger in area than the next smaller one.

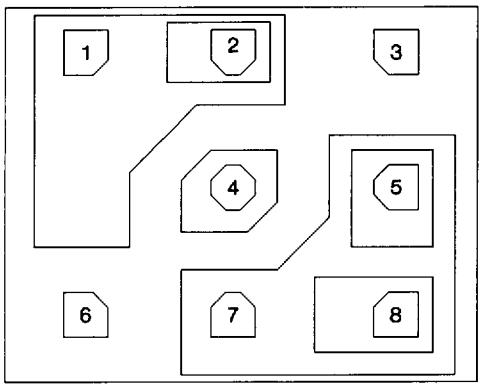
Each chip contains the same basic components and is based on an identical architecture. In the center portion of the chips are islands of 12 transistors each, 10 of which are convertible from NPN to PNP and 2 are Schottky NPN transistors. These islands are surrounded by a field of resistors. The number of resistors and the total resistance is extra large, which makes it easier to design an IC, especially for a first-time design.

Between the bonding pads along the periphery are all other devices: large (200mA) NPN transistors, large (6mA) PNP transistors, pinch (high-value) resistors and junction capacitors. Sprinkled throughout each chip are low-value cross-under resistors.

Chip Series	710	712	713	723	724	734	736	747
Die Size mils	33 x 33	47 x 53	53 x 66	70 x 66	74 x 79	98 x 79	98 x 105	118 x 119
Die Size square mils	1089	2491	3498	4620	5846	7742	10290	14042
Pads	4	17	22	25	30	30	41	48
Dual NPN/PNP Transistors	14	27	39	60	80	120	180	280
Schottky NPN Transistors	4	10	11	12	16	24	36	56
Large NPN Transistors	1	1	2	3	4	9	5	9
Large PNP Transistors	0	1	2	3	3	6	4	5
Total Transistors	33	66	93	143	183	279	405	630
750 Ohm Resistors	120	214	412	635	900	1270	1735	2400
Total Base Resistance	90k	160k	310k	475k	675k	950k	1.3M	1.8M
Base Pinch Resistors	2	9	9	8	11	8	14	16
Epi Pinch Resistors	1	2	2	2	2	2	2	2
Junction Capacitors	1	2	4	7	7	9	12	10
Cross-Unders	40	70	160	200	300	450	650	950

COMPONENTS

The basic transistor in the 700 Series has three modes of operation, NPN transistor, lateral PNP transistor, and substrate PNP transistor.



Pin Function

1. NPN Base, PNP Collector
2. NPN Emitter
3. NPN Collector, PNP Base
4. PNP Emitter
5. NPN Emitter
6. NPN Collector, PNP Base
7. NPN Base, PNP Collector
8. NPN Emitter

NPN Transistor

As an NPN transistor there are two separate bases and three emitters which you can use individually or together.

Current gain = 100 to 300 (Figure 1)
ft = 800MHz
Maximum current = 24mA (8mA per emitter)

The base emitter junction of the NPN transistor makes an excellent 5.9 volt zener diode with near zero temperature coefficient.

Lateral PNP Transistor

As a lateral PNP transistor there are two isolated collectors splitting the current accurately 1:1.

Current gain = 40 to 90 (Figure 2)
ft = 15MHz
Maximum current = 300uA

Substrate PNP Transistor

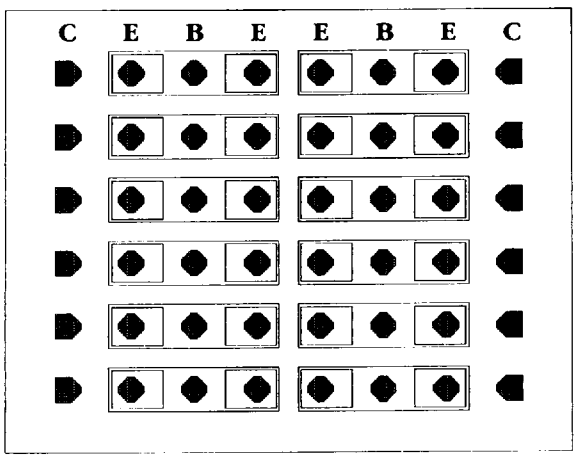
The substrate transistor is formed tying the collector to the most negative voltage. The design of this transistor allows for several leads to cross over it. All devices have identical orientation for optimum matching.

Current gain = 30 to 75
ft = 15MHz
Maximum current = 1 mA

Large NPN Transistors

Large NPN transistors contain 24 emitters identical to those of the small device. The 24 identical emitters provide 200mA, a substantial amount of current, and are very useful to create current ratios anywhere between 1 and 24.

Current gain = 100 to 300 (Figure 3)
ft = 400MHz
Current = 8mA per emitter
Maximum current = 200mA



Large PNP Transistors

Large lateral PNP transistors are provided to steer the large NPN device for high current outputs.

Current gain = 40 to 90 (Figure 4)
ft = 15MHz
Maximum current = 6mA

Resistors

For optimum matching a single base value of 750 ohms is used. There are 2400 resistors available on the largest chip. You may connect this 750 ohm resistor value in series or parallel to obtain any value between 50 ohms and 100Kohms or more. (Figure 6)

Schottky Diode

Some of the small transistors contain a Schottky diode which has a small forward drop of 300mV to 400mV. (Figure 5)

NPN Transistor

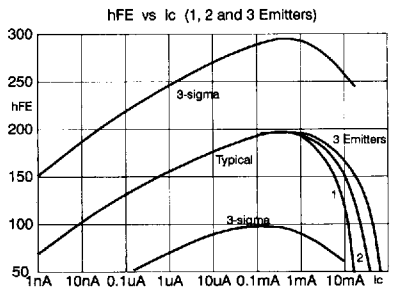


Figure 1

PNP Transistor

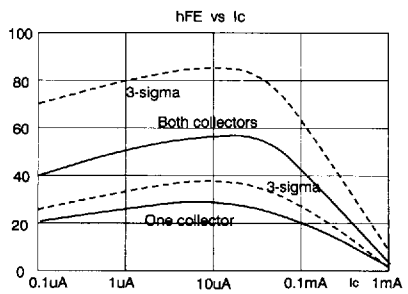


Figure 2

Large NPN Transistor

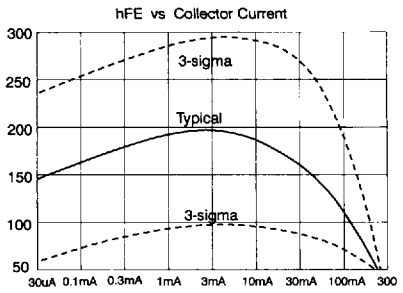


Figure 3

Large PNP Transistor

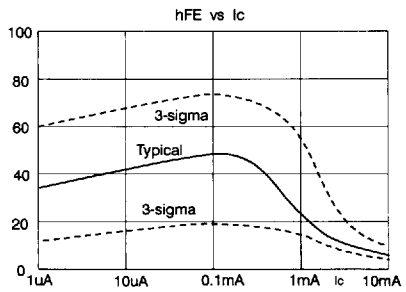


Figure 4

Schottky Diode

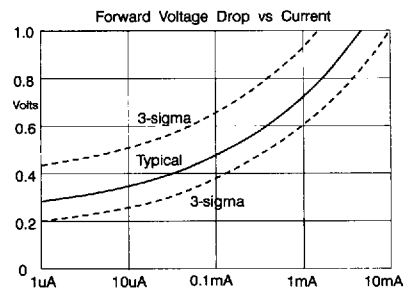


Figure 5

Resistor

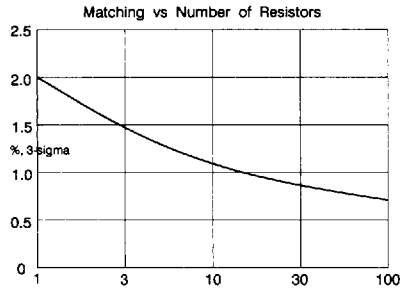


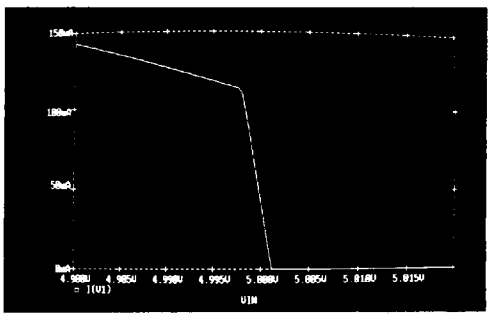
Figure 6

700 SERIES, A COMPARISON WITH GEC PLESSEY CHIPS

	713	MMA	747	MMF
Die Dimensions, mils	53 x 66	56 x 69	118 x 119	109 x 133
Die Area, mils²	3498	3864	14042	14495
Small Transistors	50	40	336	168
Large NPN Transistors	2(0.2A)	1(0.1A)	9(0.2A)	8(0.1A)
Large PNP Transistors	1	0	5	0
Base Resistance	310k	93k	1.8M	610k
Pads	22	14	48	30
Capacitors	4	1	10	3
20 Volt Pinch Resistors	2	1	2	1
5 Volt Pinch Resistors	9	2	16	16
Schottky Diodes	11	0	56	0
Cross-Unders	160	50	950	224

DESIGN AND ANALYSIS

We have spent more than a year putting together the device models for the 700 Series; an accurate model is what makes computer analysis work. We compared them against breadboards and even integrated test circuits to make sure they have no flaws.



You can plug these models into Spice and simulate all or part of your circuit before you commit to integration. We even added the important parameter variations so you can perform a Monte Carlo analysis and find out how well your IC will yield in production. The models come on a disk, which is part of the design manual.

Spice can be used for DC, AC and Transient analysis. It also has some handy features which show you the behavior of your circuit over temperature. The design manual gives you advice and examples on how to best use Spice for linear ICs.

ECI

LAYOUT

We have put the 700 Series on ICED, by far the best PC-based layout program available. ICED is inexpensive and easy to use. Just call up the chip-size you want and start interconnecting the devices with a mouse. You can do this in one or two metal layers and even add custom thin-film resistors.

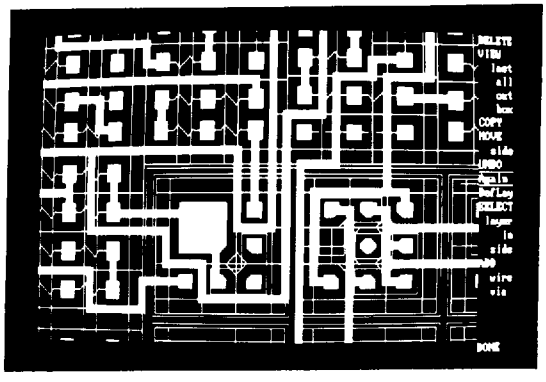
A disk in the design manual contains all the chip patterns. We have removed the layers which are not going to be changed and added routing channels so you always know where you can place an interconnection stripe and where you can't. No need to be familiar with IC processing.

ICED has plotter and printer outputs so you can have a permanent record. Once you are satisfied with the layout it produces a stream-file from which the mask is made.

ICED also has an optional Design Rule Checker (DRC) which makes sure your lines have the proper spacing and will soon add a program which compares your layout with the schematic (LVS).

If you prefer to do your layout with pencil and paper, we have large (300X), colored layout sheets.

If you have another layout program ECI can provide streamfiles for use on your system.



THE DESIGN MANUAL

1. Semicustom Chips - the concept - comparison with full custom and standard cells.
2. How These Chips Are Made - a detailed explanation of the process.
3. Devices - data and parameter curves for all devices.
4. The 700 Chips - data on the chips and a component count.
5. Linear IC Design - an introduction to the principles and elements of linear IC design. This chapter will be gradually enlarged with examples on disks, free to registered manual owners.
6. Breadboarding - the available kit-parts.
7. Computer Simulation - examples using PSpice - device models.
8. Layout - how to use ICED - layout hints - chip patterns.
9. Packaging - commonly available packages - how to make a bonding diagram.
10. Making Prototypes and Production Parts - how to have a mask made and wafers patterned - interfacing with your foundry - Wafer specifications and the test pattern - the Mask Protection Act.

Order Information

700 Series Design Manual	
U.S., shipped first-class mail or UPS	$60.00
U.S., shipped FEDEX	$75.00
Outside U.S., airmail	$70.00
Outside U.S., FEDEX	$85.00

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