National Semiconductor

September 1995

# 74ABT2541
# Octal Buffer/Line Driver with 25Ω Series Resistors in the Outputs

## General Description

The 'ABT2541 is an octal buffer and line driver designed to drive the capacitive inputs of MOS memory drivers, address drivers, clock drivers, and bus-oriented transmitters/receivers. Functionally identical to the 'ABT541.

The 25Ω series resistors in the outputs reduce ringing and eliminate the need for external resistors.

## Features

- Guaranteed output skew
- Guaranteed multiple output switching specifications
- Output switching specified for both 50 pF and 250 pF loads
- Guaranteed simultaneously switching noise level and dynamic threshold performance
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Nondestructive hot insertion capability
- Disable time less than enable time to avoid bus contention

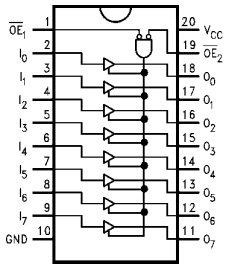
| Commercial | Package Number | Package Description |
|---|---|---|
| 74ABT2541CSC (Note 1) | M20B | 20-Lead (0.300″ Wide) Molded Small Outline, JEDEC |
| 74ABT2541CSJ (Note 1) | M20D | 20-Lead (0.300″ Wide) Molded Small Outline, EIAJ |
| 74ABT2541CMSA (Note 1) | MSA20 | 20-Lead Molded Shrink Small Outline, EIAJ Type II |
| 74ABT2541CMTC (Notes 1, 2) | MTC20 | 20-Lead Molded Thin Shrink Small Outline, JEDEC |

**Note 1:** Devices also available in 13″ reel. Use suffix = SCX, SJX, MSAX and MTCX.

**Note 2:** Contact factory for package availability.

## Connection Diagram

**Pin Assignment for SOIC and SSOP**

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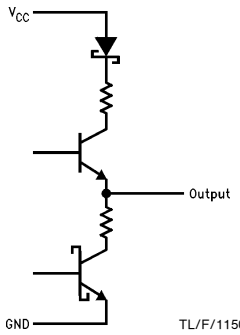
**Schematic of Each Output**

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## Truth Table

| Inputs | | | Outputs |
|---|---|---|---|
| $\overline{OE}_1$ | $\overline{OE}_2$ | I | ABT2541C |
| L | L | H | H |
| H | X | X | Z |
| X | H | X | Z |
| L | L | L | L |

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

| Pin Names | Description |
|---|---|
| $\overline{OE}_1$, $\overline{OE}_2$ | Output Enable Input (Active Low) |
| $I_0$–$I_7$ | Inputs |
| $O_0$–$O_7$ | Outputs |

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## Absolute Maximum Ratings (Note 1)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Ambient Temperature under Bias | −55°C to +125°C |
| Junction Temperature under Bias | |
| Plastic | −55°C to +150°C |
| $V_{CC}$ Pin Potential to Ground Pin | −0.5V to +7.0V |
| Input Voltage (Note 2) | −0.5V to +7.0V |
| Input Current (Note 2) | −30 mA to +5.0 mA |
| Voltage Applied to Any Output | |
| in the Disabled or Power-off State | −0.5V to 5.5V |
| in the HIGH State | −0.5V to $V_{CC}$ |
| Current Applied to Output in LOW State (Max) | twice the rated $I_{OL}$ (mA) |
| DC Latchup Source Current | −500 mA |
| Over Voltage Latchup (I/O) | 10V |

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

## Recommended Operating Conditions

| | |
|---|---|
| Free Air Ambient Temperature | |
| Commercial | −40°C to +85°C |
| Supply Voltage | |
| Commercial | +4.5V to +5.5V |
| Minimum Input Edge Rate | (ΔV/Δt) |
| Data Input | 50 mV/ns |
| Enable Input | 20 mV/ns |

## DC Electrical Characteristics

| Symbol | Parameter | | ABT2541 Min | ABT2541 Typ | ABT2541 Max | Units | $V_{CC}$ | Conditions |
|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | | 2.0 | | | V | | Recognized HIGH Signal |
| $V_{IL}$ | Input LOW Voltage | | | | 0.8 | V | | Recognized LOW Signal |
| $V_{CD}$ | Input Clamp Diode Voltage | | | | −1.2 | V | Min | $I_{IN}$ = −18 mA |
| $V_{OH}$ | Output HIGH Voltage | 74ABT | 2.5 | | | V | Min | $I_{OH}$ = −3 mA |
| | | 74ABT | 2.0 | | | V | Min | $I_{OH}$ = −32 mA |
| $V_{OL}$ | Output LOW Voltage | 74ABT | | | 0.8 | V | Min | $I_{OL}$ = 15 mA |
| $I_{IH}$ | Input HIGH Current | | | | 5<br>5 | μA | Max | $V_{IN}$ = 2.7V (Note 2)<br>$V_{IN}$ = $V_{CC}$ |
| $I_{BVI}$ | Input HIGH Current Breakdown Test | | | | 7 | μA | Max | $V_{IN}$ = 7.0V |
| $I_{IL}$ | Input LOW Current | | | | −5<br>−5 | μA | Max | $V_{IN}$ = 0.5V (Note 2)<br>$V_{IN}$ = 0.0V |
| $V_{ID}$ | Input Leakage Test | | 4.75 | | | V | 0.0 | $I_{ID}$ = 1.9 μA<br>All Other Pins Grounded |
| $I_{OZH}$ | Output Leakage Current | | | | 50 | μA | 0 − 5.5V | $V_{OUT}$ = 2.7V; $\overline{OE}_n$ = 2.0V |
| $I_{OZL}$ | Output Leakage Current | | | | −50 | μA | 0 − 5.5V | $V_{OUT}$ = 0.5V; $\overline{OE}_n$ = 2.0V |
| $I_{OS}$ | Output Short-Circuit Current | | −100 | | −275 | mA | Max | $V_{OUT}$ = 0.0V |
| $I_{CEX}$ | Output High Leakage Current | | | | 50 | μA | Max | $V_{OUT}$ = $V_{CC}$ |
| $I_{ZZ}$ | Bus Drainage Test | | | | 100 | μA | 0.0 | $V_{OUT}$ = 5.5V; All Others GND |
| $I_{CCH}$ | Power Supply Current | | | | 50 | μA | Max | All Outputs HIGH |
| $I_{CCL}$ | Power Supply Current | | | | 30 | mA | Max | All Outputs LOW |
| $I_{CCZ}$ | Power Supply Current | | | | 50 | μA | Max | $\overline{OE}_n$ = $V_{CC}$;<br>All Others at $V_{CC}$ or GND |
| $I_{CCT}$ | Additional $I_{CC}$/Input | Outputs Enabled<br>Outputs TRI-STATE®<br>Outputs TRI-STATE | | | 2.5<br>2.5<br>50 | mA<br>mA<br>μA | Max | $V_I$ = $V_{CC}$ − 2.1V<br>Enable Input $V_I$ = $V_{CC}$ − 2.1V<br>Data Input $V_I$ = $V_{CC}$ − 2.1V<br>All Others at $V_{CC}$ or GND |
| $I_{CCD}$ | Dynamic $I_{CC}$ (Note 2) | No Load | | | 0.1 | mA/MHz | Max | Outputs Open<br>$\overline{OE}_n$ = GND (Note 1)<br>One Bit Toggling, 50% Duty Cycle |

**Note 1:** For 8 bit toggling, $I_{CCD}$ < 0.8 mA/MHz.

**Note 2:** Guaranteed, but not tested.

## DC Electrical Characteristics (SOIC package) (Continued)

| Symbol | Parameter | Min | Typ | Max | Units | $V_{CC}$ | Conditions $C_L = 50$ pF, $R_L = 500\Omega$ |
|---|---|---|---|---|---|---|---|
| $V_{OLP}$ | Quiet Output Maximum Dynamic $V_{OL}$ | | 0.6 | 0.8 | V | 5.0 | $T_A = 25°C$ (Note 1) |
| $V_{OLV}$ | Quiet Output Minimum Dynamic $V_{OL}$ | −0.5 | −0.4 | | V | 5.0 | $T_A = 25°C$ (Note 1) |
| $V_{OHV}$ | Minimum High Level Dynamic Output Voltage | 2.7 | 3.1 | | V | 5.0 | $T_A = 25°C$ (Note 3) |
| $V_{IHD}$ | Minimum High Level Dynamic Input Voltage | 2.0 | 1.4 | | V | 5.0 | $T_A = 25°C$ (Note 2) |
| $V_{ILD}$ | Maximum Low Level Dynamic Input Voltage | | 1.2 | 0.8 | V | 5.0 | $T_A = 25°C$ (Note 2) |

**Note 1:** Max number of outputs defined as (n). n-1 data inputs are driven 0V to 3V. One output at LOW. Guaranteed, but not tested.

**Note 2:** Max number of data inputs (n) switching. n-1 inputs switching 0V to 3V. Input-under-test switching: 3V to threshold ($V_{ILD}$), 0V to threshold ($V_{IHD}$). Guaranteed, but not tested.

**Note 3:** Max number of outputs defined as (n). n − 1 data inputs are driven 0V to 3V. One output HIGH. Guaranteed, but not tested.

## AC Electrical Characteristics (SOIC and SSOP package)

| Symbol | Parameter | 74ABT $T_A = +25°C$, $V_{CC} = +5V$, $C_L = 50$ pF | | | 74ABT $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V-5.5V$, $C_L = 50$ pF | | Units |
|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Max | |
| $t_{PLH}$ | Propagation Delay | 1.0 | 2.3 | 3.6 | 1.0 | 3.6 | ns |
| $t_{PHL}$ | Data to Outputs | 1.0 | 3.3 | 4.1 | 1.0 | 4.1 | |
| $t_{PZH}$ | Output Enable Time | 1.5 | 3.7 | 6.0 | 1.5 | 6.0 | ns |
| $t_{PZL}$ | | 1.5 | 4.3 | 6.5 | 1.5 | 6.5 | |
| $t_{PHZ}$ | Output Disable Time | 1.0 | 3.5 | 6.0 | 1.0 | 6.0 | ns |
| $t_{PLZ}$ | | 1.0 | 3.7 | 5.6 | 1.0 | 5.6 | |

## Extended AC Electrical Characteristics (SOIC package)

| Symbol | Parameter | 74ABT $-40°C$ to $+85°C$, $V_{CC} = 4.5V-5.5V$, $C_L = 50$ pF, 8 Outputs Switching (Note 4) | | | 74ABT $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V-5.5V$, $C_L = 250$ pF, 1 Output Switching (Note 5) | | 74ABT $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V-5.5V$, $C_L = 250$ pF, 8 Outputs Switching (Note 6) | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Max | Min | Max | |
| $f_{toggle}$ | Max Toggle Frequency | | 100 | | | | | | MHz |
| $t_{PLH}$ | Propagation Delay | 1.5 | | 5.0 | 1.5 | 6.0 | 2.5 | 8.5 | ns |
| $t_{PHL}$ | Data to Outputs | 1.5 | | 5.5 | 1.5 | 10.0 | 2.5 | 11.0 | |
| $t_{PZH}$ | Output Enable Time | 1.5 | | 6.5 | 2.5 | 7.5 | 2.5 | 9.5 | ns |
| $t_{PZL}$ | | 1.5 | | 7.0 | 2.5 | 11.0 | 2.5 | 12.5 | |
| $t_{PHZ}$ | Output Disable Time | 1.0 | | 6.0 | (Note 7) | | (Note 7) | | ns |
| $t_{PLZ}$ | | 1.0 | | 6.0 | | | | | |

**Note 4:** This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.).

**Note 5:** This specification is guaranteed but not tested. The limits represent propagation delay with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

**Note 6:** This specification is guaranteed but not tested. The limits represent propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.) with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

**Note 7:** The TRI-STATE delays are dominated by the RC network (500Ω, 250 pF) on the output and have been excluded from the datasheet.

## Skew (SOIC package)

| Symbol | Parameter | 74ABT<br>$T_A = -40°C$ to $+85°C$<br>$V_{CC} = 4.5V–5.5V$<br>$C_L = 50$ pF<br>8 Outputs Switching<br>(Note 3) | 74ABT<br>$T_A = -40°C$ to $+85°C$<br>$V_{CC} = 4.5V–5.5V$<br>$C_L = 250$ pF<br>8 Outputs Switching<br>(Note 4) | Units |
|---|---|---|---|---|
| | | Max | Max | |
| $t_{OSHL}$ (Note 1) | Pin to Pin Skew HL Transitions | 1.3 | 2.3 | ns |
| $t_{OSLH}$ (Note 1) | Pin to Pin Skew LH Transitions | 1.0 | 1.8 | ns |
| $t_{PS}$ (Note 5) | Duty Cycle LH–HL Skew | 2.0 | 5.0 | ns |
| $t_{OST}$ (Note 1) | Pin to Pin Skew LH/HL Transitions | 2.0 | 5.0 | ns |
| $t_{PV}$ (Note 2) | Device to Device Skew LH/HL Transitions | 2.0 | 5.0 | ns |

**Note 1:** Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH to LOW ($t_{OSHL}$), LOW to HIGH ($t_{OSLH}$), or any combination switching LOW to HIGH and/or HIGH to LOW ($t_{OST}$). The specification is guaranteed but not tested.

**Note 2:** Propagation delay variation for a given set of conditions (i.e., temperature and $V_{CC}$) from device to device. This specification is guaranteed but not tested.

**Note 3:** This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.)

**Note 4:** These specifications guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

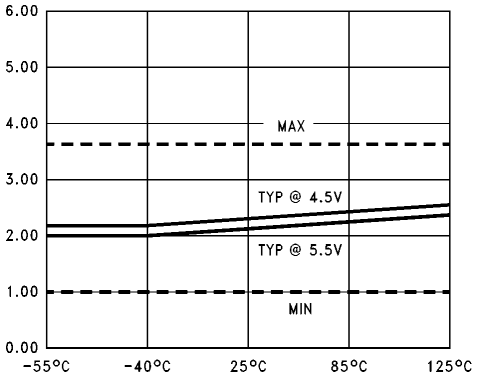
**Note 5:** This describes the difference between the delay of the LOW-to-HIGH and the HIGH-to-LOW transition on the same pin. It is measured across all the outputs (drivers) on the same chip, the worst (largest delta) number is the guaranteed specification. This specification is guaranteed but not tested.

## Capacitance

| Symbol | Parameter | Typ | Units | Conditions<br>$T_A = 25°C$ |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | 5.0 | pF | $V_{CC} = 0V$ |
| $C_{OUT}$ (Note 1) | Output Capacitance | 9.0 | pF | $V_{CC} = 5.0V$ |

**Note 1:** $C_{OUT}$ is measured at frequency f = 1 MHz; per MIL-STD-883B, Method 3012.

**$t_{PLH}$ vs. Temperature ($T_A$)**
**$C_L = 50$ pF, 1 Output Switching**

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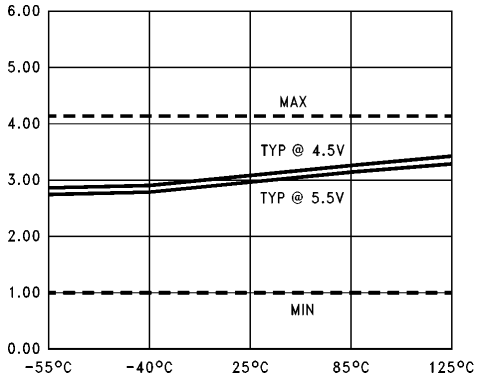
**$t_{PHL}$ vs Temperature ($T_A$)**
**$C_L$ = 50 pF, 1 Output Switching**

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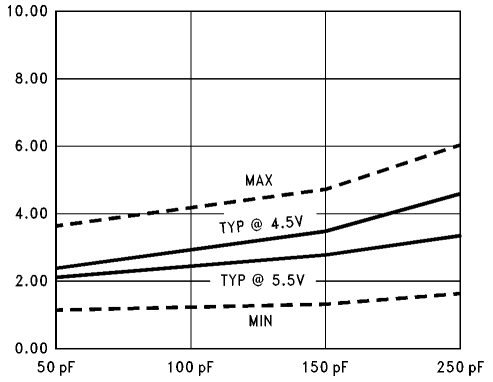
**$t_{PLH}$ vs Load Capacitance**
**1 Output Switching, $T_A$ = 25°C**

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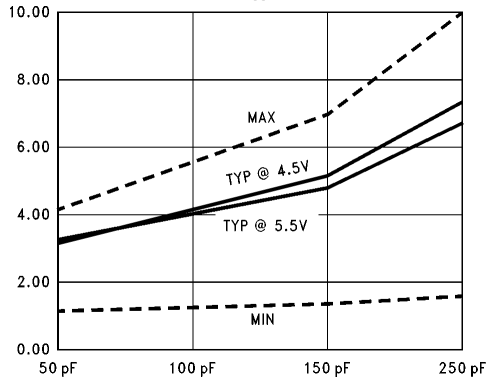
**$t_{PHL}$ vs Load Capacitance**
**1 Output Switching, $T_A$ = 25°C**

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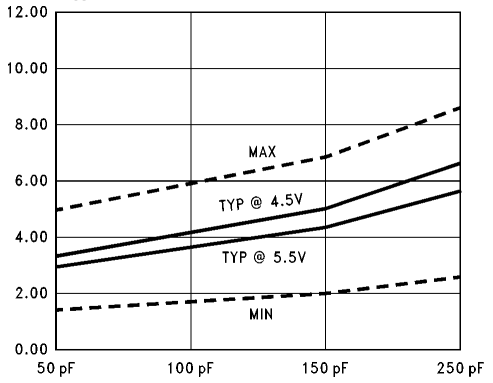
**$t_{PLH}$ vs Load Capacitance**
**8 Outputs Switching,**
**$T_A$ = −40°C to 85°C**

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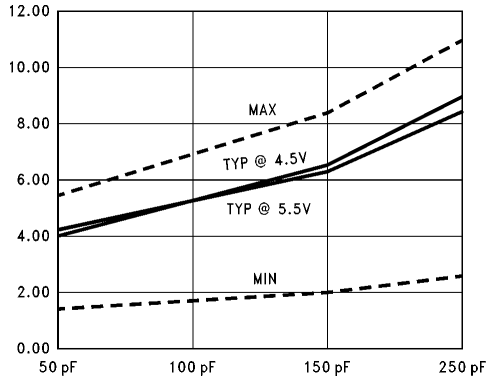
**$t_{PHL}$ vs Load Capacitance**
**8 Outputs Switching, $T_A$ = 25°C**

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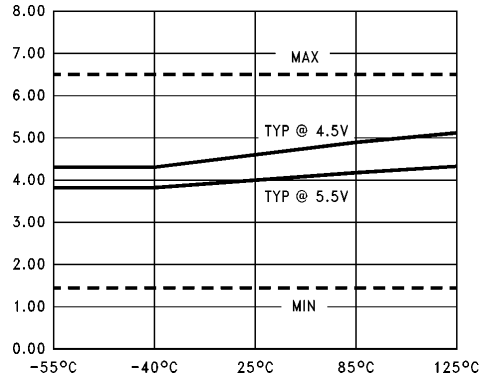
**$t_{PZL}$ vs Temperature ($T_A$)**
**$C_L$ = 50 pF, 1 Output Switching**

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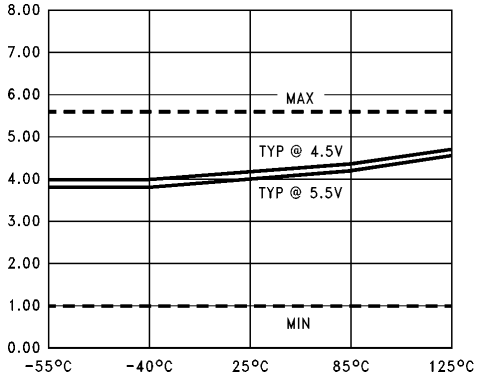
Dashed lines represent design characteristics, for specified guarantees refer to AC Characteristics Table.

**$t_{PLZ}$ vs Temperature ($T_A$)**
**$C_L$ = 50 pF, 1 Output Switching**

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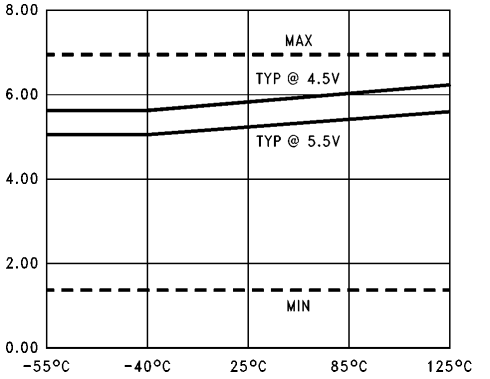
**$t_{PZL}$ vs Temperature ($T_A$)**
**$C_L$ = 50 pF, 8 Outputs Switching**

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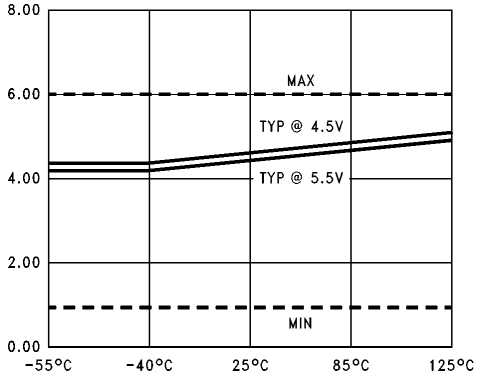
**$t_{PLZ}$ vs Temperature ($T_A$)**
**$C_L$ = 50 pF, 8 Outputs Switching**

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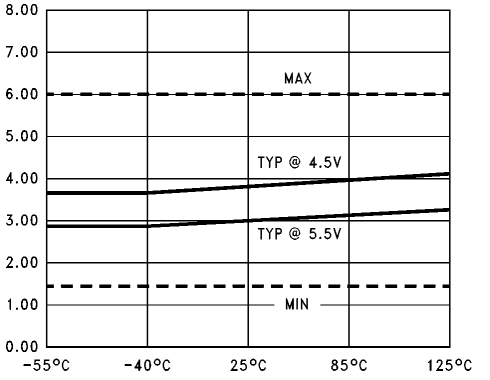
**$t_{PZH}$ vs Temperature ($T_A$)**
**$C_L$ = 50 pF, 1 Output Switching**

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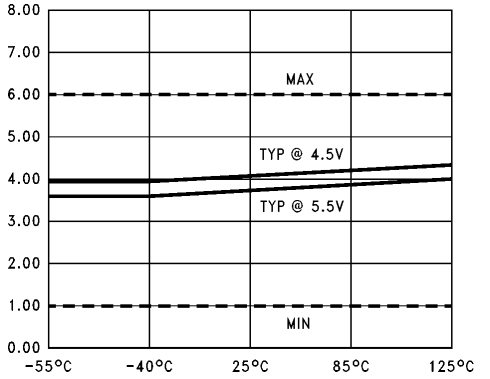
**$t_{PHZ}$ vs Temperature ($T_A$)**
**$C_L$ = 50 pF, 1 Output Switching**

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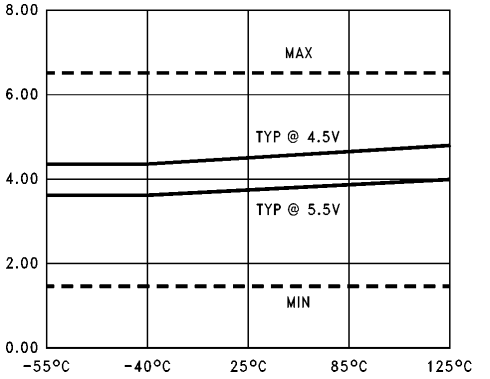
**$t_{PZH}$ vs Temperature ($T_A$)**
**$C_L$ = 50 pF, 8 Outputs Switching**

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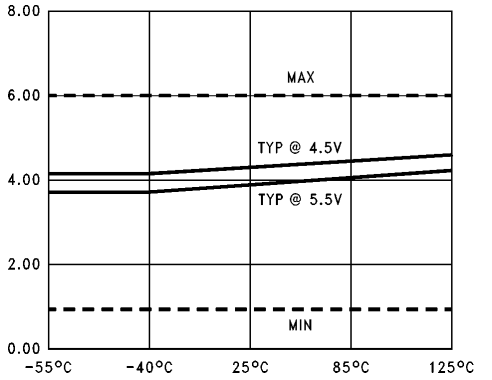
Dashed lines represent design characteristics, for specified guarantees refer to AC Characteristics Table.

**$t_{PHZ}$ vs Temperature ($T_A$)**
**$C_L$ = 50 pF, 8 Outputs Switching**

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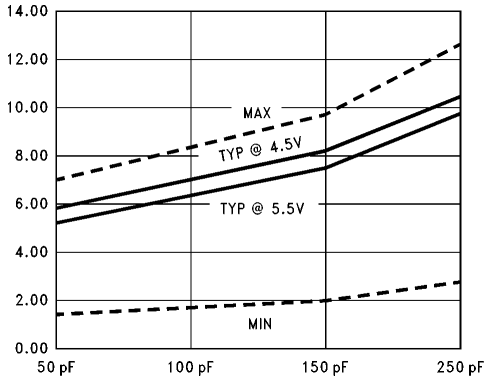
**$t_{PZL}$ vs Load Capacitance**
**8 Outputs Switching, $T_A$ = 25°C**

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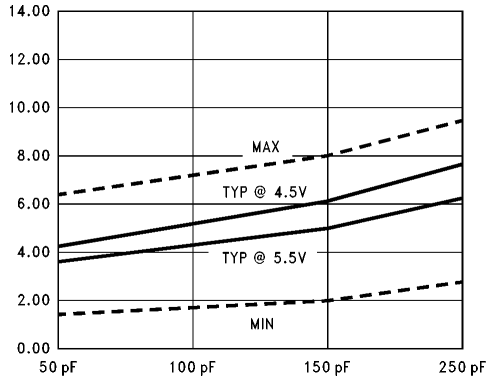
**$t_{PZH}$ vs Load Capacitance**
**8 Outputs Switching, $T_A$ = 25°C**

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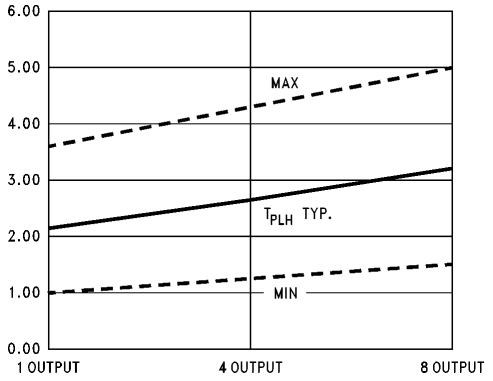
**$t_{PLH}$ vs Number Outputs Switching**
**$V_{CC}$ = 5.0V, $T_A$ = 25°C, $C_L$ = 50 pF**

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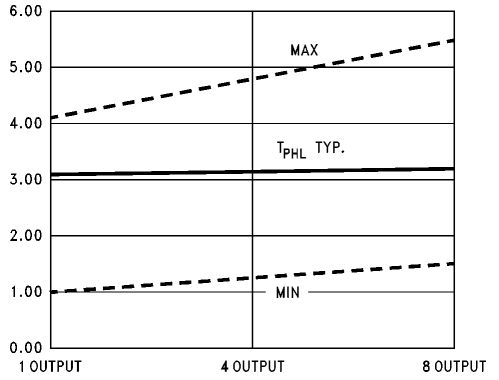
**$t_{PHL}$ vs Number Outputs Switching**
**$V_{CC}$ = 5.0V, $T_A$ = 25°C, $C_L$ = 50 pF**

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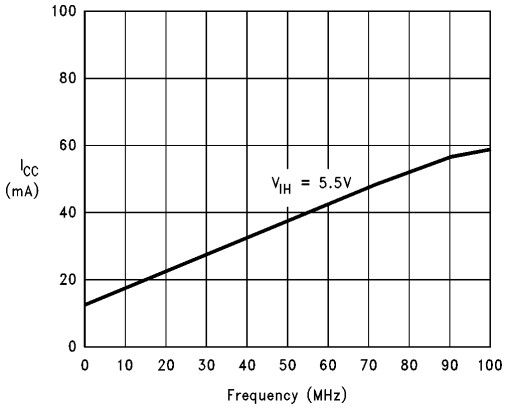
**$I_{CC}$ vs Frequency, Average, $T_A$ = 25°C**
**All outputs unloaded/unterminated**

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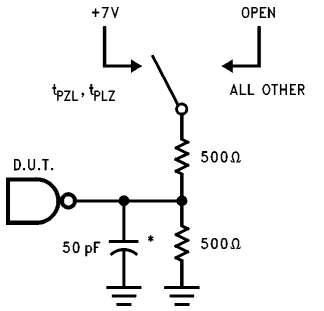
Dashed lines represent design characteristics, for specified guarantees refer to AC Characteristics Table.

## AC Loading

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*Includes jig and probe capacitance.

**FIGURE 1. Standard AC Test Load**

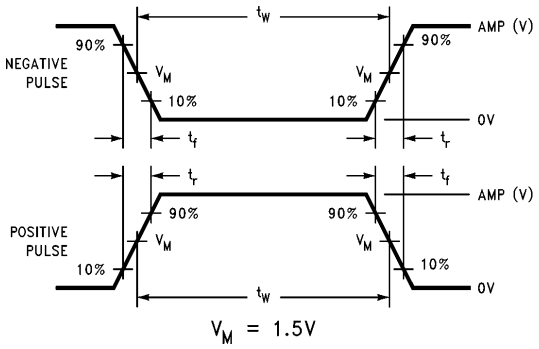


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**FIGURE 2a. Test Input Signal Levels**

| Amplitude | Rep. Rate | $t_w$ | $t_r$ | $t_f$ |
|---|---|---|---|---|
| 3.0V | 1 MHz | 500 ns | 2.5 ns | 2.5 ns |

**FIGURE 2b. Test Input Signal Requirements**

## AC Waveforms

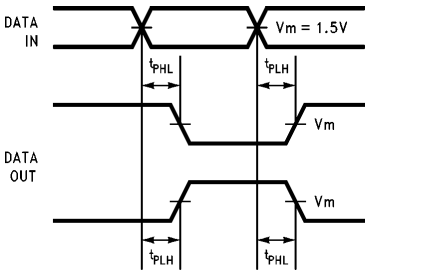


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**FIGURE 3. Propagation Delay Waveforms for Inverting and Non-Inverting Functions**

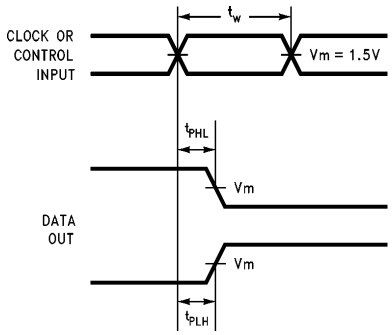


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**FIGURE 4. Propagation Delay, Pulse Width Waveforms**

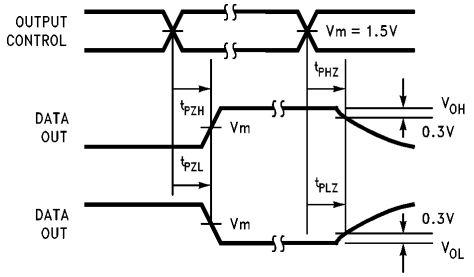


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**FIGURE 5. TRI-STATE Output HIGH and LOW Enable and Disable Times**

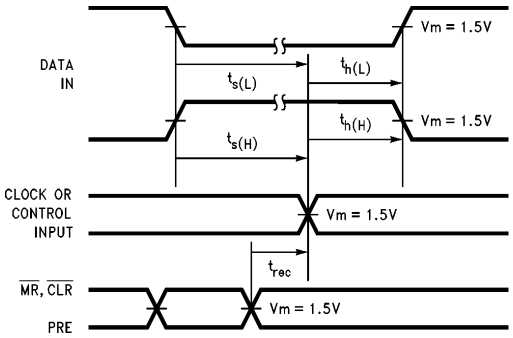


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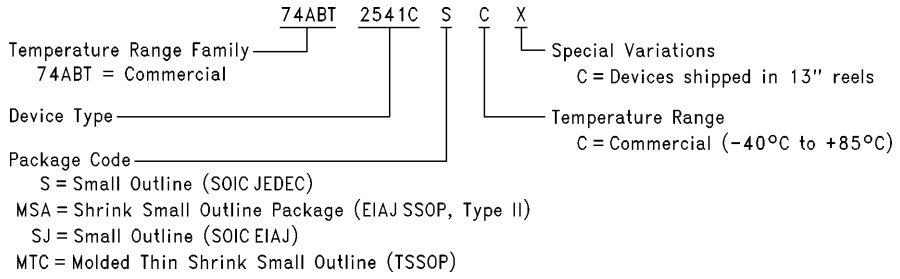
**FIGURE 6. Setup Time, Hold Time and Recovery Time Waveforms**

## Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are derived as follows:

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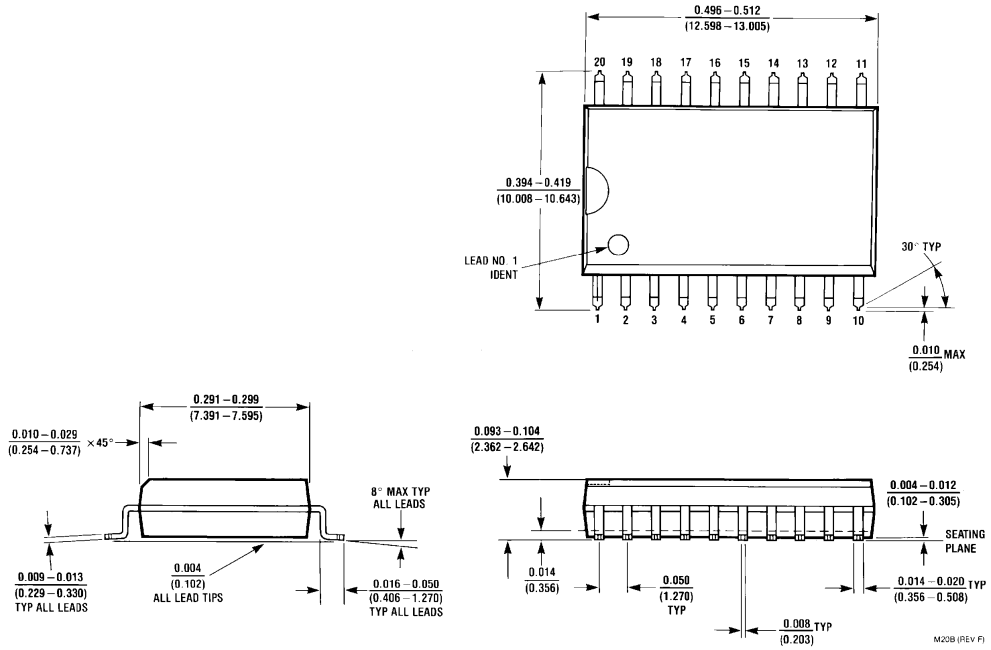
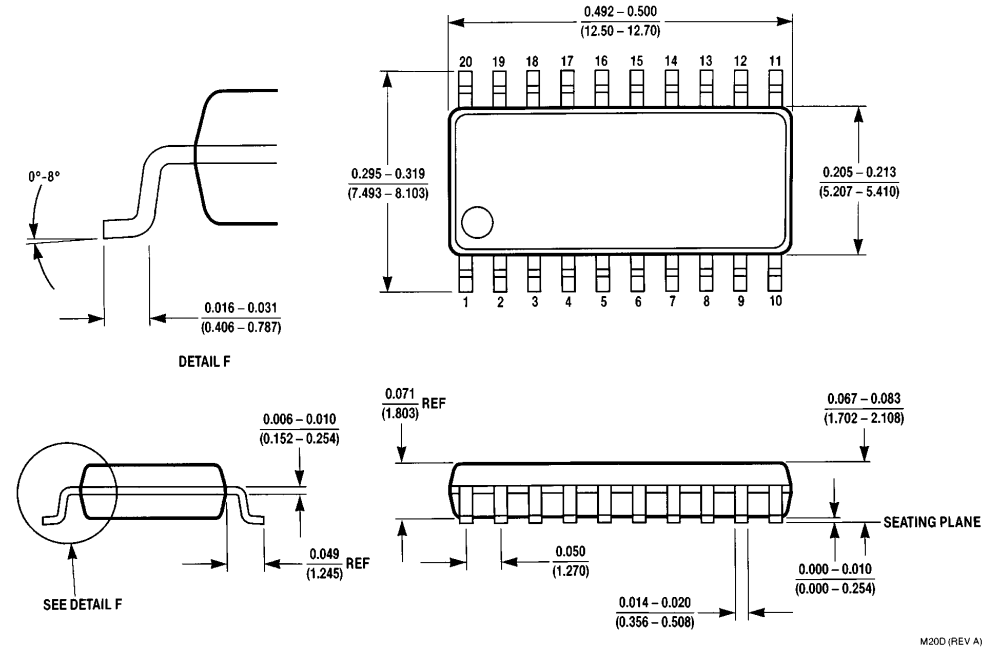
## Physical Dimensions inches (millimeters)

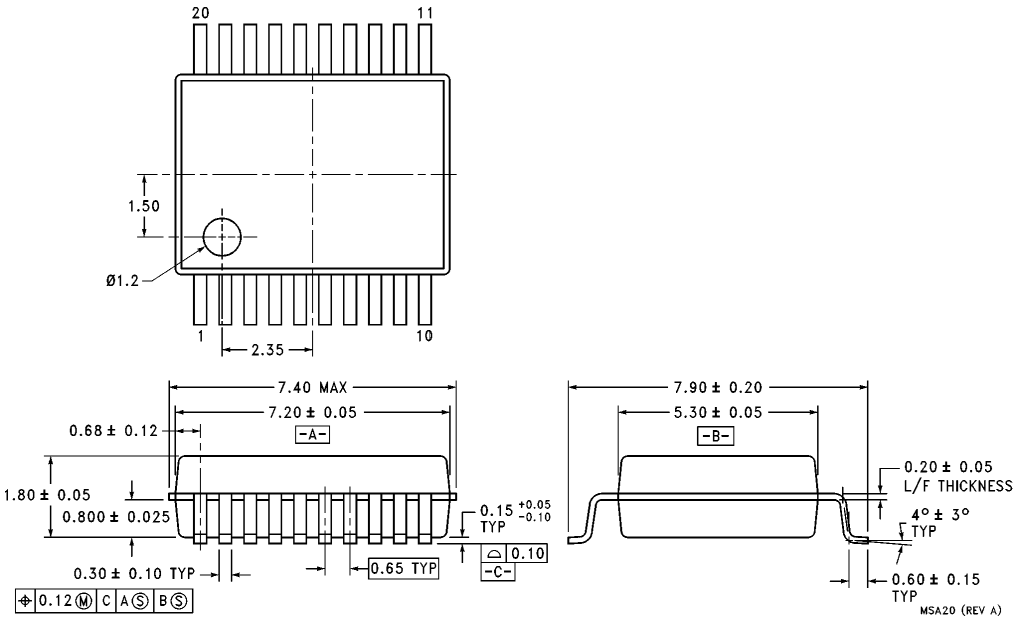



**20-Lead Small Outline Integrated Circuit JEDEC (S)**
**NS Package Number M20B**



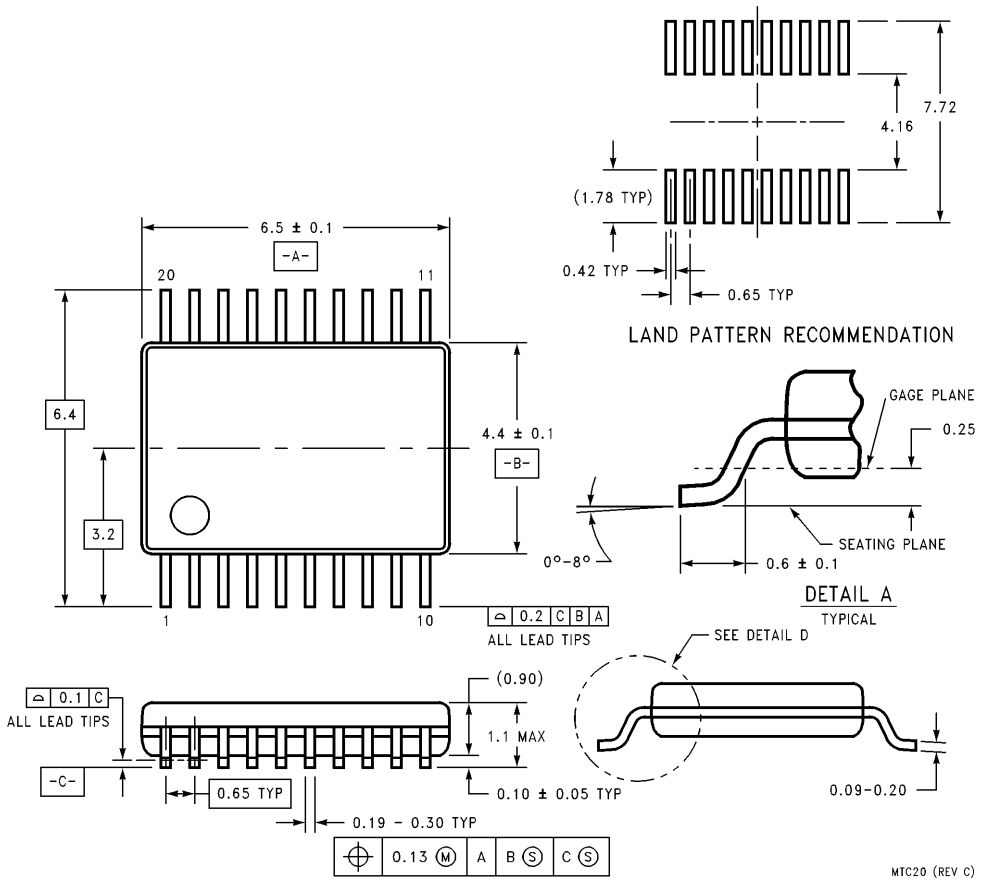

**20-Lead Small Outline Integrated Circuit EIAJ (SJ)**
**NS Package Number M20D**

## Physical Dimensions millimeters (Continued)




**20-Lead Plastic EIAJ SSOP, Type II (MSA)**
**NS Package Number MSA20**

## Physical Dimensions millimeters (Continued)




**20-Lead Molded Thin Shrink Small Outline Package, JEDEC**
**NS Package Number MTC20**

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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