National Semiconductor

September 1995

74ABT2952
Octal Registered Transceiver

General Description

The 'ABT2952 is an octal registered transceiver. Two 8-bit back to back registers store data flowing in both directions between two bidirectional buses. Separate clock, clock enable and TRI-STATE® output enable signals are provided for each register. The output pins are guaranteed to source 32 mA (24 mA mil.) and to sink 64 mA (48 mA mil).

Features

- Separate clock, clock enable and TRI-STATE output enable provided for each register
- A and B output sink capability of 64 mA source capability of 32 mA
- Guaranteed output skew
- Guaranteed multiple output switching specifications
- Output switching specified for both 50 pF and 250 pF loads
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Nondestructive hot insertion capability

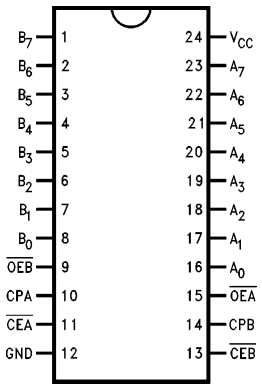
Commercial	Package Number	Package Description
74ABT2952CSC (Note 1)	M24B	24-Lead (0.300″ Wide) Molded Small Outline, JEDEC
74ABT2952CMSA (Note 1)	MSA24	24-Lead Molded Shrink Small Outline, EIAJ Type II
74ABT2952CMTC (Notes 1, 2)	MTC24	24-Lead Molded Thin Shrink Small Outline, JEDEC

Note 1: Devices also available in 13″ reel. Use suffix = SCX, MSAX and MTCX.

Note 2: Contact factory for package availability.

Connection Diagram

Pin Assignment for SOIC and SSOP



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Pin Descriptions

Pin Names	Description
A_0–A_7	A-Register Inputs/B-Register TRI-STATE Outputs
B_0–B_7	B-Register Inputs/A-Register TRI-STATE Outputs
$\overline{OEA}$	Output Enable A-Register
CPA	A-Register Clock
$\overline{CEA}$	A-Register Clock Enable
$\overline{OEB}$	Output Enable B-Register
CPB	B-Register Clock
$\overline{CEB}$	B-Register Clock Enable

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Pin Descriptions (Continued)

Output Control

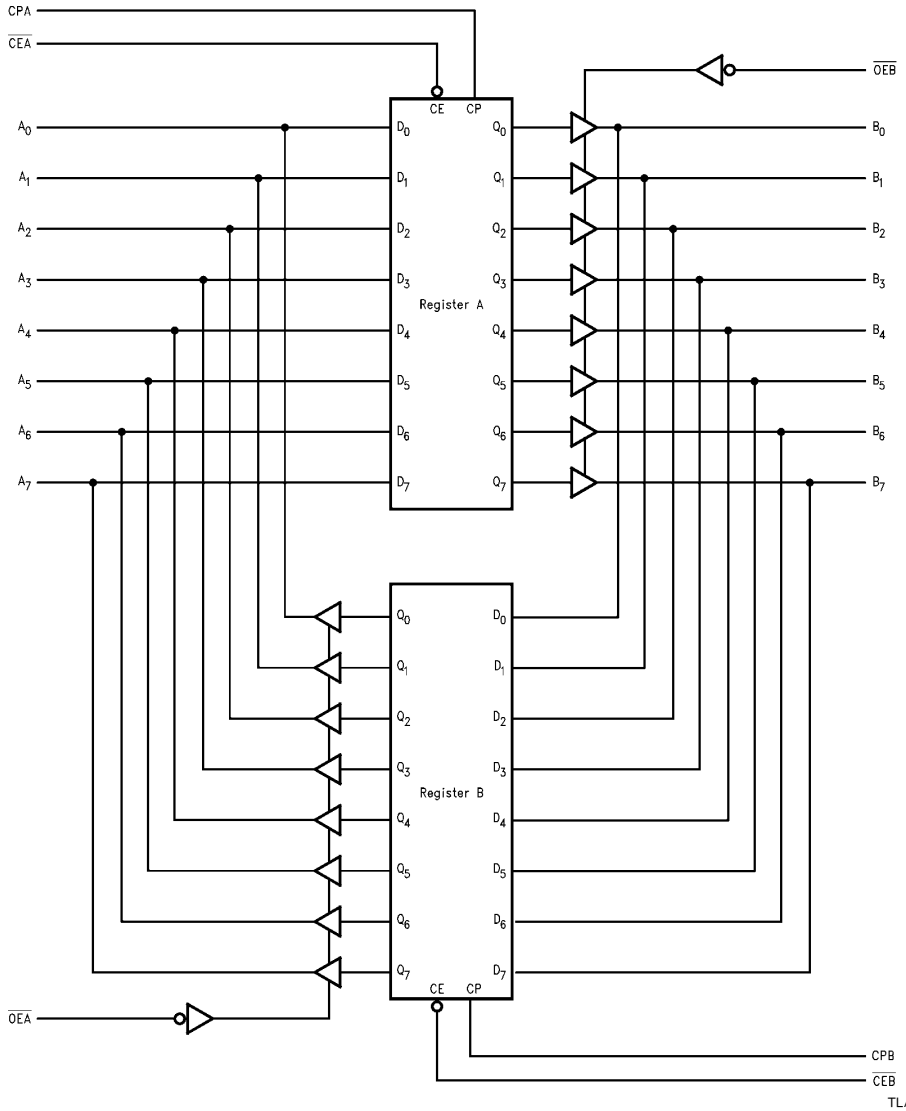
$\overline{OE}$	Internal Q	Output ’ABT2952	Function
H	X	Z	Disable Outputs
L	L	L	Enable Outputs
L	H	H	

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = HIGH Impedance
↗ = LOW-to-HIGH Transition
NC = No Change

Register Function Table (Applies to A or B Register)

Inputs			Internal Q	Function
D	CP	$\overline{CE}$		
X	X	H	NC	Hold Data
L	↗	L	L	Load Data
H	↗	L	H	

Block Diagram



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Absolute Maximum Ratings (Note 1)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Any Output	
in the Disable or Power-Off State	−0.5V to +5.5V
in the HIGH State	−0.5V to V_{CC}

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)
DC Latchup Source Current	−500 mA
Over Voltage Latchup (I/O)	10V

Recommended Operating Conditions

Free Air Ambient Temperature	
Commercial	−40°C to +85°C
Supply Voltage	
Commercial	+4.5V to +5.5V
Minimum Input Edge Rate	(ΔV/Δt)
Data Input	50 mV/ns
Enable Input	20 mV/ns
Clock Input	100 mV/ns

DC Electrical Characteristics

Symbol	Parameter		ABT2952 Min	ABT2952 Typ	ABT2952 Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA (Non I/O Pins)
V_{OH}	Output HIGH Voltage	74ABT 74ABT	2.5 2.0					I_{OH} = −3 mA (A_n, B_n) I_{OH} = −32 mA (A_n, B_n)
V_{OL}	Output LOW Voltage	74ABT			0.55	V	Min	I_{OL} = 64 mA (A_n, B_n)
V_{ID}	Input Leakage Test		4.75			V	0.0	I_{ID} = 1.9 μA (Non-I/O Pins) All Other Pins Grounded
I_{IH}	Input HIGH Current				5	μA	Max	V_{IN} = 2.7V (Non-I/O Pins) (Note 2) V_{IN} = V_{CC} (Non-I/O Pins)
I_{BVI}	Input HIGH Current Breakdown Test				7	μA	Max	V_{IN} = 7.0V (Non-I/O Pins)
I_{BVIT}	Input HIGH Current Breakdown Test (I/O)				100	μA	Max	V_{IN} = 5.5V (A_n, B_n)
I_{IL}	Input LOW Current				−5	μA	Max	V_{IN} = 0.5V (Non-I/O Pins) (Note 2) V_{IN} = 0.0V (Non-I/O Pins)
I_{IH} + I_{OZH}	Output Leakage Current				50	μA	0V–5.5V	V_{OUT} = 2.7V (A_n, B_n); $\overline{OEA}$ or $\overline{OEB}$ = 2.0V
I_{IL} + I_{OZL}	Output Leakage Current				−50	μA	0V–5.5V	V_{OUT} = 0.5V (A_n, B_n); $\overline{OEA}$ or $\overline{OEB}$ = 2.0V
I_{OS}	Output Short-Circuit Current		−100		−275	mA	Max	V_{OUT} = 0V (A_n, B_n)
I_{CEX}	Output HIGH Leakage Current				50	μA	Max	V_{OUT} = V_{CC} (A_n, B_n)
I_{ZZ}	Bus Drainage Test				100	μA	0.0V	V_{OUT} = 5.5V (A_n, B_n); All Others GND
I_{CCH}	Power Supply Current				250	μA	Max	All Outputs HIGH
I_{CCL}	Power Supply Current				30	mA	Max	All Outputs LOW
I_{CCZ}	Power Supply Current				50	μA	Max	Outputs TRI-STATE; All Others GND
I_{CCT}	Additional I_{CC}/Input				2.5	mA	Max	V_I = V_{CC} − 2.1V; All Others at V_{CC} or GND
I_{CCD}	Dynamic I_{CC} (Note 2)	No Load			0.18	mA/MHz	Max	Outputs Open $\overline{OEA}$ or $\overline{OEB}$ = GND, Non-I/O = GND or V_{CC} One Bit toggling, 50% duty cycle (Note 1)

Note 1: For 8-bit toggling, I_{CCD} < 1.4 mA/MHz.

Note 2: Guaranteed, but not tested.

DC Electrical Characteristics (SOIC package) (Continued)

Symbol	Parameter	Min	Typ	Max	Units	V_{CC}	Conditions $C_L = 50$ pF, $R_L = 500\Omega$
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}		0.6	0.8	V	5.0	$T_A = 25°C$ (Note 1)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	−1.2	−1.0		V	5.0	$T_A = 25°C$ (Note 1)
V_{OHV}	Minimum High Level Dynamic Output Voltage	2.5	3.0		V	5.0	$T_A = 25°C$ (Note 3)
V_{IHD}	Minimum High Level Dynamic Input Voltage	2.0	1.7		V	5.0	$T_A = 25°C$ (Note 2)
V_{ILD}	Maximum Low Level Dynamic Input Voltage		1.2	0.8	V	5.0	$T_A = 25°C$ (Note 2)

Note 1: Max number of outputs defined as (n). n − 1 data inputs are driven 0V to 3V. One output at Low. Guaranteed, but not tested.

Note 2: Max number of data inputs (n) switching. n − 1 inputs switching 0V to 3V. Input-under-test switching: 3V to theshold (V_{ILD}), 0V to threshold (V_{IHD}). Guaranteed, but not tested.

Note 3: Max number of outputs defined as (n). n − 1 data inputs are driven 0V to 3V. One output HIGH. Guaranteed, but not tested.

AC Electrical Characteristics

Symbol	Parameter	74ABT $T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF			74ABT $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 50$ pF		Units
		Min	Typ	Max	Min	Max	
f_{max}	Max Clock Frequency	200			200		MHz
t_{PLH} t_{PHL}	Propagation Delay CPA or CPB to A_n or B_n	1.5 1.5	3.4 3.6	5.3 5.3	1.5 1.5	5.3 5.3	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEA}$ or $\overline{OEB}$ to A_n or B_n	1.5 1.5	3.2 3.5	5.5 5.5	1.5 1.5	5.5 5.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OEA}$ or $\overline{OEB}$ to A_n or B_n	1.5 1.5	3.6 3.2	6.0 6.0	1.5 1.5	6.0 6.0	ns

AC Operating Requirements

Symbol	Parameter	74ABT $T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF		74ABT $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 50$ pF		Units
		Min	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW A_n or B_n to CPA or CPB	2.5 2.5		2.5 2.5		ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW A_n or B_n to CPA or CPB	1.5 1.5		1.5 1.5		ns
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{CEA}$ or $\overline{CEB}$ to CPA or CPB	2.5 2.5		2.5 2.5		ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{CEA}$ or $\overline{CEB}$ to CPA or CPB	1.5 1.5		1.5 1.5		ns
$t_w(H)$ $t_w(L)$	Pulse Width, HIGH or LOW CPA or CPB	3.0 3.0		3.0 3.0		ns

Extended AC Electrical Characteristics

Symbol	Parameter	74ABT $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 50$ pF, 8 Outputs Switching (Note 4)		74ABT $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 250$ pF (Note 5)		74ABT $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 250$ pF, 8 Outputs Switching (Note 6)		Units
		Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Progagation Delay CPA or CPB to A_n or B_n	1.5 1.5	6.0 6.0	2.0 2.0	8.0 8.0	2.5 2.5	10.5 10.5	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEA}$ or $\overline{OEB}$ to A_n or B_n	1.5 1.5	6.0 6.0	2.0 2.0	8.0 8.0	2.5 2.5	11.5 11.5	ns
t_{PHZ} t_{PZL}	Output Disable Time $\overline{OEA}$ or $\overline{OEB}$ to A_n or B_n	1.5 1.5	6.0 6.0	(Note 7)		(Note 7)		ns

Note 4: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.).

Note 5: This specification is guaranteed but not tested. The limits represent propagation delay with 250 pF load capacitors in plce of the 50 pF load capacitors in the standard AC load. This specificaiton pertains to single output switching only.

Note 6: This specification is guaranteed but not tested. The limits represent propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.) with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

Note 7: The TRI-STATE delays are dominated by the RC network (500Ω, 250 pF) on the output and has been excluded from the datasheet.

Skew

Symbol	Parameter	74ABT $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V–5.5V$, $C_L = 50$ pF, 8 Outputs Switching (Note 3)	74ABT $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V–5.5V$, $C_L = 250$ pF, 8 Outputs Switching (Note 4)	Units
		Max	Max	
t_{OSHL} (Note 1)	Pin to Pin Skew HL Transitions	1.0	1.5	ns
t_{OSLH} (Note 1)	Pin to Pin Skew LH Transitions	1.0	2.0	ns
t_{PS} (Note 5)	Duty Cycle LH–HL Skew	2.0	4.5	ns
t_{OST} (Note 1)	Pin to Pin Skew LH/HL Transitions	2.1	4.5	ns
t_{PV} (Note 2)	Device to Device Skew LH/HL Transitions	2.5	5.0	ns

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH to LOW (t_{OSHL}), LOW to HIGH (t_{OSLH}), or any combination switching LOW to HIGH and/or HIGH to LOW (t_{OST}). This specification is guaranteed but not tested.

Note 2: Propagation delay variation for a given set of conditions (i.e., temperature and V_{CC}) from device to device. This specification is guaranteed but not tested.

Note 3: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.).

Note 4: This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

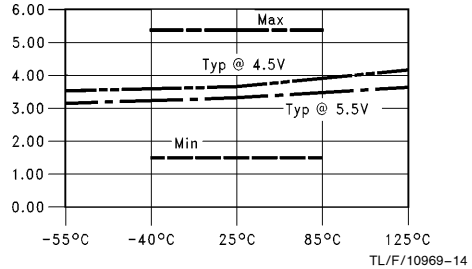
Note 5: This describes the difference between the delay of the LOW-to-HIGH and the HIGH-to-LOW transition on the same pin. It is measured across all the outputs (drivers) on the same chip, the worst (largest delta) number is the guaranteed specification. This specification is guaranteed but not tested.

Capacitance

Symbol	Parameter	Typ	Units	Conditions $T_A = 25°C$
C_{IN}	Input Capacitance	5	pF	$V_{CC} = 0V$ (Non I/O Pins)
$C_{I/O}$ (Note 1)	Output Capacitance	11	pF	$V_{CC} = 5.0V$ (A_n, B_n)

Note 1: $C_{I/O}$ is measured at frequency f = 1 MHz, per MIL-STD-883B, Method 3012.

t_{PLH} vs Temperature (T_A)
$C_L = 50$ pF, 1 Output Switching



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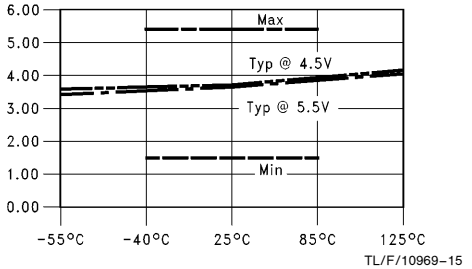
t_{PHL} vs Temperature (T_A)
$C_L = 50$ pF, 1 Output Switching



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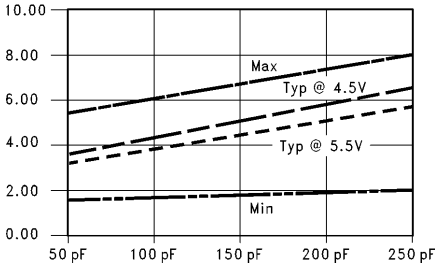
t_{PLH} vs Load Capacitance
1 Output Switching, $T_A = 25°C$



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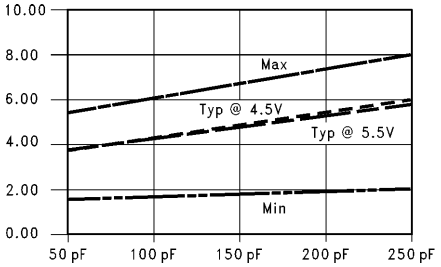
t_{PHL} vs Load Capacitance
1 Output Switching, $T_A = 25°C$



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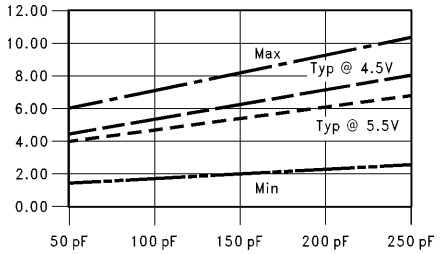
t_{PLH} vs Load Capacitance
8 Outputs Switching, $T_A = 25°C$



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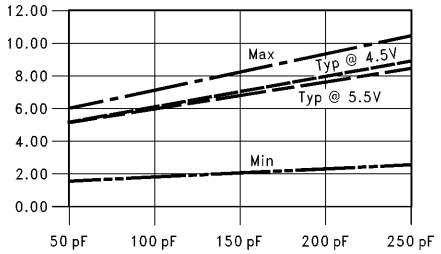
t_{PHL} vs Load Capacitance
8 Outputs Switching, $T_A = 25°C$



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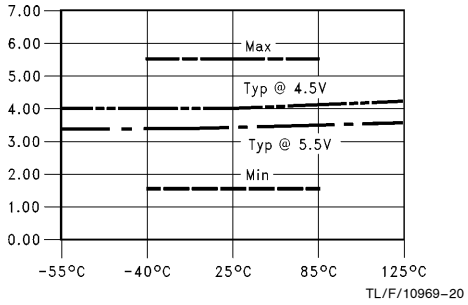
Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Tables.

t_{PZL} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching



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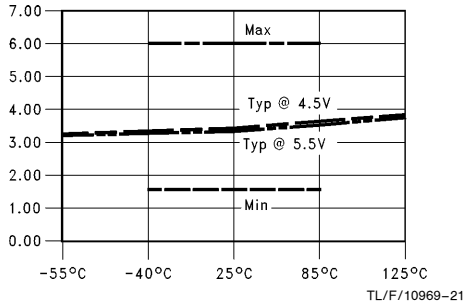
t_{PLZ} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching



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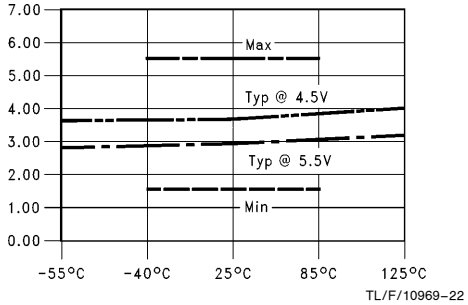
t_{PZH} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching



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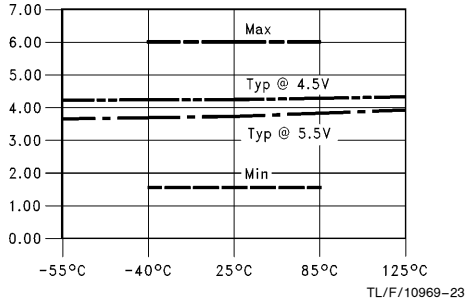
t_{PHZ} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching



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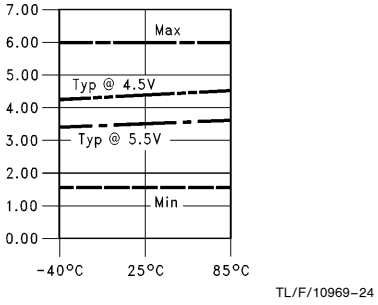
t_{PZH} vs Temperature (T_A)
C_L = 50 pF, 8 Outputs Switching



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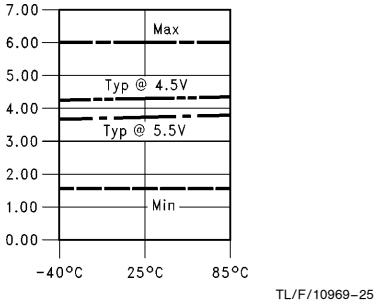
t_{PHZ} vs Temperature (T_A)
C_L = 50 pF, 8 Outputs Switching



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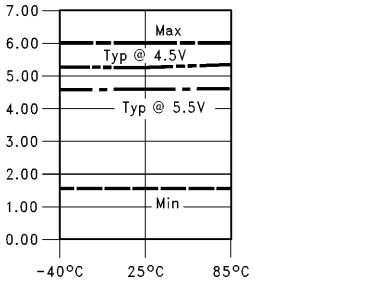
Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Tables.

t_{PZL} vs Temperature (T_A)
C_L = 50 pF, 8 Outputs Switching



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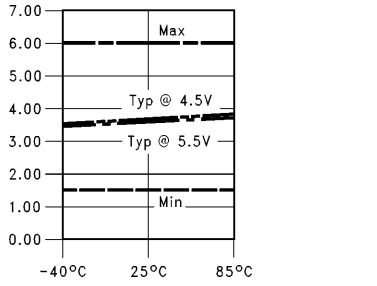
t_{PLZ} vs Temperature (T_A)
C_L = 50 pF, 8 Outputs Switching



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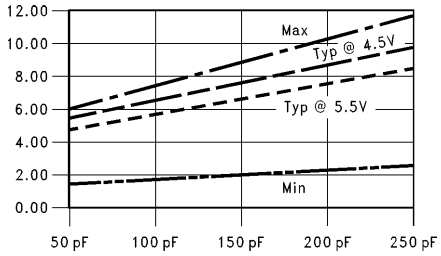
t_{PZL} vs Load Capacitance
8 Outputs Switching, T_A = 25°C



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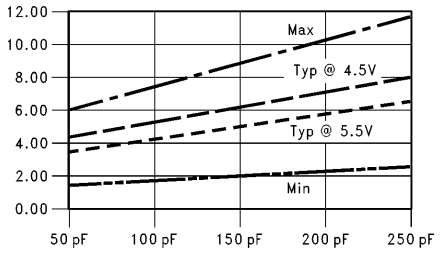
t_{PZH} vs Load Capacitance
8 Outputs Switching, T_A = 25°C



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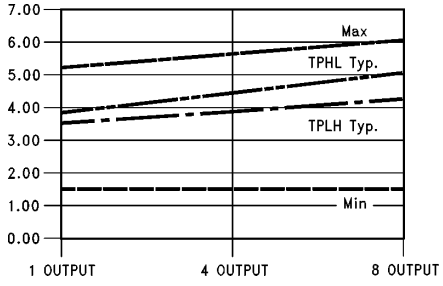
t_{PLH} vs Number Output Switching
V_{CC} = 5.0V, T_A = 25°C, C_L = 50 pF



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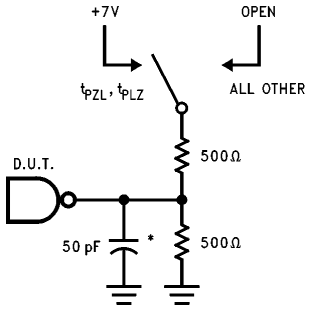
Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Tables.

AC Loading



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*Includes jig and probe capacitance

FIGURE 1. Standard AC Test Load

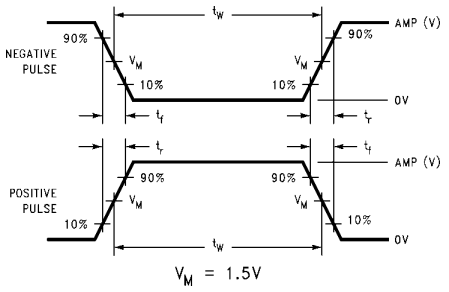

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FIGURE 2a. Test Input Signal Levels

Amplitude	Rep. Rate	t_W	t_r	t_f
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 2b. Input Signal Requirements

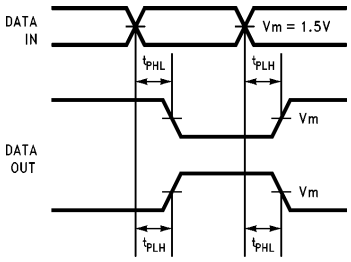

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FIGURE 3. Propagation Delay Waveforms for Inverting and Non-Inveting Functions

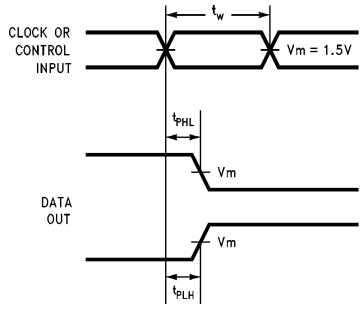

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FIGURE 4. Propagation Delay, Pulse Width Waveforms

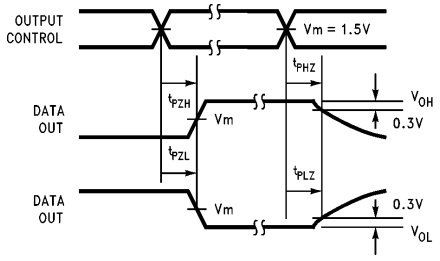

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FIGURE 5. TRI-STATE Output HIGH and LOW Enable and Disable Times

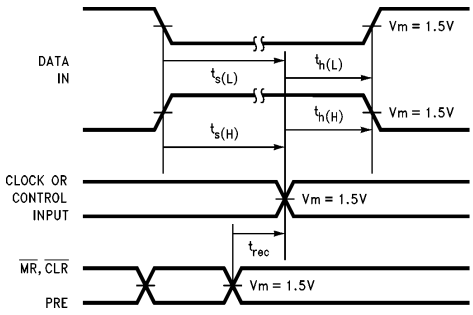

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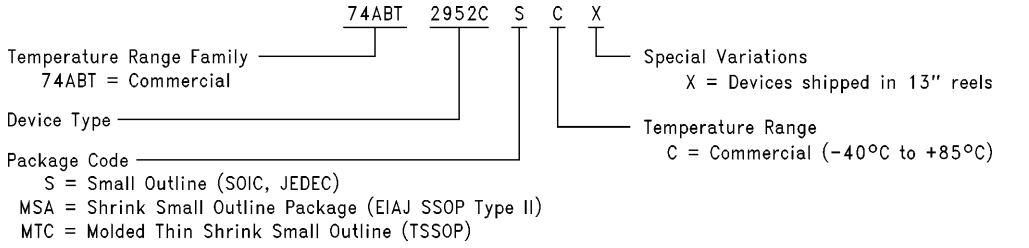
FIGURE 6. Setup Time, Hold Time and Recovery Time Waveforms

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



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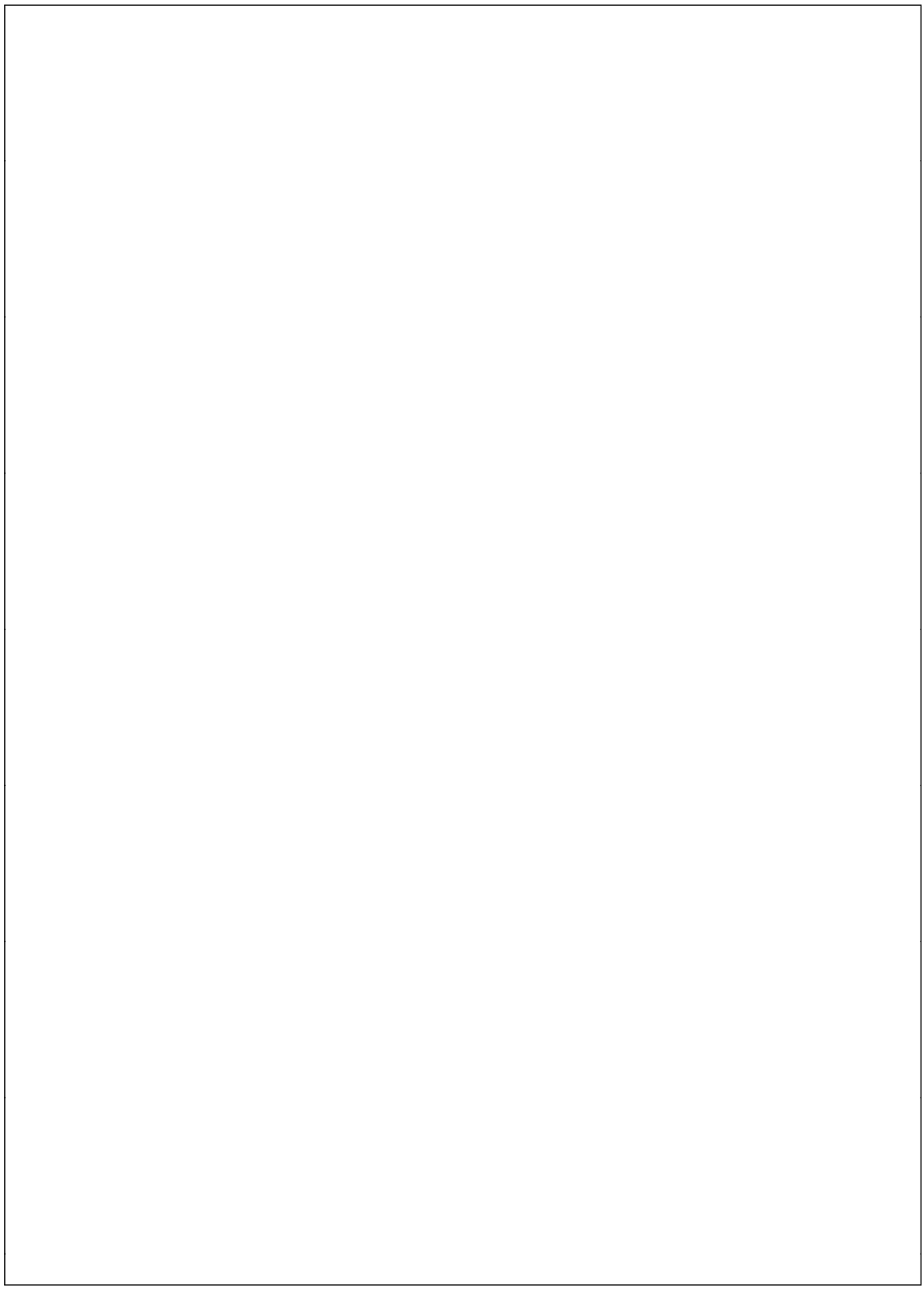
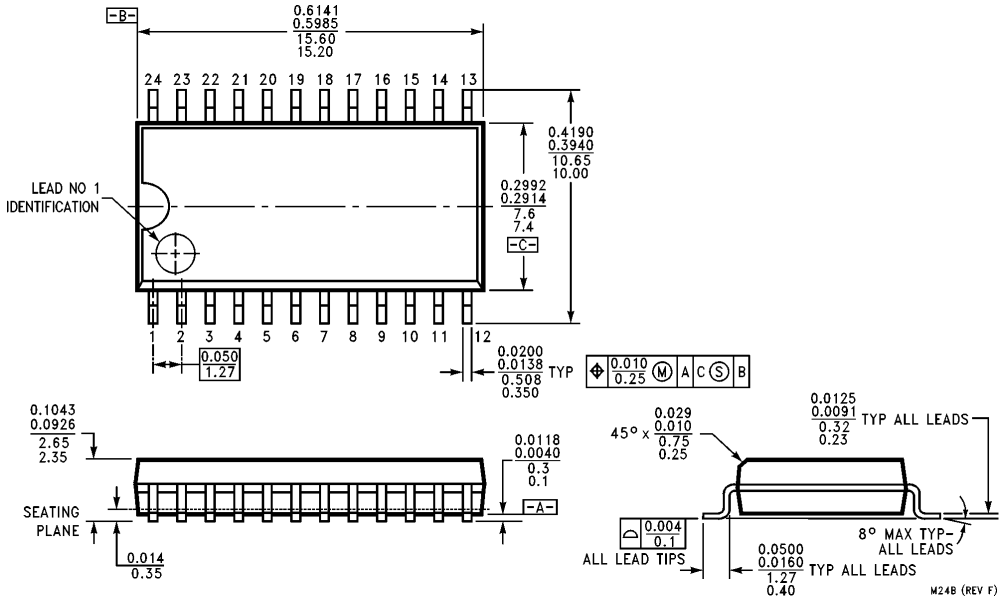
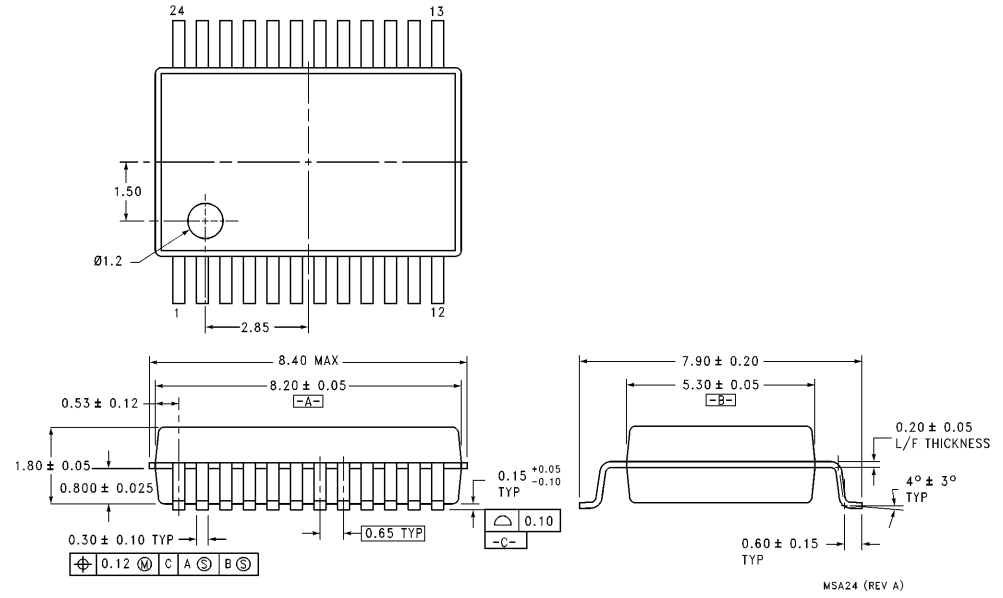


Physical Dimensions inches (millimeters)

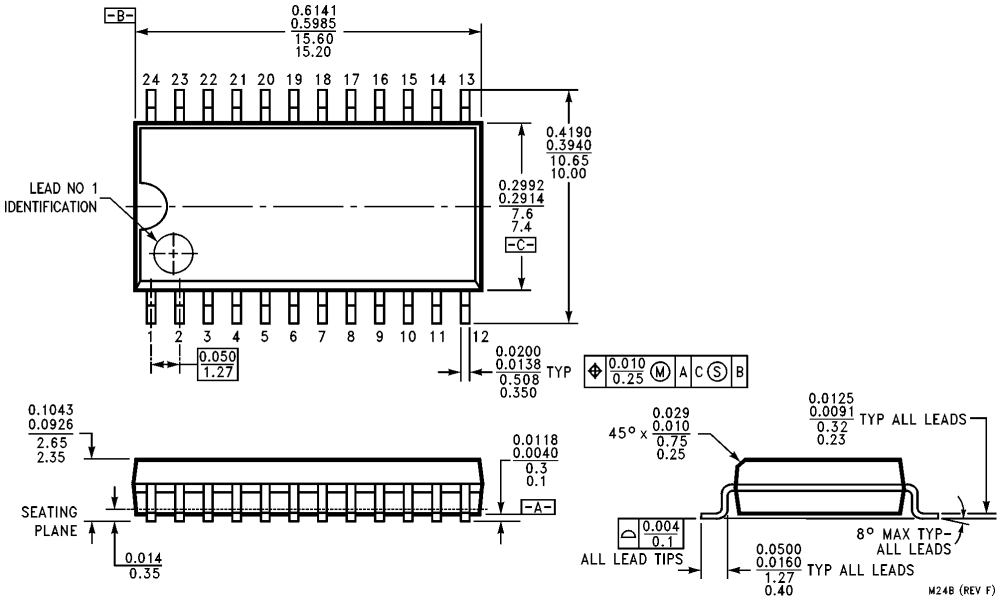


24-Lead (0.300″ Wide) Molded Small Outline, JEDEC (M)
NS Package Number M24B

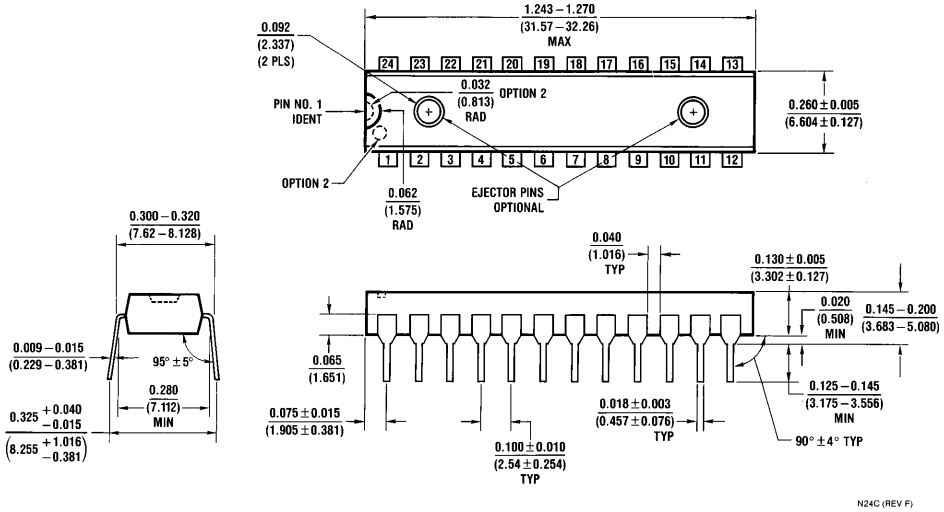


24-Lead Plastic EIAJ SSOP, Type II (MSA)
NS Package Number MSA24

Physical Dimensions inches (millimeters) (Continued)

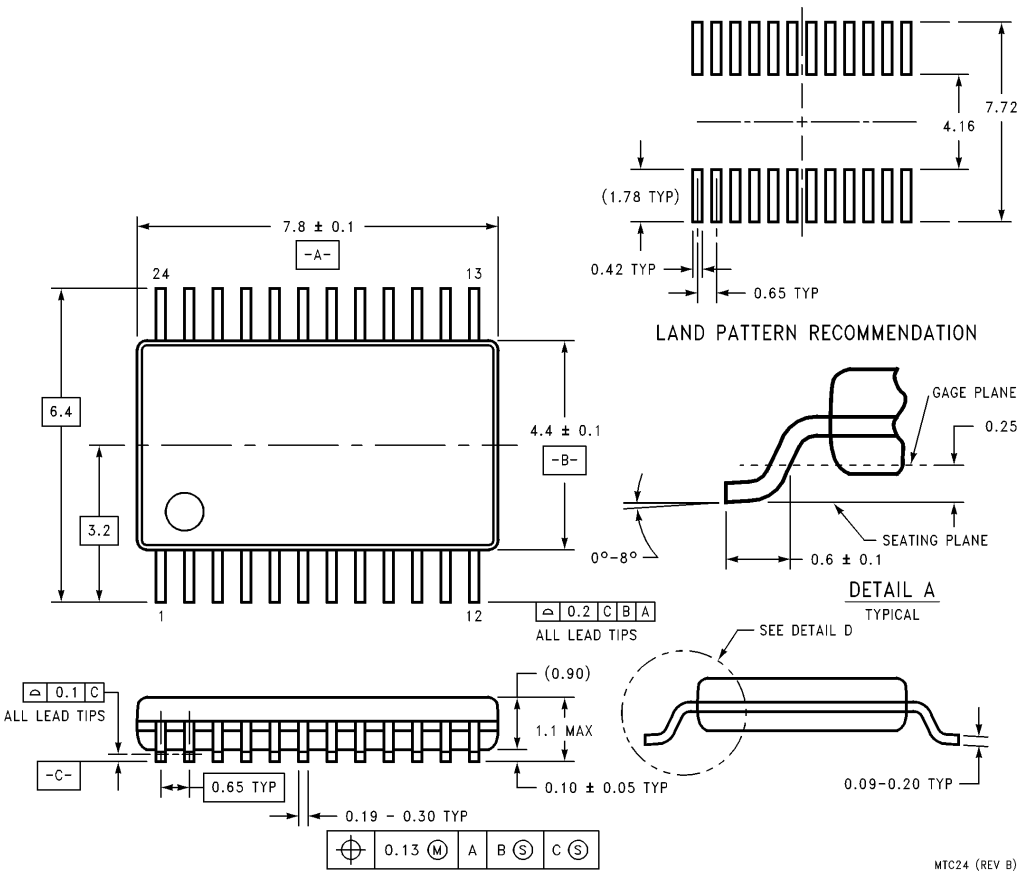


24-Lead Small Outline Integrated Circuit (S)
NS Package Number M24B



24-Lead Plastic Slim (0.300″ Wide) Dual-In-Line Package (SP)
NS Package Number N24C

Physical Dimensions millimeters (Continued)



24-Lead Molded Thin Shrink Small Outline Package, JEDEC
NS Package Number MTC24

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National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

National Semiconductor Europe
Fax: (+49) 0-180-530 85 86
Email: cnjwge@tevm2.nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
Français Tel: (+49) 0-180-532 93 58
Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
Tel: 81-043-299-2309
Fax: 81-043-299-2408

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