National Semiconductor

54ABT/74ABT374
Octal D-Type Flip-Flop with TRI-STATE® Outputs

General Description

The 'ABT374 is an octal D-type flip-flop featuring separate D-type inputs for each flip-flop and TRI-STATE outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable ($\overline{OE}$) are common to all flip-flops.

Features

- Edge-triggered D-type inputs
- Buffered positive edge-triggered clock
- TRI-STATE outputs for bus-oriented applications
- Output sink capability of 64 mA, source capability of 32 mA
- Guaranteed output skew
- Guaranteed multiple output switching specifications
- Output switching specified for both 50 pF and 250 pF loads
- Guaranteed simultaneous switching, noise level and dynamic threshold performance
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Non-destructive hot insertion capability
- Standard Military Drawing (SMD) 5962-9314901

Ordering Code: See Section 10

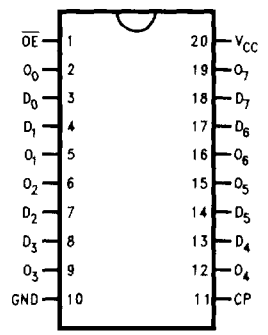
Commercial	Military	Package Number	Package Description
74ABT374CSC (Note 1)		M20B	20-Lead (0.300" Wide) Molded Small Outline, JEDEC
74ABT374CSJ (Note 1)		M20D	20-Lead (0.300" Wide) Molded Small Outline, EIAJ
74ABT374CPC		N20B	20-Lead (0.300" Wide) Molded Dual-In-Line
	54ABT374J/883	J20A	20-Lead Ceramic Dual-In-Line
74ABT374CMSA (Note 1)		MSA20	20-Lead Molded Shrink Small Outline, EIAJ Type II
	54ABT374W/883	W20A	20-Lead Cerpack
	54ABT374E/883	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C
74ABT374CMTC (Notes 1, 2)		MTC20	20-Lead Molded Thin Shrink Small Outline, JEDEC

Note 1: Devices also available in 13" reel. Use suffix = SCX, SJX, MSAX, and MTCX.

Note 2: Contact factory for package availability.

Connection Diagrams

Pin Assignment for DIP, SOIC, SSOP and Flatpak



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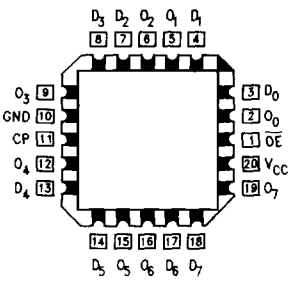
Pin Assignment for LCC



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Pin Descriptions

Pin Names	Description
D_0–D_7	Data Inputs
CP	Clock Pulse Input (Active Rising Edge)
$\overline{OE}$	TRI-STATE Output Enable Input (Active LOW)
O_0–O_7	TRI-STATE Outputs

Functional Description

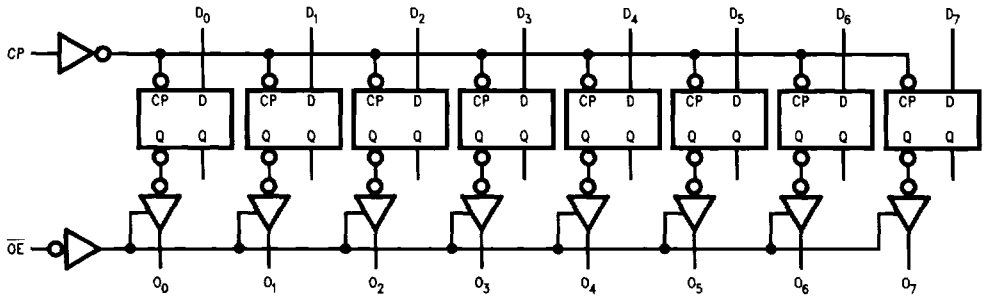
The 'ABT374 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When $\overline{OE}$ is HIGH, the outputs are in a high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

Function Table

Inputs			Internal	Outputs	Function
$\overline{OE}$	CP	D	Q	O	
H	H	L	NC	Z	Hold
H	H	H	NC	Z	Hold
H	⌐	L	L	Z	Load
H	⌐	H	H	Z	Load
L	⌐	L	L	L	Data Available
L	⌐	H	H	H	Data Available
L	H	L	NC	NC	No Change in Data
L	H	H	NC	NC	No Change in Data

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
⌐ = LOW-to-HIGH Transition
NC = No Change

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	
Ceramic	−55°C to +175°C
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Any Output	
in the Disabled or Power-Off State	−0.5V to 5.5V
in the HIGH State	−0.5V to V_{CC}
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)
DC Latchup Source Current: $\overline{OE}$ Pin	−150 mA
(Across Comm Operating Range) Other Pins	−500 mA
Over Voltage Latchup (I/O)	10V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	−40°C to +85°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V
Minimum Input Edge Rate	($\Delta V/\Delta t$)
Data Input	50 mV/ns
Enable Input	20 mV/ns
Clock Input	100mV/ns

DC Electrical Characteristics

Symbol	Parameter		ABT374 Min	ABT374 Typ	ABT374 Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54ABT/74ABT	2.5			V	Min	I_{OH} = −3 mA
		54ABT	2.0			V	Min	I_{OH} = −24 mA
		74ABT	2.0			V	Min	I_{OH} = −32 mA
V_{OL}	Output LOW Voltage	54ABT			0.55	V	Min	I_{OL} = 48 mA
		74ABT			0.55			I_{OL} = 64 mA
I_{IH}	Input HIGH Current				5	μA	Max	V_{IN} = 2.7V (Note 2)
					5			V_{IN} = V_{CC}
I_{BVI}	Input HIGH Current Breakdown Test				7	μA	Max	V_{IN} = 7.0V
I_{IL}	Input LOW Current				−5	μA	Max	V_{IN} = 0.5V (Note 2)
					−5			V_{IN} = 0.0V
V_{ID}	Input Leakage Test		4.75			V	0.0	I_{ID} = 1.9 μA All Other Pins Grounded
I_{OZH}	Output Leakage Current				50	μA	0 − 5.5V	V_{OUT} = 2.7V; $\overline{OE}$ = 2.0V
I_{OZL}	Output Leakage Current				−50	μA	0 − 5.5V	V_{OUT} = 0.5V; $\overline{OE}$ = 2.0V
I_{OS}	Output Short-Circuit Current		−100		−275	mA	Max	V_{OUT} = 0.0V
I_{CEX}	Output High Leakage Current				50	μA	Max	V_{OUT} = V_{CC}
I_{ZZ}	Bus Drainage Test				100	μA	0.0	V_{OUT} = 5.5V; All Others V_{CC} or GND
I_{CCH}	Power Supply Current				50	μA	Max	All Outputs HIGH
I_{CCL}	Power Supply Current				30	mA	Max	All Outputs LOW
I_{CCZ}	Power Supply Current				50	μA	Max	$\overline{OE}$ = V_{CC}; All Others at V_{CC} or GND
I_{CCT}	Additional I_{CC}/Input	Outputs Enabled			2.5	mA	Max	V_I = V_{CC} − 2.1V
		Outputs TRI-STATE			2.5	mA		Enable Input V_I = V_{CC} − 2.1V
		Outputs TRI-STATE			2.5	mA		Data Input V_I = V_{CC} − 2.1V All Others at V_{CC} or GND
I_{CCD}	Dynamic I_{CC} (Note 2)	No Load			0.30	mA/ MHz	Max	Outputs Open $\overline{OE}$ = GND, (Note 1) One Bit Toggling, 50% Duty Cycle

Note 1: For 8-bit toggling, I_{CCD} < 0.8 mA/MHz.

Note 2: Guaranteed, but not tested.

DC Electrical Characteristics (SOIC package) (Continued)

Symbol	Parameter	Min	Typ	Max	Units	V_{CC}	Conditions C_L = 50 pF, R_L = 500Ω
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}		0.5	0.8	V	5.0	T_A = 25°C (Note 1)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	−1.3	−0.9		V	5.0	T_A = 25°C (Note 1)
V_{OHV}	Minimum High Level Dynamic Output Voltage	2.5	3.0		V	5.0	T_A = 25°C (Note 3)
V_{IHD}	Minimum High Level Dynamic Input Voltage	2.0	1.6		V	5.0	T_A = 25°C (Note 2)
V_{ILD}	Maximum Low Level Dynamic Input Voltage		1.3	0.8	V	5.0	T_A = 25°C (Note 2)

Note 1: Max number of outputs defined as (n). n − 1 data inputs are driven 0V to 3V. One output at Low. Guaranteed, but not tested.

Note 2: Max number of data inputs (n) switching. n − 1 inputs switching 0V to 3V. Input-under-test switching: 3V to theshold (V_{ILD}), 0V to threshold (V_{IHD}). Guaranteed, but not tested.

Note 3: Max number of outputs defined as (n). n − 1 data inputs are driven 0V to 3V. One output HIGH. Guaranteed, but not tested.

AC Electrical Characteristics: See Section 2 for Waveforms (SOIC and SSOP package)

Symbol	Parameter	74ABT T_A = +25°C, V_{CC} = +5.0V, C_L = 50 pF			54ABT T_A = −55°C to +125°C, V_{CC} = 4.5V to 5.5V, C_L = 50 pF		74ABT T_A = −40°C to +85°C, V_{CC} = 4.5V to 5.5V, C_L = 50 pF		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Max Clock Frequency	150	200		150		150		MHz	
t_{PLH}	Propagation Delay	2.0	3.2	5.0	1.4	6.6	2.0	5.0	ns	2-3, 5
t_{PHL}	CP to O_n	2.0	3.3	5.0	2.0	7.6	2.0	5.0		
t_{PZH}	Output Enable Time	1.5	3.1	5.3	0.8	5.7	1.5	5.3	ns	2-4
t_{PZL}		1.5	3.1	5.3	1.5	7.2	1.5	5.3		
t_{PHZ}	Output Disable Time	1.5	3.6	5.4	1.3	7.2	1.5	5.4	ns	2-4
t_{PLZ}		1.5	3.4	5.4	1.0	7.0	1.5	5.4		

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	74ABT T_A = +25°C, V_{CC} = +5.0V, C_L = 50 pF		54ABT T_A = −55°C to +125°C, V_{CC} = 4.5V to 5.5V, C_L = 50 pF		74ABT T_A = −40°C to +85°C, V_{CC} = 4.5V to 5.5V, C_L = 50 pF		Units	Fig. No.
		Min	Max	Min	Max	Min	Max		
t_s(H)	Setup Time, HIGH	1.5		2.5		1.0		ns	2-6
t_s(L)	or LOW D_n to CP	1.5		2.5		1.5			
t_h(H)	Hold Time, HIGH	1.0		2.5		1.0		ns	2-6
t_h(L)	or LOW D_n to CP	1.0		2.5		1.0			
t_w(H)	Pulse Width, CP	3.0		3.3		3.0		ns	2-3
t_w(L)	HIGH or LOW	3.0		3.3		3.0			

Extended AC Electrical Characteristics: See Section 2 for Waveforms (SOIC package)

Symbol	Parameter	74ABT $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 50$ pF, 8 Outputs Switching (Note 4)		74ABT $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 250$ pF (Note 5)		74ABT $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 250$ pF, 8 Outputs Switching (Note 6)		Units	Fig. No.
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Progagation Delay CP to O_n	1.5 1.5	5.7 5.7	2.0 2.0	7.8 7.8	2.0 2.0	10.0 10.0	ns	2-3, 5
t_{PZH} t_{PZL}	Output Enable Time	1.5 1.5	6.2 6.2	2.0 2.0	8.0 8.0	2.0 2.0	10.5 10.5	ns	2-4
t_{PHZ} t_{PZL}	Output Disable Time	1.0 1.0	5.5 5.5	(Note 7)		(Note 7)		ns	2-4

Note 4: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.).

Note 5: This specification is guaranteed but not tested. The limits represent propagation delay with 250 pF load capacitors in plce of the 50 pF load capacitors in the standard AC load. This specificaiton pertains to single output switching only.

Note 6: This specification is guaranteed but not tested. The limits represent propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.) with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

Note 7: The TRI-STATE delay Time is dominated by the RC network (500Ω, 250 pF) on the output and has been excluded from the datasheet.

Skew: See Section 2 (SOIC package) (Note 3)

Symbol	Parameter	74ABT $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V$–$5.5V$, $C_L = 50$ pF, 8 Outputs Switching (Note 3)	74ABT $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V$–$5.5V$, $C_L = 250$ pF, 8 Outputs Switching (Note 4)	Units	Fig. No.
		Max	Max		
t_{OSHL} (Note 1)	Pin to Pin Skew HL Transitions	1.0	1.8	ns	2-13
t_{OSLH} (Note 1)	Pin to Pin Skew LH Transitions	1.0	1.8	ns	2-13
t_{PS} (Note 5)	Duty Cycle LH–HL Skew	1.8	4.3	ns	2-14
t_{OST} (Note 1)	Pin to Pin Skew LH/HL Transitions	2.0	4.3	ns	2-17
t_{PV} (Note 2)	Device to Device Skew LH/HL Transitions	2.5	4.6	ns	2-20

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH to LOW (t_{OSHL}), LOW to HIGH (t_{OSLH}), or any combination switching LOW to HIGH and/or HIGH to LOW (t_{OST}). This specification is guaranteed but not tested.

Note 2: Propagation delay variation for a given set of conditions (i.e., temperature and V_{CC}) from device to device. This specification is guaranteed but not tested.

Note 3: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.).

Note 4: This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

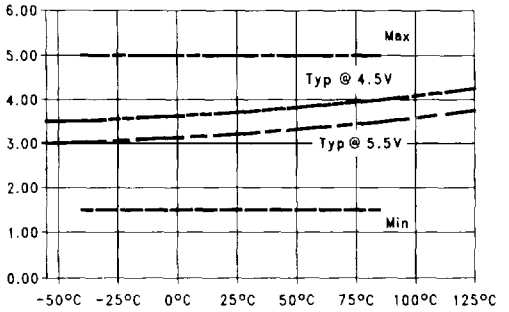
Note 5: This describes the difference between the delay of the LOW-to-HIGH and the HIGH-to-LOW transition on the same pin. It is measured across all the outputs (drivers) on the same chip, the worst (largest delta) number is the guaranteed specification. This specification is guaranteed but not tested.

Capacitance

Symbol	Parameter	Typ	Units	Conditions ($T_A = 25°C$)
C_{IN}	Input Capacitance	5.0	pF	$V_{CC} = 0V$
C_{OUT} (Note 1)	Output Capacitance	9.0	pF	$V_{CC} = 5.0V$

Note 1: C_{OUT} is measured at frequency f = 1 MHz, per MIL-STD-883B, Method 3012.

t_{PLH} vs Temperature (T_A) C_L = 50 pF, 1Output Switching Clock to Output



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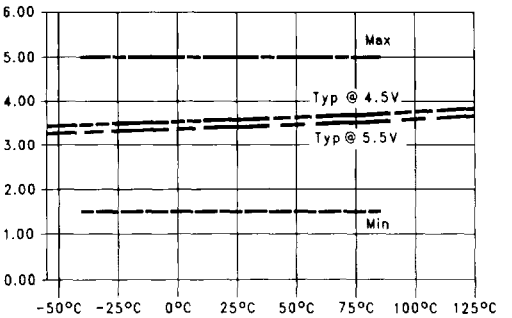
t_{PHL} vs Temperature (T_A) C_L = 50 pF, 1 Output Switching Clock to Output



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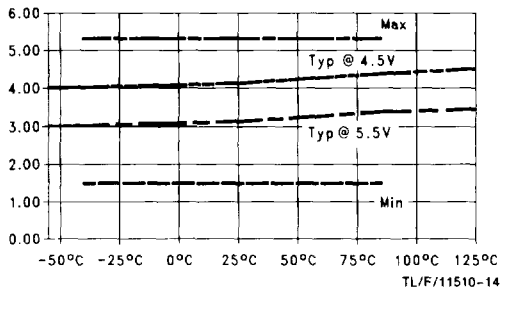
t_{PZH} vs Temperature (T_A) C_L = 50 pF, 1 Output Switching $\overline{OE}$ to Output



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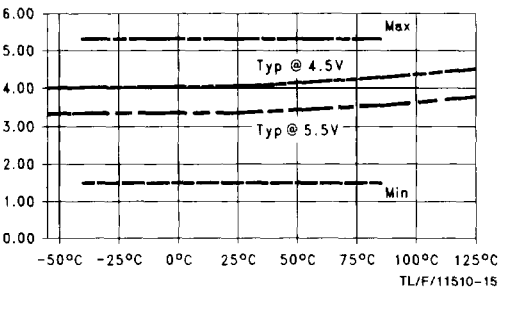
t_{PZL} vs Temperature (T_A) C_L = 50 pF, 1 Output Switching $\overline{OE}$ to Output



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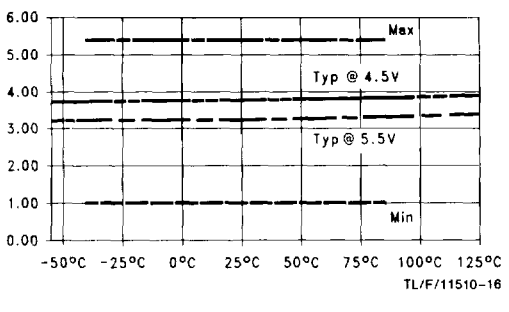
t_{PHZ} vs Temperature (T_A) C_L = 50 pF, 1 Output Switching $\overline{OE}$ to Output



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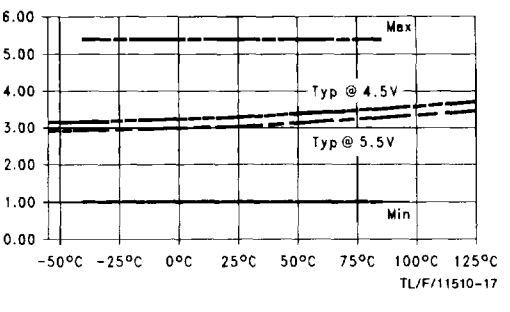
t_{PLZ} vs Temperature (T_A) C_L = 50 pF, 1 Output Switching $\overline{OE}$ to Output



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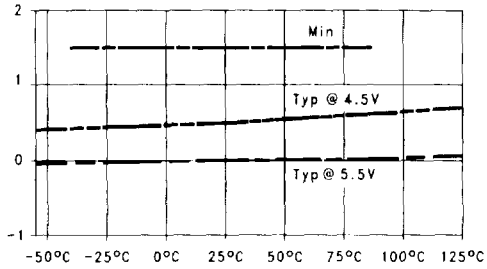
Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Tables.

t_{SET} LOW vs Temperature (T_A) C_L = 50 pF, 1 Output Switching Data to Clock



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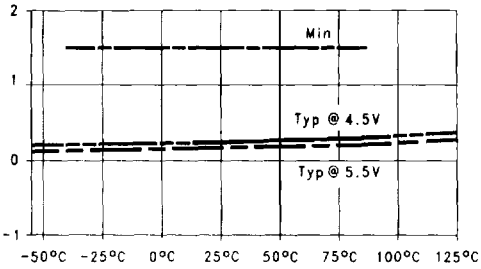
t_{SET} HIGH vs Temperature (T_A) C_L = 50 pF, 1 Output Switching Data to Clock



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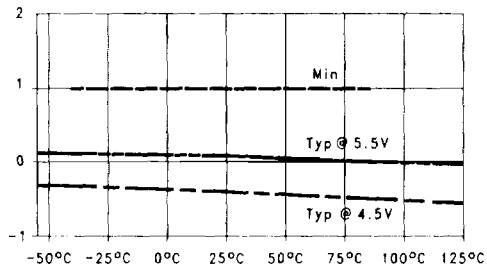
t_{HOLD} HIGH vs Temperature (T_A) C_L = 50 pF, 1 Output Switching Data to Clock



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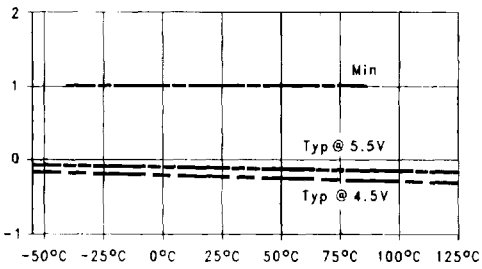
t_{HOLD} LOW vs Temperature (T_A) C_L = 50 pF, 1 Output Switching Data to Clock



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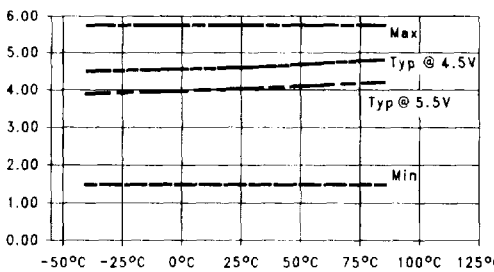
t_{PLH} vs Temperature (T_A) C_L = 50 pF, 8 Outputs Switching Clock to Output



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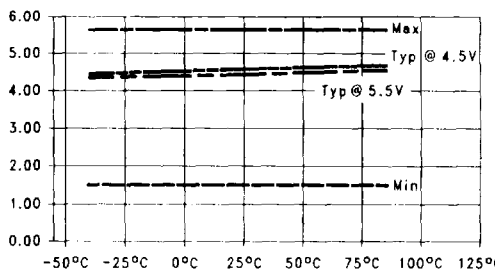
t_{PHL} vs Temperature (T_A) C_L = 50 pF, 8 Outputs Switching Clock to Output



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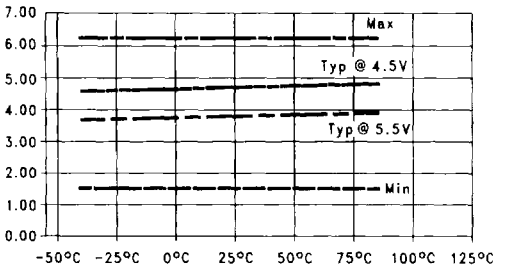
Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Tables.

t_{PZH} vs Temperature (T_A) C_L = 50 pF, 8 Outputs Switching $\overline{OE}$ to Output



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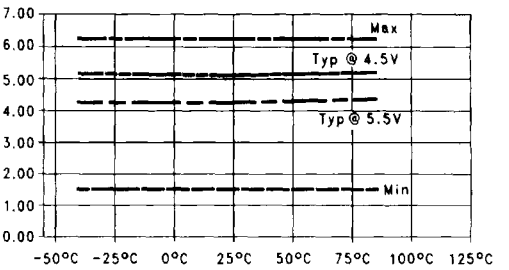
t_{PZL} vs Temperature (T_A) C_L = 50 pF, 8 Outputs Switching $\overline{OE}$ to Output



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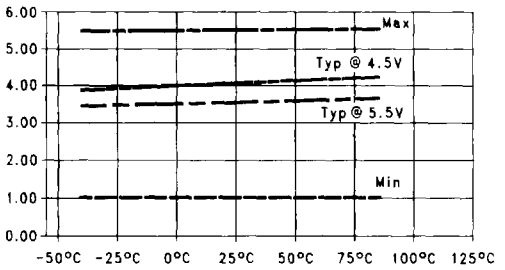
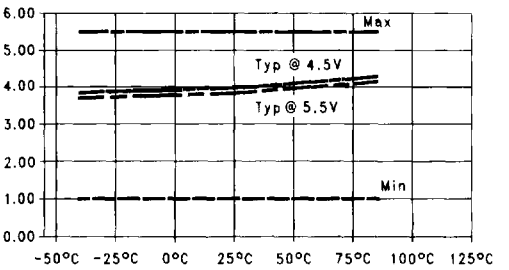
t_{PHZ} vs Temperature (T_A) C_L = 50 pF, 8 Outputs Switching $\overline{OE}$ to Output



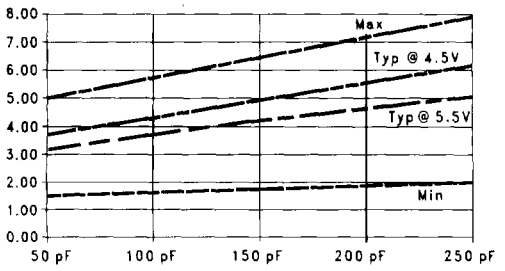
TL/F/11510-26

t_{PLZ} vs Temperature (T_A) C_L = 50 pF, 8 Outputs Switching $\overline{OE}$ to Output



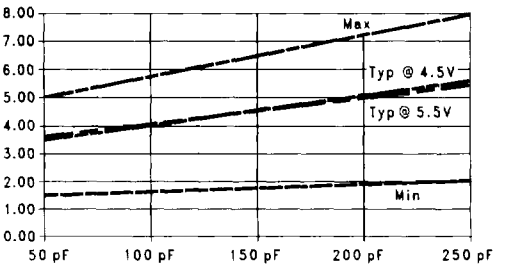
TL/F/11510-27

t_{PLH} vs Load Capacitance T_A = 25°C, 1 Output Switching Clock to Output



TL/F/11510-28

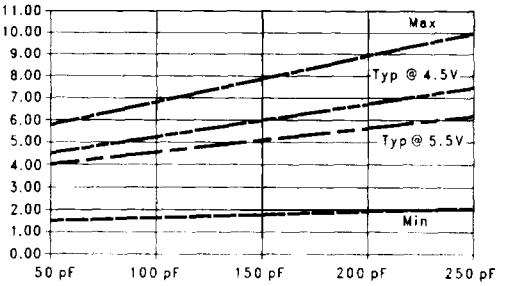
t_{PHL} vs Load Capacitance T_A = 25°C, 1 Output Switching Clock to Output



TL/F/11510-29

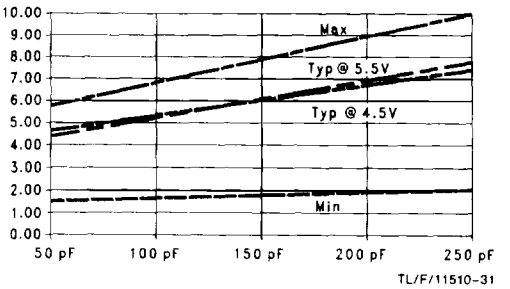
Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Tables.

t_{PLH} vs Load Capacitance T_A = 25°C, 8 Outputs Switching Clock to Output



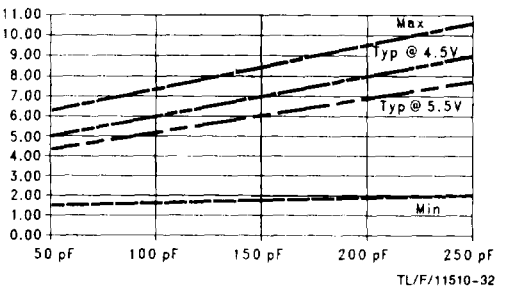
TL/F/11510–30

t_{PHL} vs Load Capacitance T_A = 25°C, 8 Outputs Switching Clock to Output



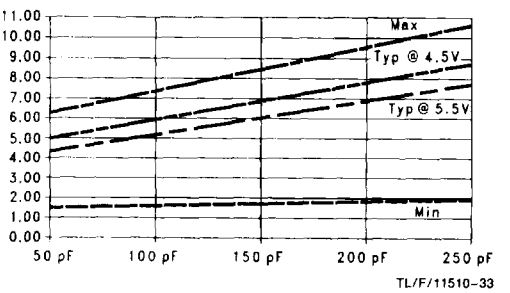
TL/F/11510–31

t_{PZH} vs Load Capacitance T_A = 25°C, 8 Outputs Switching $\overline{OE}$ to Output



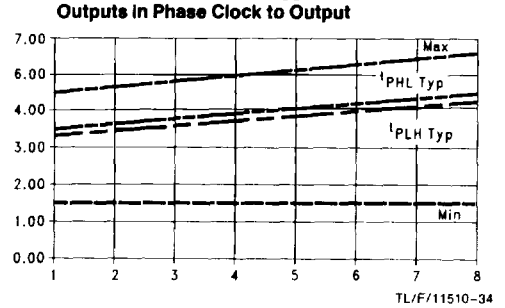
TL/F/11510–32

t_{PZL} vs Load Capacitance T_A = 25°C, 8 Outputs Switching $\overline{OE}$ to Output



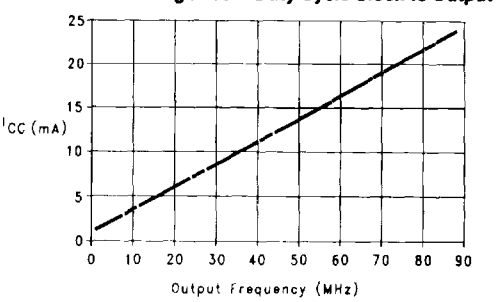
TL/F/11510–33

t_{PLH} and t_{PHL} vs Number Outputs Switching C_L = 50 pF, T_A = 25°C, V_{CC} = 5.0V, Outputs in Phase Clock to Output



TL/F/11510–34

Typical I_{CC} vs Output Switching Frequency C_L = 0 pF, V_{CC} = V_{IH} = 5.5V, 1 Output Switching at 50% Duty Cycle Clock to Output



TL/F/11510–35

Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Tables.