

74ABT544

Octal latched transceiver with dual enable; 3-state

Rev. 05 — 20 May 2010

Product data sheet

1. General description

The 74ABT544 high performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT544 octal latched transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate latch enable ($\overline{\text{LEAB}}$, $\overline{\text{LEBA}}$) and output enable ($\overline{\text{OEAB}}$, $\overline{\text{OEBA}}$) inputs are provided for each register to permit independent control of data transfer in either direction. The outputs are guaranteed to sink 64 mA.

2. Features and benefits

- Combines 74ABT640 and 74ABT373 type functions in one device
- 8-bit octal transceiver with D-type latch
- Back-to-back registers for storage
- Separate controls for data flow in each direction
- Live insertion and extraction permitted
- Output capability: +64 mA to -32 mA
- Power-up 3-state
- Power-up reset
- Latch-up protection exceeds 500 mA per JESD78B class II level A
- ESD protection:
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V

3. Ordering information

Table 1. Ordering information

| Type number | Package | | | Version |
|-------------|-------------------|---------|--|----------|
| | Temperature range | Name | Description | |
| 74ABT544D | -40 °C to +85 °C | SO24 | plastic small outline package; 24 leads; body width 7.5 mm | SOT137-1 |
| 74ABT544DB | -40 °C to +85 °C | SSOP24 | plastic shrink small outline package; 24 leads; body width 5.3 mm | SOT340-1 |
| 74ABT544PW | -40 °C to +85 °C | TSSOP24 | plastic thin shrink small outline package; 24 leads; body width 4.4 mm | SOT355-1 |



4. Functional diagram

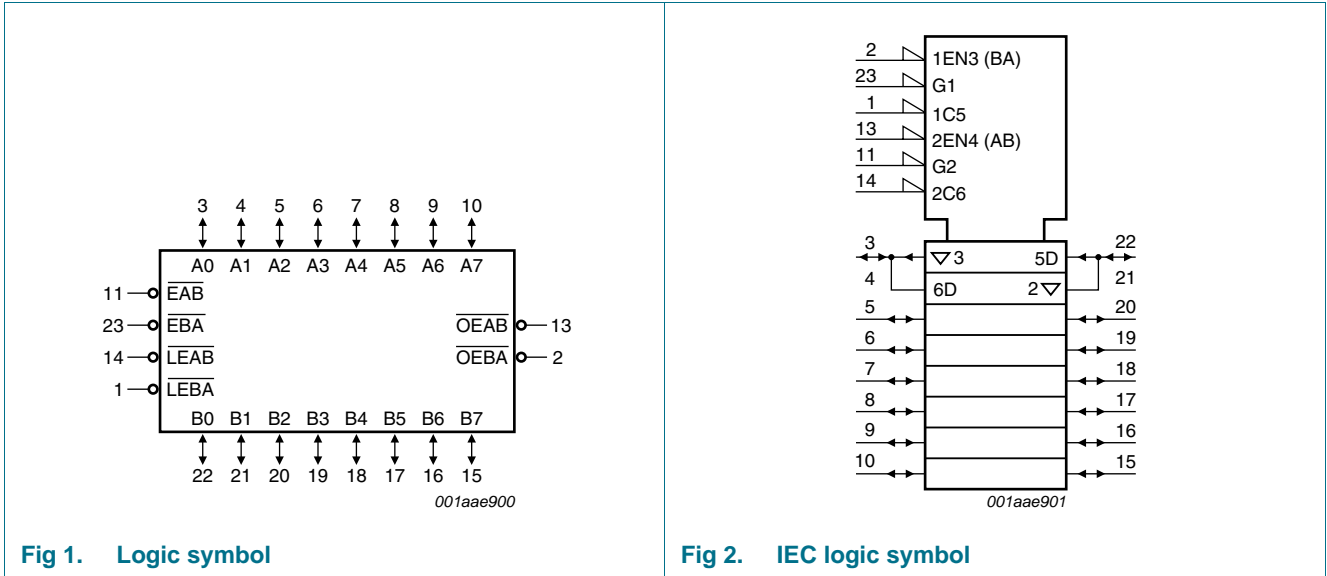


Fig 1. Logic symbol

Fig 2. IEC logic symbol

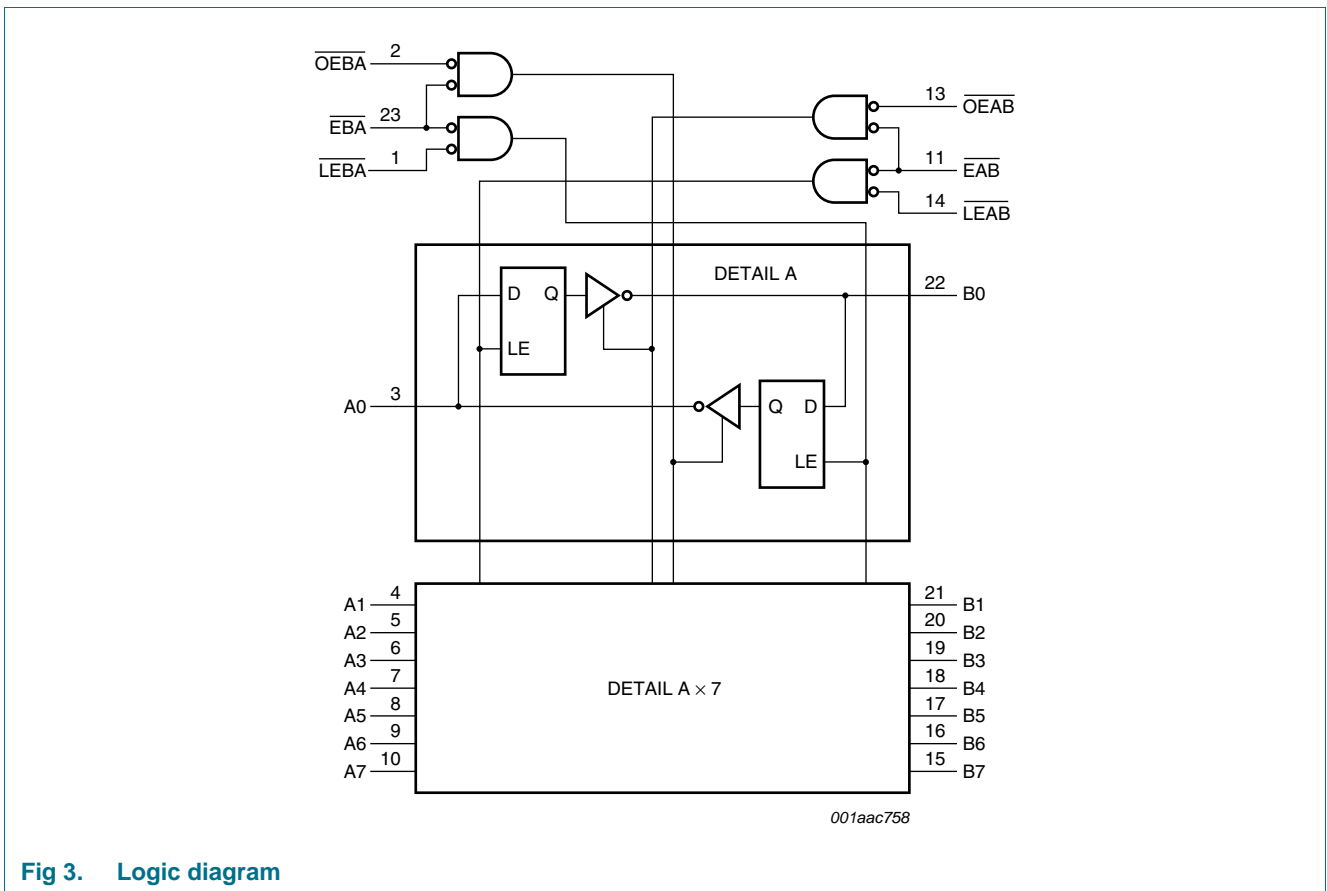


Fig 3. Logic diagram

5. Pinning information

5.1 Pinning

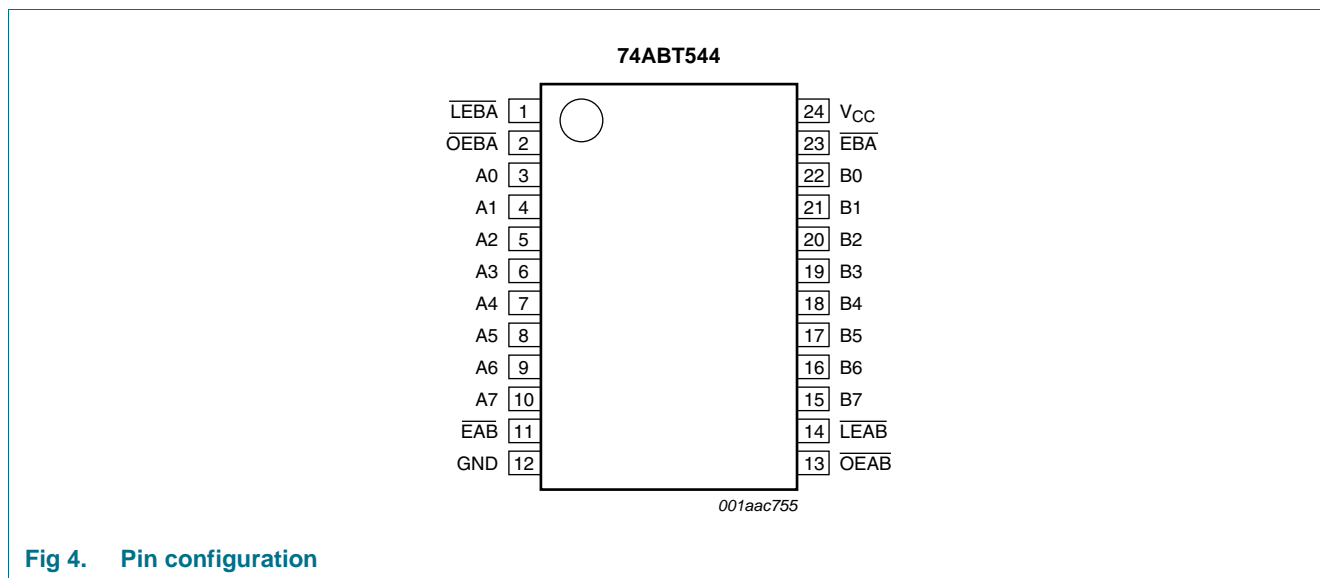


Fig 4. Pin configuration

5.2 Pin description

Table 2. Pin description

| Symbol | Pin | Description |
|--------------------------|--------------------------------|---|
| $\overline{\text{LEBA}}$ | 1 | B-to-A latch enable input (active LOW) |
| $\overline{\text{OEBA}}$ | 2 | B-to-A output enable input (active LOW) |
| A0 to A7 | 3, 4, 5, 6, 7, 8, 9, 10 | data input or output |
| $\overline{\text{EAB}}$ | 11 | A-to-B enable input (active LOW) |
| GND | 12 | ground (0 V) |
| $\overline{\text{OEAB}}$ | 13 | A-to-B output enable input (active LOW) |
| $\overline{\text{LEAB}}$ | 14 | A-to-B latch enable input (active LOW) |
| B0 to B7 | 22, 21, 20, 19, 18, 17, 16, 15 | data input or output |
| $\overline{\text{EBA}}$ | 23 | B-to-A enable input (active LOW) |
| V _{CC} | 24 | positive supply voltage |

6. Functional description

6.1 Function table

Table 3. Function selection^[1]

| Input | | | | Output | Status |
|-------|-----|------|----------|----------|------------------|
| OEXX | EXX | LEXX | An or Bn | Bn or An | |
| H | X | X | X | Z | disabled |
| X | H | X | X | Z | |
| L | ↑ | L | h | Z | disabled + latch |
| | | | l | Z | |
| L | L | ↑ | h | L | latch + display |
| | | | l | H | |
| L | L | L | H | L | transparent |
| | | | L | H | |
| L | L | H | X | NC | hold |

- [1] H = HIGH voltage level;
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition of $\overline{\text{LEXX}}$ or $\overline{\text{EXX}}$ (XX = AB or BA);
L = LOW voltage level;
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition of $\overline{\text{LEXX}}$ or $\overline{\text{EXX}}$ (XX = AB or BA);
↑ = LOW-to-HIGH clock transition of $\overline{\text{LEXX}}$ or $\overline{\text{EXX}}$ (XX = AB or BA);
NC = no change;
X = don't care;
Z = high-impedance OFF-state.

6.2 Description

The 74ABT544 contains two sets of eight D-type latches, with separate control pins for each set.

Using data flow from A-to-B as an example, when the A-to-B enable ($\overline{\text{EAB}}$) input, the A-to-B latch enable ($\overline{\text{LEAB}}$) input and the A-to-B output enable ($\overline{\text{OEAB}}$) input are all LOW, the A-to-B path is transparent.

A subsequent LOW-to-HIGH transition of the $\overline{\text{LEAB}}$ signal puts the A data into the latches where it is stored and the B outputs no longer change with the A inputs. With $\overline{\text{EAB}}$ and $\overline{\text{OEAB}}$ both LOW, the 3-state B output buffers are active and display the data present at the outputs of the A latches.

Control of data flow from B-to-A is similar, but using the $\overline{\text{EBA}}$, $\overline{\text{LEBA}}$, and $\overline{\text{OEBA}}$ inputs.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).
Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------|-------------------------|-----------------------------------|----------|------|------|
| V_{CC} | supply voltage | | -0.5 | +7.0 | V |
| V_I | input voltage | | [1] -1.2 | +7.0 | V |
| V_O | output voltage | output in OFF-state or HIGH-state | [1] -0.5 | +5.5 | V |
| I_{IK} | input clamping current | $V_I < 0$ V | -18 | - | mA |
| I_{OK} | output clamping current | $V_O < 0$ V | -50 | - | mA |
| I_O | output current | output in LOW-state | - | 128 | mA |
| T_j | junction temperature | | [2] - | 150 | °C |
| T_{stg} | storage temperature | | -65 | +150 | °C |

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------|-------------------------------------|-------------|-----|-----|----------|------|
| V_{CC} | supply voltage | | 4.5 | - | 5.5 | V |
| V_I | input voltage | | 0 | - | V_{CC} | V |
| V_{IH} | HIGH-level input voltage | | 2.0 | - | - | V |
| V_{IL} | LOW-level input voltage | | - | - | 0.8 | V |
| I_{OH} | HIGH-level output current | | -32 | - | - | mA |
| I_{OL} | LOW-level output current | | - | - | 64 | mA |
| $\Delta t/\Delta V$ | input transition rise and fall rate | | 0 | - | 10 | ns/V |
| T_{amb} | ambient temperature | in free air | -40 | - | +85 | °C |

9. Static characteristics

Table 6. Static characteristics

Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | Unit |
|----------|---------------------------|---|-------|------|------|------------------|------|------|
| | | | Min | Typ | Max | Min | Max | |
| V_{IK} | input clamping voltage | $V_{CC} = 4.5$ V; $I_{IK} = -18$ mA | -1.2 | -0.9 | - | -1.2 | - | V |
| V_{OH} | HIGH-level output voltage | $V_I = V_{IL}$ or V_{IH} | | | | | | |
| | | $V_{CC} = 4.5$ V; $I_{OH} = -3$ mA | 2.5 | 3.2 | - | 2.5 | - | V |
| | | $V_{CC} = 5.0$ V; $I_{OH} = -3$ mA | 3.0 | 3.7 | - | 3.0 | - | V |
| | | $V_{CC} = 4.5$ V; $I_{OH} = -32$ mA | 2.0 | 2.3 | - | 2.0 | - | V |
| V_{OL} | LOW-level output voltage | $V_{CC} = 4.5$ V; $I_{OL} = 64$ mA; $V_I = V_{IL}$ or V_{IH} | - | 0.42 | 0.55 | - | 0.55 | V |

Table 6. Static characteristics ...continued
 Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | Unit | |
|-----------------|------------------------------------|--|-------|------------|-----------|------------------|-----------|---------------|---------------|
| | | | Min | Typ | Max | Min | Max | | |
| $V_{OL(pu)}$ | power-up LOW-level output voltage | $V_{CC} = 5.5 \text{ V}; I_O = 1 \text{ mA}; V_I = \text{GND or } V_{CC}$ | [1] | - | 0.13 | 0.55 | - | 0.55 | V |
| I_I | input leakage current | $V_{CC} = 5.5 \text{ V}; V_I = \text{GND or } 5.5 \text{ V}$ | | | | | | | |
| | | control pins | - | ± 0.01 | ± 1.0 | - | ± 1.0 | μA | |
| | | An, Bn | - | ± 5.0 | ± 100 | - | ± 100 | μA | |
| I_{OFF} | power-off leakage current | $V_{CC} = 0 \text{ V}; V_I \text{ or } V_O \leq 4.5 \text{ V}$ | - | ± 5.0 | ± 100 | - | ± 100 | μA | |
| $I_{O(pu/pd)}$ | power-up/power-down output current | $V_{CC} = 2.1 \text{ V}; V_O = 0.5 \text{ V}; V_I = \text{GND or } V_{CC}; \text{OEAB, OEBA don't care}$ | [2] | - | ± 5.0 | ± 50 | - | ± 50 | μA |
| I_{OZ} | OFF-state output current | $V_{CC} = 5.5 \text{ V}; V_I = V_{IL} \text{ or } V_{IH}$ | | | | | | | |
| | | $V_O = 2.7 \text{ V}$ | - | 5.0 | 50 | - | 50 | μA | |
| | | $V_O = 0.5 \text{ V}$ | - | -5.0 | -50 | - | -50 | μA | |
| I_{LO} | output leakage current | HIGH-state; $V_O = 5.5 \text{ V}; V_{CC} = 5.5 \text{ V}; V_I = \text{GND or } V_{CC}$ | - | 5.0 | 50 | - | 50 | μA | |
| I_O | output current | $V_{CC} = 5.5 \text{ V}; V_O = 2.5 \text{ V}$ | [3] | -180 | -65 | -50 | -180 | -50 | mA |
| I_{CC} | supply current | $V_{CC} = 5.5 \text{ V}; V_I = \text{GND or } V_{CC}$ | | | | | | | |
| | | outputs HIGH-state | - | 110 | 250 | - | 250 | μA | |
| | | outputs LOW-state | - | 20 | 30 | - | 30 | mA | |
| | | outputs disabled | - | 110 | 250 | - | 250 | μA | |
| ΔI_{CC} | additional supply current | per input pin; $V_{CC} = 5.5 \text{ V};$ one input pin at 3.4 V, other inputs at V_{CC} or GND | [4] | - | 0.3 | 1.5 | - | 1.5 | mA |
| C_I | input capacitance | $V_I = 0 \text{ V or } V_{CC}$ | - | 4 | - | - | - | - | pF |
| $C_{I/O}$ | input/output capacitance | outputs disabled; $V_O = 0 \text{ V or } V_{CC}$ | - | 7 | - | - | - | - | pF |

[1] For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.

[2] This parameter is valid for any V_{CC} between 0 V and 2.1 V, with a transition time of up to 10 ms. From $V_{CC} = 2.1 \text{ V}$ to $V_{CC} = 5 \text{ V} \pm 10 \%$, a transition time of up to 100 μs is permitted.

[3] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

[4] This is the increase in supply current for each input at 3.4 V.

10. Dynamic characteristics

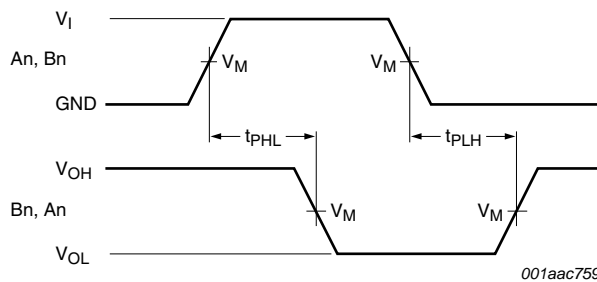
Table 7. Dynamic characteristics
 GND = 0 V; for test circuit, see Figure 10.

| Symbol | Parameter | Conditions | 25 °C; $V_{CC} = 5.0 \text{ V}$ | | | -40 °C to +85 °C; $V_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$ | | Unit |
|-----------|-------------------------------|--|---------------------------------|-----|-----|---|-----|------|
| | | | Min | Typ | Max | Min | Max | |
| t_{PLH} | LOW to HIGH propagation delay | An to Bn or Bn to An; see Figure 5 | 1.7 | 3.0 | 3.8 | 1.7 | 4.7 | ns |
| | | LEBA to An or LEAB to Bn; see Figure 6 | 2.1 | 3.5 | 4.2 | 2.1 | 5.2 | ns |

Table 7. Dynamic characteristics ...continued
GND = 0 V; for test circuit, see Figure 10.

| Symbol | Parameter | Conditions | 25 °C; V _{CC} = 5.0 V | | | -40 °C to +85 °C; V _{CC} = 5.0 V ± 0.5 V | | Unit |
|--------------------|-------------------------------------|--|--------------------------------|------|-----|--|-----|------|
| | | | Min | Typ | Max | Min | Max | |
| t _{PHL} | HIGH to LOW propagation delay | An to Bn or Bn to An; see Figure 5 | 2.4 | 3.6 | 4.5 | 2.4 | 5.2 | ns |
| | | $\overline{\text{LEBA}}$ to An or $\overline{\text{LEAB}}$ to Bn; see Figure 6 | 3.0 | 4.4 | 5.3 | 3.0 | 6.2 | ns |
| t _{PZH} | OFF-state to HIGH propagation delay | $\overline{\text{OEBA}}$ to An, $\overline{\text{OEAB}}$ to Bn; see Figure 7 | 1.8 | 3.0 | 3.9 | 1.8 | 4.7 | ns |
| | | $\overline{\text{EBA}}$ to An, $\overline{\text{EAB}}$ to Bn; see Figure 7 | 1.9 | 3.4 | 4.1 | 1.9 | 5.0 | ns |
| t _{PZL} | OFF-state to LOW propagation delay | $\overline{\text{OEBA}}$ to An, $\overline{\text{OEAB}}$ to Bn; see Figure 8 | 2.9 | 4.2 | 5.2 | 2.9 | 6.1 | ns |
| | | $\overline{\text{EBA}}$ to An, $\overline{\text{EAB}}$ to Bn; see Figure 8 | 3.1 | 4.6 | 5.5 | 3.1 | 6.5 | ns |
| t _{PHZ} | HIGH to OFF-state propagation delay | $\overline{\text{OEBA}}$ to An, $\overline{\text{OEAB}}$ to Bn; see Figure 7 | 2.0 | 3.3 | 4.3 | 2.0 | 4.9 | ns |
| | | $\overline{\text{EBA}}$ to An, $\overline{\text{EAB}}$ to Bn; see Figure 7 | 2.1 | 3.4 | 4.5 | 2.1 | 5.2 | ns |
| t _{PLZ} | LOW to OFF-state propagation delay | $\overline{\text{OEBA}}$ to An, $\overline{\text{OEAB}}$ to Bn; see Figure 8 | 2.0 | 2.8 | 5.8 | 2.0 | 6.3 | ns |
| | | $\overline{\text{EBA}}$ to An, $\overline{\text{EAB}}$ to Bn; see Figure 8 | 2.0 | 3.0 | 6.2 | 2.0 | 6.7 | ns |
| t _{su(H)} | set-up time HIGH | An to $\overline{\text{LEAB}}$, Bn to $\overline{\text{LEBA}}$; see Figure 9 | 3.0 | 1.5 | - | 3.0 | - | ns |
| | | An to $\overline{\text{EAB}}$, Bn to $\overline{\text{EBA}}$; see Figure 9 | 3.0 | 1.5 | - | 3.0 | - | ns |
| t _{su(L)} | set-up time LOW | An to $\overline{\text{LEAB}}$, Bn to $\overline{\text{LEBA}}$; see Figure 9 | 3.0 | 0.6 | - | 3.0 | - | ns |
| | | An to $\overline{\text{EAB}}$, Bn to $\overline{\text{EBA}}$; see Figure 9 | 3.0 | 0.6 | - | 3.0 | - | ns |
| t _{h(H)} | hold time HIGH | $\overline{\text{LEAB}}$ to An, $\overline{\text{LEBA}}$ to Bn; see Figure 9 | +0.5 | -0.3 | - | 0.5 | - | ns |
| | | $\overline{\text{EAB}}$ to An, $\overline{\text{EBA}}$ to Bn; see Figure 9 | +0.5 | -0.2 | - | 0.5 | - | ns |
| t _{h(L)} | hold time LOW | $\overline{\text{LEAB}}$ to An, $\overline{\text{LEBA}}$ to Bn; see Figure 9 | +0.5 | -1.3 | - | 0.5 | - | ns |
| | | $\overline{\text{EAB}}$ to An, $\overline{\text{EBA}}$ to Bn; see Figure 9 | +0.5 | -1.3 | - | 0.5 | - | ns |
| t _{WL} | pulse width LOW | latch enable; see Figure 9 | 3.5 | 1.8 | - | 3.5 | - | ns |

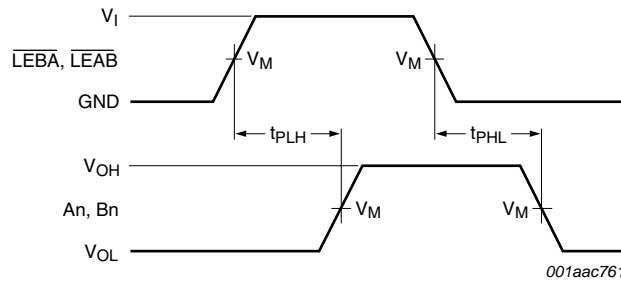
11. Waveforms



V_M = 1.5 V

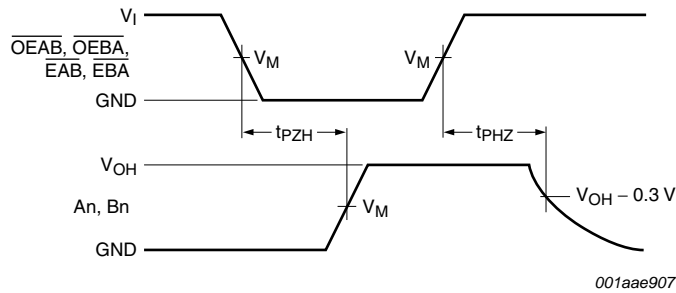
V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 5. Propagation delay input (An, Bn) to output (Bn, An)



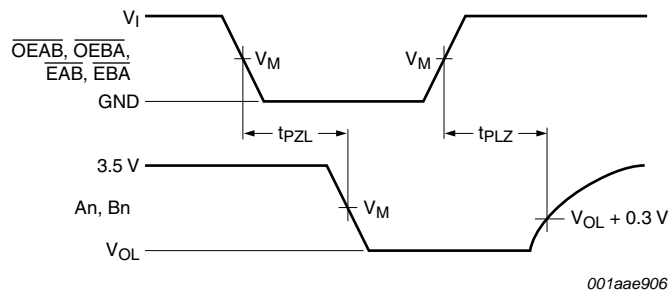
$V_M = 1.5\text{ V}$
 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 6. Propagation delay latch enable ($\overline{LEAB}, \overline{LEBA}$) to output (An, Bn)



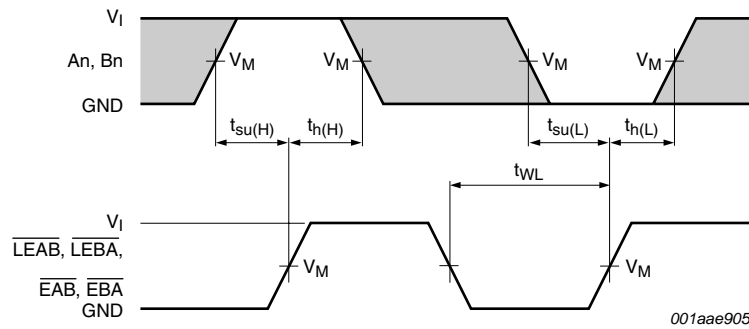
$V_M = 1.5\text{ V}$
 V_{OH} is a typical voltage output level that occurs with the output load.

Fig 7. Propagation delay 3-state output enable to HIGH-level and output disable from HIGH-level



$V_M = 1.5\text{ V}$
 V_{OL} is a typical voltage output level that occurs with the output load.

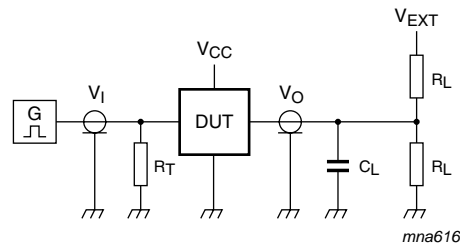
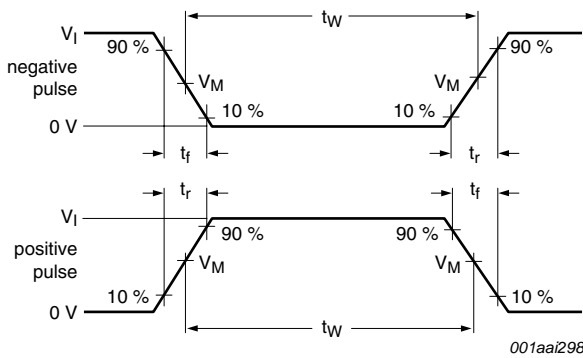
Fig 8. Propagation delay 3-state output enable to LOW-level and output disable from LOW-level



$V_M = 1.5\text{ V}$

The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig 9. Data set-up and hold times and latch enable pulse width



a. Input pulse definition

Test data is given in [Table 8](#).

Definitions test circuit:

R_L = Load resistor.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = Test voltage for switching times.

b. Test circuit

Fig 10. Load circuitry for switching times

Table 8. Test data

| Input | | | | Load | | V_{EXT} | | |
|-------|-------|--------|----------------------|-------|--------------|--------------------|--------------------|--------------------|
| V_I | f_i | t_w | t_r, t_f | C_L | R_L | t_{PHL}, t_{PLH} | t_{PZH}, t_{PHZ} | t_{PZL}, t_{PLZ} |
| 3.0 V | 1 MHz | 500 ns | $\leq 2.5\text{ ns}$ | 50 pF | 500 Ω | open | open | 7.0 V |

12. Package outline

SO24: plastic small outline package; 24 leads; body width 7.5 mm

SOT137-1

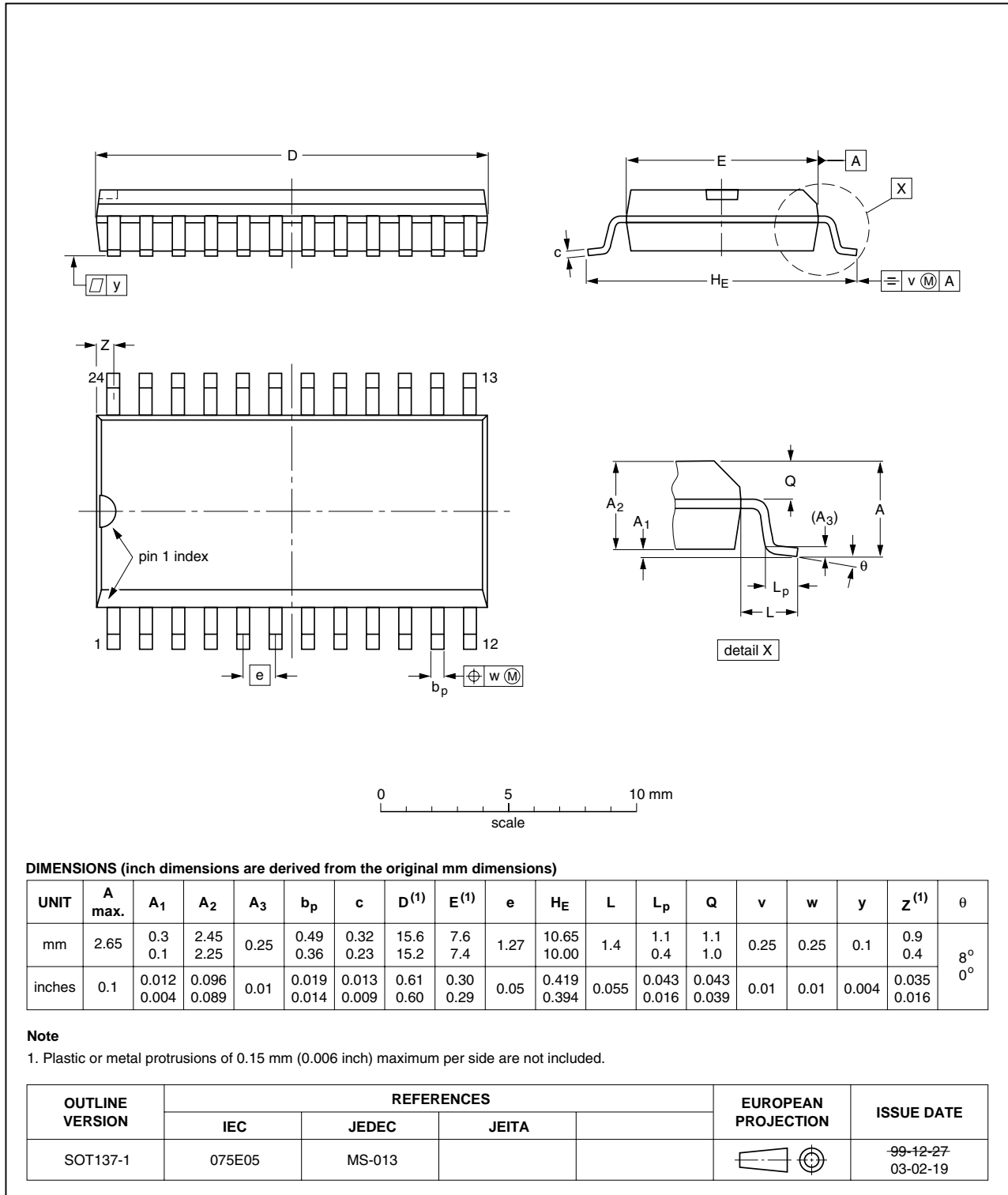


Fig 11. Package outline SOT137-1 (SO24)

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm

SOT340-1

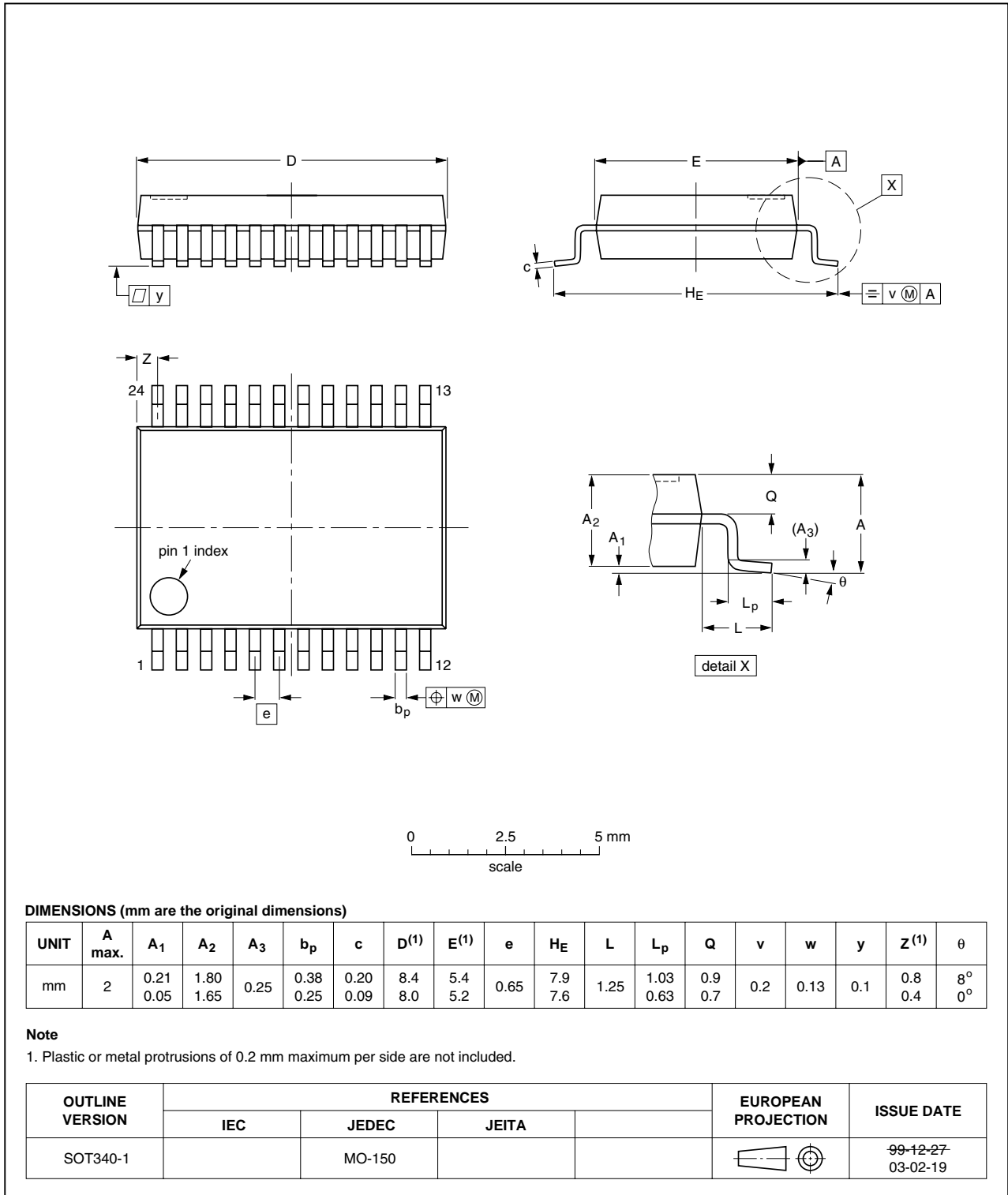


Fig 12. Package outline SOT340-1 (SSOP24)

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm

SOT355-1

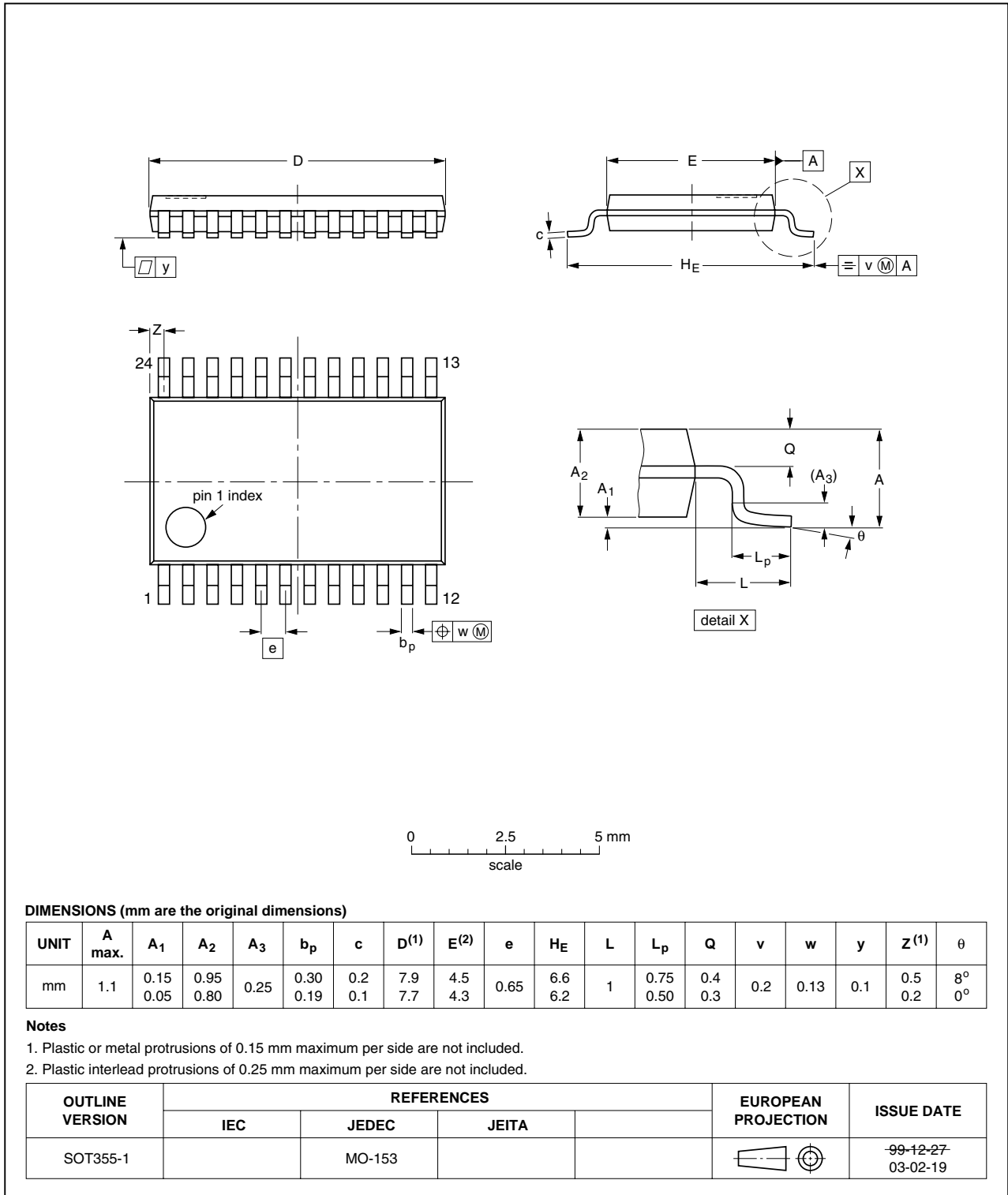


Fig 13. Package outline SOT355-1 (TSSOP24)

13. Abbreviations

Table 9. Abbreviations

| Acronym | Description |
|---------|---|
| BICMOS | Bipolar Complementary Metal-Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| MM | Machine Model |

14. Revision history

Table 10. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|----------------|---|-----------------------|---------------|------------|
| 74ABT544 v.5 | 20100520 | Product data sheet | - | 74ABT544_4 |
| Modifications: | <ul style="list-style-type: none"> • Table 6 , Table note 2 transition time corrected. | | | |
| 74ABT544_4 | 20100115 | Product data sheet | - | 74ABT544_3 |
| Modifications: | <ul style="list-style-type: none"> • The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. | | | |
| 74ABT544_3 | 20050420 | Product specification | - | 74ABT544_2 |
| 74ABT544_2 | 20021118 | Product specification | - | 74ABT544 |
| 74ABT544 | 19930701 | Product specification | - | - |

15. Legal information

15.1 Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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