National Semiconductor

74ABT652
Octal Transceivers and Registers with TRI-STATE® Outputs

General Description

The 'ABT652 consists of bus transceiver circuits with D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to HIGH logic level. Output Enable pins (OEAB, $\overline{OEBA}$) are provided to control the transceiver function.

Features

- Independent registers for A and B buses
- Multiplexed real-time and stored data
- A and B output sink capability of 64 mA, source capability of 32 mA
- Guaranteed output skew
- Guaranteed multiple output switching specifications
- Output switching specified for both 50 pF and 250 pF loads
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Nondestructive hot insertion capability

Ordering Code: See Section 10

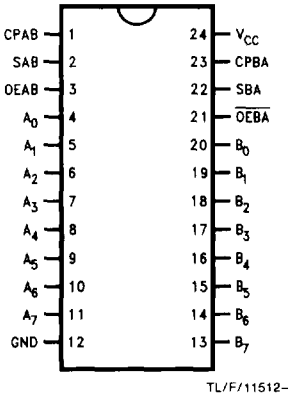
Commercial	Package Number	Package Description
74ABT652CSC (Note 1)	M24B	24-Lead (0.300" Wide) Molded Small Outline, JEDEC
74ABT652CMSA (Note 1)	MSA24	24-Lead Molded Shrink Small Outline, EIAJ Type II
74ABT652CMTC (Notes 1, 2)	MTC24	24-Lead Molded Thin Shrink Small Outline, JEDEC

Note 1: Devices also available in 13" reel. Use suffix = SCX, MSAX and MTCX.

Note 2: Contact factory for package availability.

Connection Diagram

Pin Assignment for DIP, SOIC and SSOP



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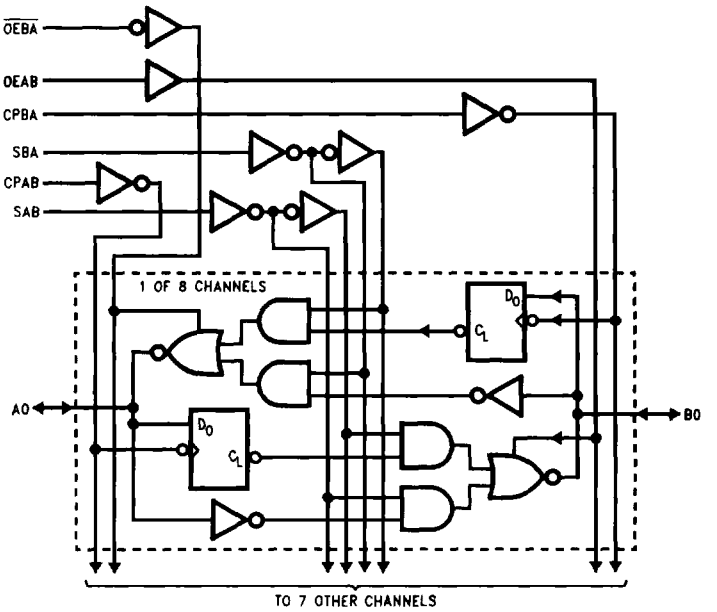
Pin Descriptions

Pin Names	Description
A_0–A_7	Data Register A Inputs/TRI-STATE Outputs
B_0–B_7	Data Register B Inputs/TRI-STATE Outputs
CPAB, CPBA	Clock Pulse Inputs
SAB, SBA	Select Inputs
OEAB, $\overline{OEBA}$	Output Enable Inputs

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Functional Description

In the transceiver mode, data present at the HIGH impedance port may be stored in either the A or B register or both.

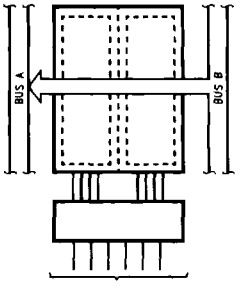
The select (SAB, SBA) controls can multiplex stored and real-time.

The examples in *Figure 1* demonstrate the four fundamental bus-management functions that can be performed with the 'ABT652C.

Data on the A or B data bus, or both can be stored in the internal D flip-flop by LOW to HIGH transitions at the appropriate Clock Inputs (CPAB, CPBA) regardless of the Select or Output Enable Inputs. When SAB and SBA are in the real time transfer mode, it is also possible to store data without using the internal D flip-flops by simultaneously enabling OEAB and $\overline{\text{OEBA}}$. In this configuration each Output reinforces its Input. Thus when all other data sources to the two sets of bus lines are in a HIGH Impedance state, each set of bus lines will remain at its last state.

Functional Description (Continued)

Note A: Real-Time Transfer Bus B to Bus A



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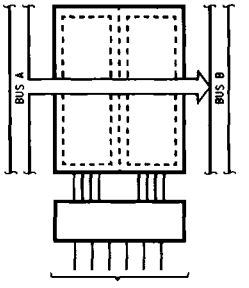
OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA
L	L	X	X	X	L

Note B: Real-Time Transfer Bus A to Bus B



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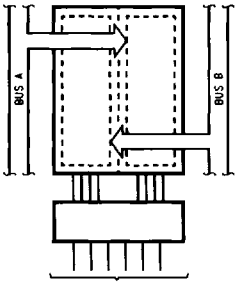
OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA
H	H	X	X	L	X

Note C: Storage



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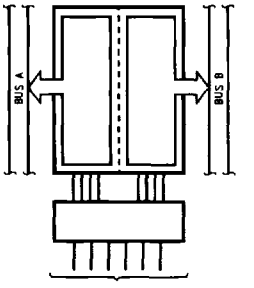
OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA
X	H	⌐	X	X	X
L	X	X	⌐	X	X
L	H	⌐	⌐	X	X

Note D: Transfer Storage Data to A or B



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OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA
H	L	H or L	H or L	H	H

FIGURE 1

Inputs						Inputs/Outputs (Note 1)		Operating Mode
OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA	A_0 thru A_7	B_0 thru B_7	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	⌐	⌐	X	X			Store A and B Data
X	H	⌐	H or L	X	X	Input	Not Specified	Store A, Hold B
H	H	⌐	⌐	X	X	Input	Output	Store A in Both Registers
L	X	H or L	⌐	X	X	Not Specified	Input	Hold A, Store B
L	L	⌐	⌐	X	X	Output	Input	Store B in Both Registers
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus
L	L	X	H or L	X	H			Store B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus
H	H	H or L	X	H	X			Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored A Data to B Bus and Stored B Data to A Bus

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐ = LOW to HIGH Clock Transition

Note 1: The data output functions may be enabled or disabled by various signals at OEAB or $\overline{OEBA}$ inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW to HIGH transition on the clock inputs.

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Absolute Maximum Ratings (Note 1)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Any Output	
in the Disable or Power-Off State	−0.5V to +5.5V
in the HIGH State	−0.5V to V_{CC}
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)
DC Latchup Source Current	−500 mA
Over Voltage Latchup (I/O)	10V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Commercial	−40°C to +85°C
Supply Voltage	
Commercial	+4.5V to +5.5V
Minimum Input Edge Rate	(ΔV/Δt)
Data Input	50 mV/ns
Enable Input	20 mV/ns
Clock Input	100 mV/ns

DC Electrical Characteristics

Symbol	Parameter	ABT652 Min	ABT652 Typ	ABT652 Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage	2.0			V		Recognized HIGH Signal
V_{IL}	Input LOW Voltage			0.8	V		Recognized LOW Signal
V_{CD}	Input Clamp Diode Voltage			−1.2	V	Min	I_{IN} = −18 mA (Non I/O Pins)
V_{OH}	Output HIGH 74ABT Voltage 74ABT	2.5 2.0			V	Min	I_{OH} = −3 mA, (A_n, B_n) I_{OH} = −32 mA, (A_n, B_n)
V_{OL}	Output LOW 74ABT Voltage			0.55	V	Min	I_{OL} = 64 mA, (A_n, B_n)
V_{ID}	Input Leakage Test	4.75			V	0.0	I_{ID} = 1.9 μA, (Non-I/O Pins) All Other Pins Grounded
I_{IH}	Input HIGH Current			5	μA	Max	V_{IN} = 2.7V (Non-I/O Pins) (Note 3) V_{IN} = V_{CC} (Non-I/O Pins)
I_{BVI}	Input HIGH Current Breakdown Test			7	μA	Max	V_{IN} = 7.0V (Non-I/O Pins)
I_{BVIT}	Input HIGH Current Breakdown Test (I/O)			100	μA	Max	V_{IN} = 5.5V (A_n, B_n)
I_{IL}	Input LOW Current			−5	μA	Max	V_{IN} = 0.5V (Non-I/O Pins) (Note 3) V_{IN} = 0.0V (Non-I/O Pins)
I_{IH} + I_{OZH}	Output Leakage Current			50	μA	0V–5.5V	V_{OUT} = 2.7V (A_n, B_n); $\overline{OEBA}$ = 2.0V and OEAB = GND = 2.0V
I_{IL} + I_{OZL}	Output Leakage Current			−50	μA	0V–5.5V	V_{OUT} = 0.5V (A_n, B_n); $\overline{OEBA}$ = 2.0V and OEAB = GND = 2.0V

Note 3: Guaranteed but not tested.

DC Electrical Characteristics (Continued)

Symbol	Parameter	ABT652			Units	V_{CC}	Conditions
		Min	Typ	Max			
I_{OS}	Output Short-Circuit Current	−100		−275	mA	Max	V_{OUT} = 0V (A_n, B_n)
I_{CEX}	Output HIGH Leakage Current			50	μA	Max	V_{OUT} = V_{CC} (A_n, B_n)
I_{ZZ}	Bus Drainage Test			100	μA	0.0V	V_{OUT} = 5.5V (A_n, B_n); All Others GND
I_{CCH}	Power Supply Current			250	μA	Max	All Outputs HIGH
I_{CCL}	Power Supply Current			30	mA	Max	All Outputs LOW
I_{CCZ}	Power Supply Current			50	μA	Max	Outputs TRI-STATE; All others at V_{CC} or GND
I_{CCT}	Additional I_{CC}/Input			2.5	mA	Max	V_I = V_{CC} − 2.1V All others at V_{CC} or GND
I_{CCD}	Dynamic I_{CC} No Load (Note 2)			0.18	mA/MHz	Max	Outputs Open (Note 1) OEAB = $\overline{OEBA}$ = GND One bit toggling, 50% duty cycle (Note 1)

Note 1: For 8 outputs toggling, I_{CCD} < 1.4 mA/MHz.

Note 2: Guaranteed, but not tested.

DC Electrical Characteristics (SOIC package)

Symbol	Parameter	Min	Typ	Max	Units	V_{CC}	Conditions C_L = 50 pF, R_L = 500Ω
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}		0.6	0.8	V	5.0	T_A = 25°C (Note 1)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	−1.2	−0.9		V	5.0	T_A = 25°C (Note 1)
V_{OHV}	Minimum High Level Dynamic Output Voltage	2.5	3.0		V	5.0	T_A = 25° (Note 3)
V_{IHD}	Minimum High Level Dynamic Input Voltage	2.2	1.8		V	5.0	T_A = 25°C (Note 2)
V_{ILD}	Maximum Low Level Dynamic Input Voltage		0.8	0.4	V	5.0	T_A = 25°C (Note 2)

Note 1: Max number of outputs defined as (n). n − 1 data inputs are driven 0V to 3V. One output at LOW. Guaranteed, but not tested.

Note 2: Max number of data inputs (n) switching. n − 1 inputs switching 0V to 3V. Input-under-test switching: 3V to theshold (V_{ILD}), 0V to threshold (V_{IHD}). Guaranteed, but not tested.

Note 3: Max number of outputs defined as (n). n − 1 data inputs are driven 0V to 3V. One output HIGH. Guaranteed, but not tested.

AC Electrical Characteristics (SOIC and SSOP package): See Section 2 for Waveforms

Symbol	Parameter	74ABT T_A = +25°C V_{CC} = +5.0V C_L = 50 pF			74ABT T_A = −40°C to +85°C V_{CC} = 4.5V–5.5V C_L = 50 pF		Units	Fig. No.
		Min	Typ	Max	Min	Max		
f_{max}	Max Clock Frequency	200			200		MHz	
t_{PLH} t_{PHL}	Propagation Delay Clock to Bus	1.7 1.7	3.0 3.4	4.9 4.9	1.7 1.7	4.9 4.9	ns	2-3, 5
t_{PLH} t_{PHL}	Propagation Delay Bus to Bus	1.5 1.5	2.6 3.0	4.5 4.5	1.5 1.5	4.5 4.5	ns	2-3, 5
t_{PLH} t_{PHL}	Propagation Delay SBA or SAB to A_n to B_n	1.5 1.5	3.0 3.4	5.0 5.0	1.5 1.5	5.0 5.0	ns	2-3, 5
t_{PZH} t_{PZL}	Enable Time $\overline{OEBA}$ or OEAB to A_n or B_n	1.5 1.5	3.3 3.7	5.5 5.5	1.5 1.5	5.5 5.5	ns	2-4
t_{PHZ} t_{PLZ}	Disable Time $\overline{OEBA}$ or OEAB to A_n or B_n	1.5 1.5	3.7 3.3	6.0 6.0	1.5 1.5	6.0 6.0	ns	2-4

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	74ABT $T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF		74ABT $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V-5.5V$, $C_L = 50$ pF		Units	Fig. No.
		Min	Max	Min	Max		
$t_S(H)$ $t_S(L)$	Setup Time, HIGH or LOW Bus to Clock	1.5		1.5		ns	2-6
$t_H(H)$ $t_H(L)$	Hold Time, HIGH or LOW Bus to Clock	1.0		1.0		ns	2-6
$t_W(H)$ $t_W(L)$	Pulse Width, HIGH or LOW	3.0		3.0		ns	2-3

Extended AC Electrical Characteristics (SOIC package): See Section 2 for Waveforms

Symbol	Parameter	74ABT $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V-5.5V$, $C_L = 50$ pF, 8 Outputs Switching (Note 4)		74ABT $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V-5.5V$, $C_L = 250$ pF, 1 Output Switching (Note 5)		74ABT $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V-5.5V$, $C_L = 250$ pF, 8 Outputs Switching (Note 6)		Units	Fig. No.
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Progagation Delay Clock to Bus	1.5 1.5	5.5 5.5	2.0 2.0	7.5 7.5	2.5 2.5	10.0 10.0	ns	2-3, 5
t_{PLH} t_{PHL}	Progagation Delay Bus to Bus	1.5 1.5	6.0 6.0	2.0 2.0	7.0 7.0	2.5 2.5	9.5 9.5	ns	2-3, 5
t_{PLH} t_{PHL}	Progagation Delay SBA or SAB to A_n or B_n	1.5 1.5	6.0 6.0	2.0 2.0	7.5 7.5	2.5 2.5	10.0 10.0	ns	2-3, 5
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEBA}$ or OEAB to A_n or B_n	1.5 1.5	6.0 6.0	2.0 2.0	8.0 8.0	2.5 2.5	11.5 11.5	ns	2-4
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OEBA}$ or OEAB to A_n or B_n	1.5 1.5	6.0 6.0	(Note 7)		(Note 7)		ns	2-4

Note 4: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.).

Note 5: This specification is guaranteed but not tested. The limits represent propagation delay with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

Note 6: This specification is guaranteed but not tested. The limits represent propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.) with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

Note 7: The TRI-STATE delay times are dominated by the RC network (500Ω, 250 pF) on the output and has been excluded from the datasheet.

Skew: See Section 2 (SOIC Package)

Symbol	Parameter	74ABT $T_A = -40°C$ to $+85°C$ $V_{CC} = 4.5V-5.5V$ $C_L = 50$ pF 8 Outputs Switching (Note 3)	74ABT $T_A = -40°C$ to $+85°C$ $V_{CC} = 4.5V-5.5V$ $C_L = 250$ pF 8 Outputs Switching (Note 4)	Units	Fig. No.
		Max	Max		
t_{OSHL} (Note 1)	Pin to Pin Skew HL Transitions	1.3	2.5	ns	2-13
t_{OSLH} (Note 1)	Pin to Pin Skew LH Transitions	1.0	2.0	ns	2-13
t_{PS} (Note 5)	Duty Cycle LH–HL Skew	2.0	4.0	ns	2-14
t_{OST} (Note 1)	Pin to Pin Skew LH/HL Transitions	2.0	4.0	ns	2-17
t_{PV} (Note 2)	Device to Device Skew LH/HL Transitions	2.5	4.5	ns	2-20

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH to LOW (t_{OSHL}), LOW to HIGH (t_{OSLH}), or any combination switching LOW to HIGH and/or HIGH to LOW (t_{OST}). This specification is guaranteed but not tested.

Note 2: Propagation delay variation for a given set of conditions (i.e., temperature and V_{CC}) from device to device. This specification is guaranteed but not tested.

Note 3: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.).

Note 4: This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

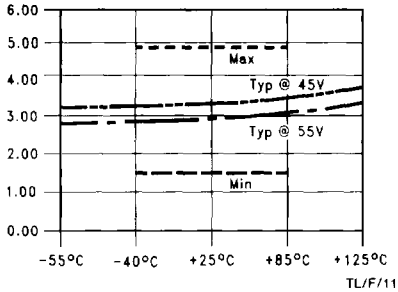
Note 5: This describes the difference between the delay of the LOW-to-HIGH and the HIGH-to-LOW transition on the same pin. It is measured across all the outputs (drivers) on the same chip, the worst (largest delta) number is the guaranteed specification. This specification is guaranteed but not tested.

Capacitance

Symbol	Parameter	Typ	Units	Conditions ($T_A = 25°C$)
C_{IN}	Input Capacitance	5.0	pF	$V_{CC} = 0V$ (non I/O pins)
$C_{I/O}$ (Note 1)	I/O Capacitance	11.0	pF	$V_{CC} = 5.0V$ (A_n, B_n)

Note 1: $C_{I/O}$ is measured at frequency, f = 1 MHz, per MIL-STD-883D, Method 3012.

t_{PLH} vs Temperature (T_A)
$C_L = 50$ pF, 1 Output Switching
Clock to Bus



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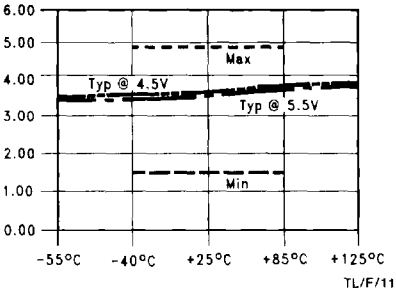
t_{PHL} vs Temperature (T_A)
$C_L = 50$ pF, 1 Output Switching
Clock to Bus



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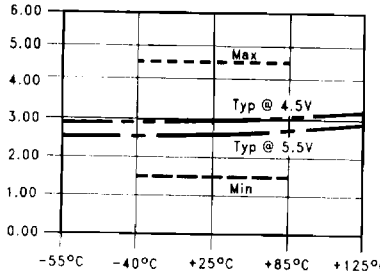
t_{PLH} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching
Bus to Bus



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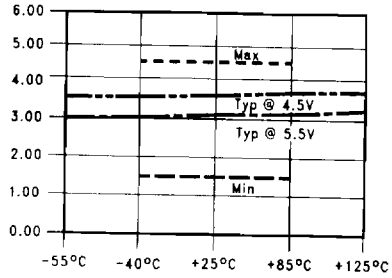
t_{PHL} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching
Bus to Bus



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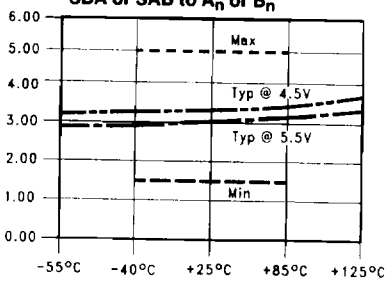
t_{PLH} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching
SBA or SAB to A_n or B_n



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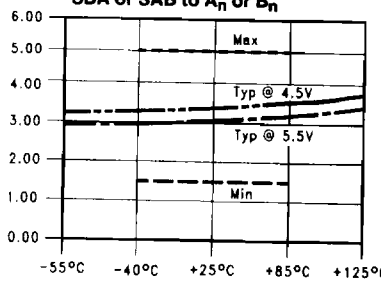
t_{PHL} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching
SBA or SAB to A_n or B_n



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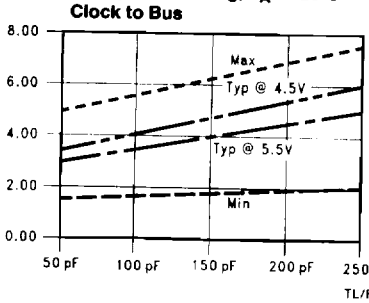
t_{PLH} vs Load Capacitance
1 Output Switching, T_A = 25°C
Clock to Bus



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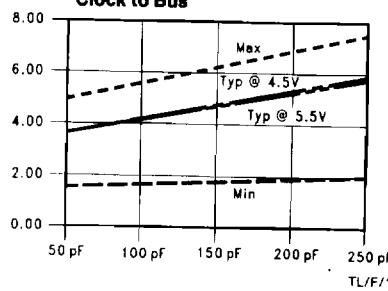
t_{PHL} vs Load Capacitance
1 Output Switching, T_A = 25°C
Clock to Bus



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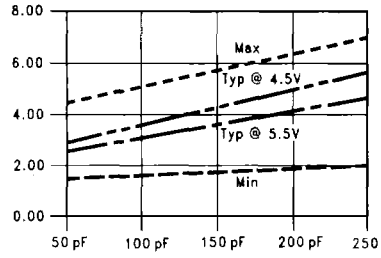
t_{PLH} vs Load Capacitance
1 Output Switching, T_A = 25°C
Bus to Bus



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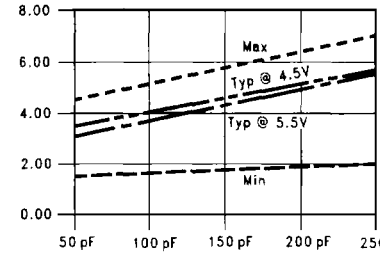
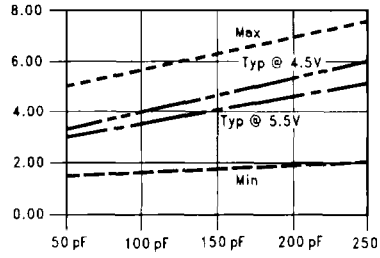
t_{PHL} vs Load Capacitance
1 Output Switching, T_A = 25°C
Bus to Bus



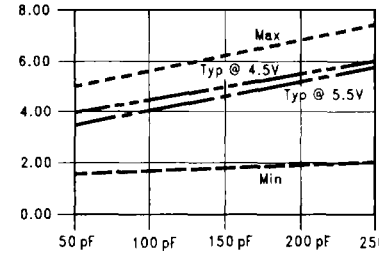
TL/F/11512-25

t_{PLH} vs Load Capacitance
1 Output Switching, T_A = 25°C
SBA or SAB to A_n or B_n



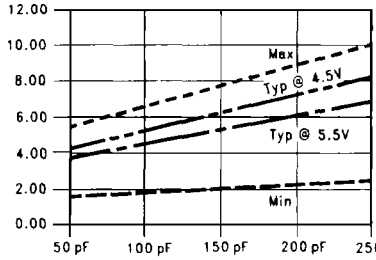
TL/F/11512-26

t_{PHL} vs Load Capacitance
1 Output Switching, T_A = 25°C
SBA or SAB to A_n or B_n



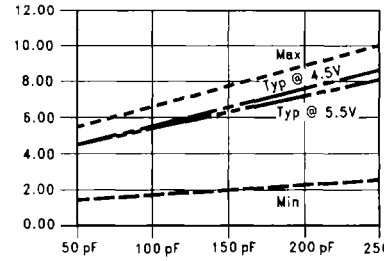
TL/F/11512-27

t_{PLH} vs Load Capacitance
8 Outputs Switching, T_A = 25°C
Clock to Bus



TL/F/11512-28

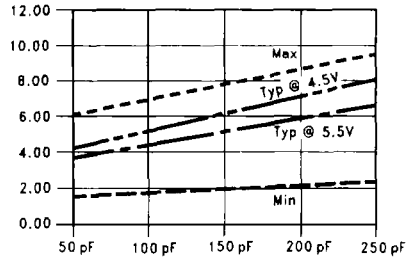
t_{PHL} vs Load Capacitance
8 Outputs Switching, T_A = 25°C
Clock to Bus



TL/F/11512-29

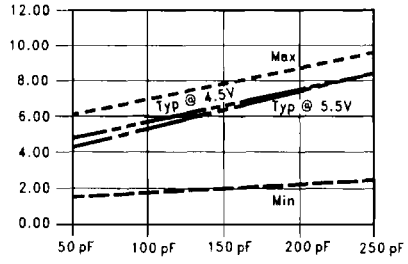
5

t_{PLH} vs Load Capacitance
8 Outputs Switching, T_A = 25°C
Bus to Bus



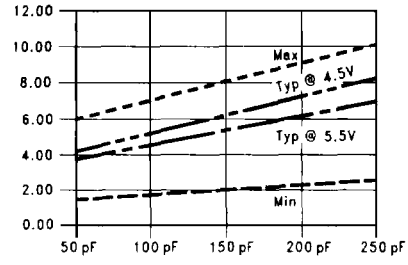
TL/F/11512-30

t_{PHL} vs Load Capacitance
8 Outputs Switching, T_A = 25°C
Bus to Bus



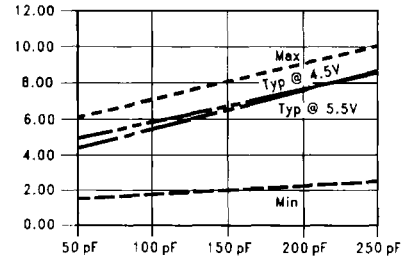
TL/F/11512-31

t_{PLH} vs Load Capacitance
8 Outputs Switching, T_A = 25°C
SBA or SAB to A_n or B_n



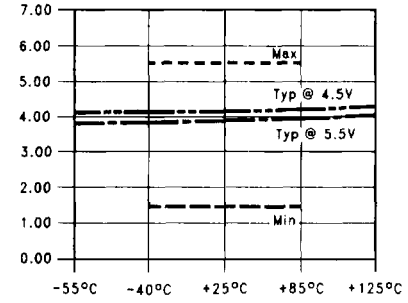
TL/F/11512-32

t_{PHL} vs Load Capacitance
8 Outputs Switching, T_A = 25°C
SBA or SAB to A_n or B_n



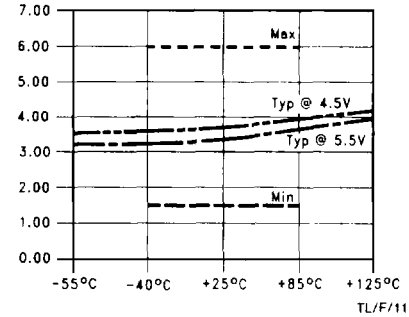
TL/F/11512-33

t_{PZL} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching



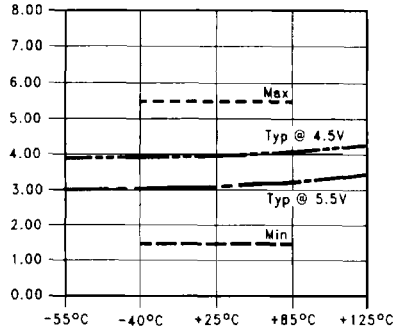
TL/F/11512-34

t_{PLZ} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching



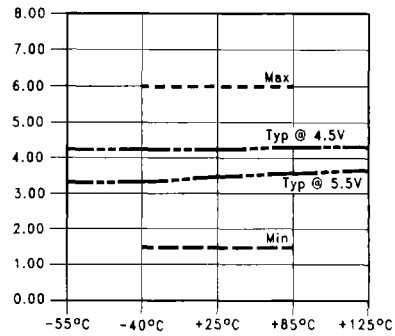
TL/F/11512-35

t_{PZH} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching



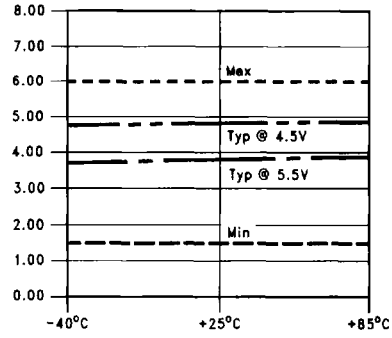
TL/F/11512-36

t_{PHZ} vs Temperature (T_A)
C_L = 50 pF, 1 Output Switching



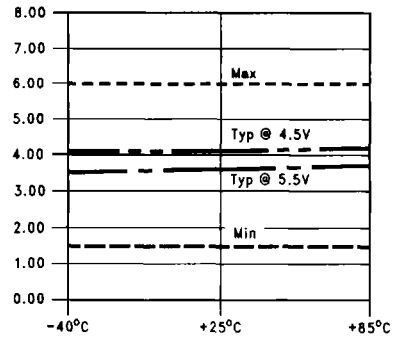
TL/F/11512-37

t_{PZH} vs Temperature (T_A)
C_L = 50 pF, 8 Outputs Switching



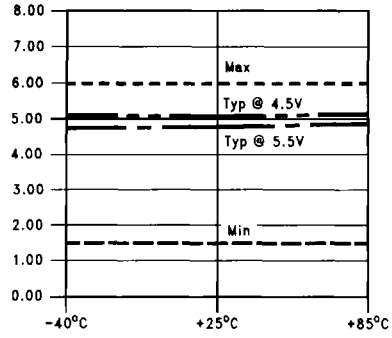
TL/F/11512-38

t_{PHZ} vs Temperature (T_A)
C_L = 50 pF, 8 Outputs Switching



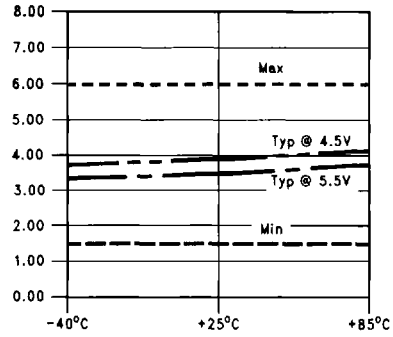
TL/F/11512-39

t_{PZL} vs Temperature (T_A)
C_L = 50 pF, 8 Outputs Switching



TL/F/11512-40

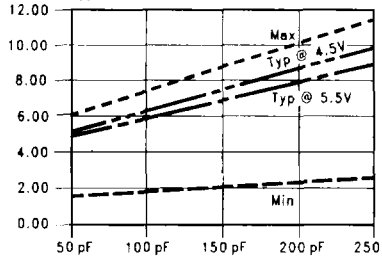
t_{PLZ} vs Temperature (T_A)
C_L = 50 pF, 8 Outputs Switching



TL/F/11512-41

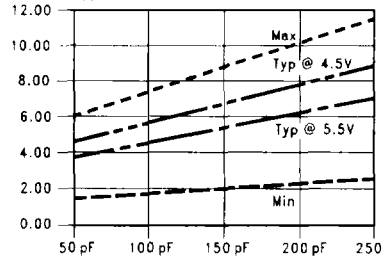
5

t_{PZL} vs Load Capacitance
8 Outputs Switching
T_A = 25°C



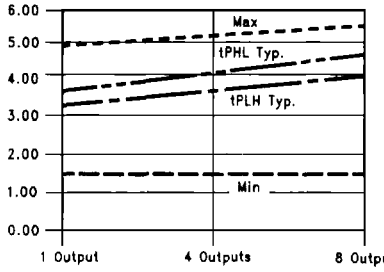
TL/F/11512–42

t_{PZH} vs Load Capacitance
8 Outputs Switching
T_A = 25°C



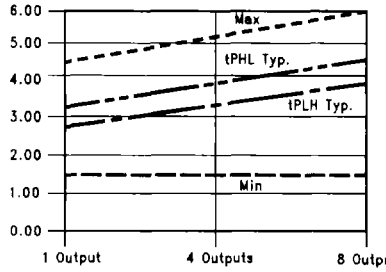
TL/F/11512–43

t_{PLH} and t_{PHL} vs Number Output Switching
V_{CC} = 5V, T_A = 25°C, C_L = 50 pF
Clock to Bus



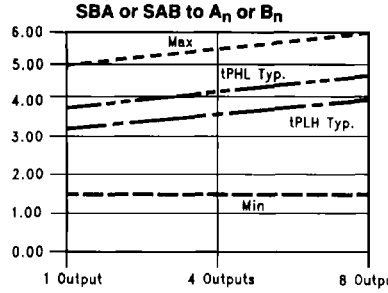
TL/F/11512–44

t_{PLH} and t_{PHL} vs Number Output Switching
V_{CC} = 5V, T_A = 25°C, C_L = 50 pF
Bus to Bus



TL/F/11512–45

t_{PLH} and t_{PHL} vs Number Output Switching
V_{CC} = 5V, T_A = 25°C, C_L = 50 pF
SBA or SAB to A_n or B_n



TL/F/11512–46