

54AC/74AC174 • 54ACT/74ACT174 Hex D Flip-Flop with Master Reset

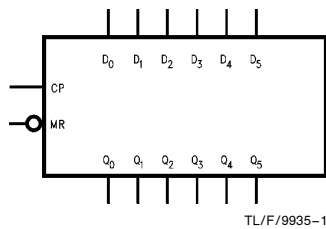
General Description

The 'AC/'ACT174 is a high-speed hex D flip-flop. The device is used primarily as a 6-bit edge-triggered storage register. The information on the D inputs is transferred to storage during the LOW-to-HIGH clock transition. The device has a Master Reset to simultaneously clear all flip-flops.

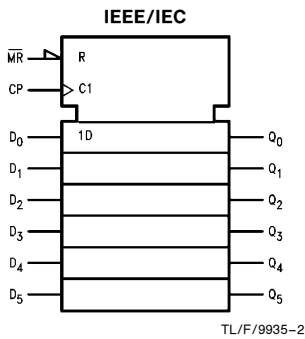
Features

- I_{CC} reduced by 50%
- Outputs source/sink 24 mA
- 'ACT174 has TTL-compatible inputs
- Standard Military Drawing (SMD)
 - 'AC174: 5962-87626
 - 'ACT174: 5962-87757

Logic Symbols

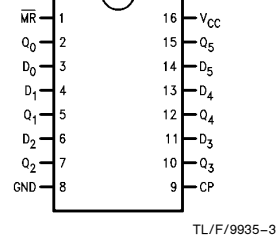


| Pin Names | Description |
|--------------------------------|--------------------|
| D ₀ -D ₅ | Data Inputs |
| CP | Clock Pulse Input |
| \overline{MR} | Master Reset Input |
| Q ₀ -Q ₅ | Outputs |

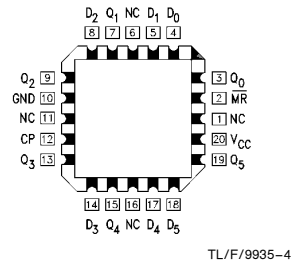


Connection Diagrams

Pin Assignment
for DIP, Flatpak and SOIC



Pin Assignment
for LCC



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Functional Description

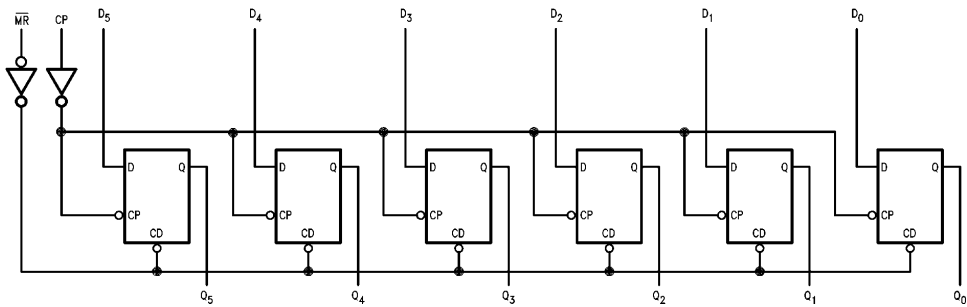
The 'AC/'ACT174 consists of six edge-triggered D flip-flops with individual D inputs and Q outputs. The Clock (CP) and Master Reset (\overline{MR}) are common to all flip-flops. Each D input's state is transferred to the corresponding flip-flop's output following the LOW-to-HIGH Clock (CP) transition. A LOW input to the Master Reset (\overline{MR}) will force all outputs LOW independent of Clock or Data inputs. The 'AC/'ACT174 is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

Truth Table

| Inputs | | | Output |
|-----------------|----|---|--------|
| \overline{MR} | CP | D | Q |
| L | X | X | L |
| H | ↗ | H | H |
| H | ↗ | L | L |
| H | L | X | Q |

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 ↗ = LOW-to-HIGH Transition

Logic Diagram



TL/F/9935-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|--|--------------------------|
| Supply Voltage (V_{CC}) | -0.5V to +7.0V |
| DC Input Diode Current (I_{IK}) | |
| $V_I = -0.5V$ | -20 mA |
| $V_I = V_{CC} + 0.5V$ | +20 mA |
| DC Input Voltage (V_I) | -0.5V to $V_{CC} + 0.5V$ |
| DC Output Diode Current (I_{OK}) | |
| $V_O = -0.5V$ | -20 mA |
| $V_O = V_{CC} + 0.5V$ | +20 mA |
| DC Output Voltage (V_O) | -0.5V to $V_{CC} + 0.5V$ |
| DC Output Source or Sink Current (I_O) | ±50 mA |
| DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND}) | ±50 mA |
| Storage Temperature (T_{STG}) | -65°C to +150°C |
| Junction Temperature (T_J) | |
| CDIP | 175°C |
| PDIP | 140°C |

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

| | |
|---|-----------------|
| Supply Voltage (V_{CC}) | |
| 'AC | 2.0V to 6.0V |
| 'ACT | 4.5V to 5.5V |
| Input Voltage (V_I) | 0V to V_{CC} |
| Output Voltage (V_O) | 0V to V_{CC} |
| Operating Temperature (T_A) | |
| 74AC/ACT | -40°C to +85°C |
| 54AC/ACT | -55°C to +125°C |
| Minimum Input Edge Rate ($\Delta V/\Delta t$) | |
| 'AC Devices | |
| V_{IN} from 30% to 70% of V_{CC} | |
| V_{CC} @ 3.3V, 4.5V, 5.5V | 125 mV/ns |
| Minimum Input Edge Rate ($\Delta V/\Delta t$) | |
| 'ACT Devices | |
| V_{IN} from 0.8V to 2.0V | |
| V_{CC} @ 4.5V, 5.5V | 125 mV/ns |

DC Characteristics for 'AC Family Devices

| Symbol | Parameter | V_{CC} (V) | 74AC | | 54AC | 74AC | | Units | Conditions |
|---|-----------------------------------|--------------|---------------------------|-------------------|--|---|------|---------------|--|
| | | | $T_A = +25^\circ\text{C}$ | | $T_A = -55^\circ\text{C to } +125^\circ\text{C}$ | $T_A = -40^\circ\text{C to } +85^\circ\text{C}$ | | | |
| | | | Typ | Guaranteed Limits | | | | | |
| V_{IH} | Minimum High Level Input Voltage | 3.0 | 1.5 | 2.1 | 2.1 | 2.1 | 2.1 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ |
| | | 4.5 | 2.25 | 3.15 | 3.15 | 3.15 | 3.15 | | |
| | | 5.5 | 2.75 | 3.85 | 3.85 | 3.85 | 3.85 | | |
| V_{IL} | Maximum Low Level Input Voltage | 3.0 | 1.5 | 0.9 | 0.9 | 0.9 | 0.9 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ |
| | | 4.5 | 2.25 | 1.35 | 1.35 | 1.35 | 1.35 | | |
| | | 5.5 | 2.75 | 1.65 | 1.65 | 1.65 | 1.65 | | |
| V_{OH} | Minimum High Level Output Voltage | 3.0 | 2.99 | 2.9 | 2.9 | 2.9 | 2.9 | V | $I_{OUT} = -50 \mu\text{A}$ |
| | | 4.5 | 4.49 | 4.4 | 4.4 | 4.4 | 4.4 | | |
| | | 5.5 | 5.49 | 5.4 | 5.4 | 5.4 | 5.4 | | |
| V_{OL} | Maximum Low Level Output Voltage | 3.0 | | 2.56 | 2.4 | 2.46 | 2.46 | V | * $V_{IN} = V_{IL}$ or V_{IH} -12 mA I_{OH} -24 mA -24 mA |
| | | 4.5 | 0.002 | 0.1 | 0.1 | 0.1 | 0.1 | | |
| | | 5.5 | 0.001 | 0.1 | 0.1 | 0.1 | 0.1 | | |
| V_{OL} | Maximum Low Level Output Voltage | 3.0 | | 0.36 | 0.50 | 0.44 | 0.44 | V | * $V_{IN} = V_{IL}$ or V_{IH} 12 mA I_{OL} 24 mA 24 mA |
| | | 4.5 | 0.002 | 0.1 | 0.1 | 0.1 | 0.1 | | |
| | | 5.5 | 0.001 | 0.1 | 0.1 | 0.1 | 0.1 | | |
| I_{IN} | Maximum Input Leakage Current | 3.0 | | 0.36 | 0.50 | 0.44 | 0.44 | μA | $V_I = V_{CC}, \text{GND}$ |
| | | 4.5 | | 0.36 | 0.50 | 0.44 | 0.44 | | |
| | | 5.5 | | 0.36 | 0.50 | 0.44 | 0.44 | | |
| *All outputs loaded; thresholds on input associated with output under test. | | | | | | | | | |

DC Characteristics for 'AC Family Devices (Continued)

| Symbol | Parameter | V _{CC} (V) | 74AC | | 54AC | 74AC | Units | Conditions |
|------------------|----------------------------------|------------------------|------------------------|-------------------|-------------------------------------|------------------------------------|-------|---|
| | | | T _A = +25°C | | T _A = –55°C to +125°C | T _A = –40°C to +85°C | | |
| | | | Typ | Guaranteed Limits | | | | |
| I _{OLD} | †Minimum Dynamic Output Current | 5.5 | | | 50 | 75 | mA | V _{OLD} = 1.65V Max |
| I _{OHD} | | 5.5 | | | –50 | –75 | mA | V _{OHD} = 3.85V Min |
| I _{CC} | Maximum Quiescent Supply Current | 5.5 | | 4.0 | 80.0 | 40.0 | μA | V _{IN} = V _{CC} or GND |

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.
I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

| Symbol | Parameter | V _{CC} (V) | 74ACT | | 54ACT | 74ACT | Units | Conditions |
|-------------------|-----------------------------------|------------------------|------------------------|-------------------|-------------------------------------|------------------------------------|-------|---|
| | | | T _A = +25°C | | T _A = –55°C to +125°C | T _A = –40°C to +85°C | | |
| | | | Typ | Guaranteed Limits | | | | |
| V _{IH} | Minimum High Level Input Voltage | 4.5 | 1.5 | 2.0 | 2.0 | 2.0 | V | V _{OUT} = 0.1V or V _{CC} – 0.1V |
| | | 5.5 | 1.5 | 2.0 | 2.0 | 2.0 | | |
| V _{IL} | Maximum Low Level Input Voltage | 4.5 | 1.5 | 0.8 | 0.8 | 0.8 | V | V _{OUT} = 0.1V or V _{CC} – 0.1V |
| | | 5.5 | 1.5 | 0.8 | 0.8 | 0.8 | | |
| V _{OH} | Minimum High Level Output Voltage | 4.5 | 4.49 | 4.4 | 4.4 | 4.4 | V | I _{OUT} = –50 μA |
| | | 5.5 | 5.49 | 5.4 | 5.4 | 5.4 | | |
| | | 4.5 | | 3.86 | 3.70 | 3.76 | V | *V _{IN} = V _{IL} or V _{IH} –24 mA I _{OH} –24 mA |
| | | 5.5 | | 4.86 | 4.70 | 4.76 | | |
| V _{OL} | Maximum Low Level Output Voltage | 4.5 | 0.001 | 0.1 | 0.1 | 0.1 | V | I _{OUT} = 50 μA |
| | | 5.5 | 0.001 | 0.1 | 0.1 | 0.1 | | |
| | | 4.5 | | 0.36 | 0.50 | 0.44 | V | *V _{IN} = V _{IL} or V _{IH} 24 mA I _{OL} 24 mA |
| | | 5.5 | | 0.36 | 0.50 | 0.44 | | |
| I _{IN} | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 | ±1.0 | μA | V _I = V _{CC} , GND |
| I _{CC} T | Maximum I _{CC} /Input | 5.5 | 0.6 | | 1.6 | 1.5 | mA | V _I = V _{CC} – 2.1V |
| I _{OLD} | †Minimum Dynamic Output Current | 5.5 | | | 50 | 75 | mA | V _{OLD} = 1.65V Max |
| I _{OHD} | | 5.5 | | | –50 | –75 | mA | V _{OHD} = 3.85V Min |
| I _{CC} | Maximum Quiescent Supply Current | 5.5 | | 4.0 | 80.0 | 40.0 | μA | V _{IN} = V _{CC} or GND |

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics

| Symbol | Parameter | V _{CC} * (V) | 74AC | | | 54AC | | 74AC | | Units |
|------------------|--|--------------------------|--|------------|-------------|---|--------------|--|--------------|-------|
| | | | T _A = +25°C C _L = 50 pF | | | T _A = -55°C to +125°C C _L = 50 pF | | T _A = -40°C to +85°C C _L = 50 pF | | |
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| f _{max} | Maximum Clock Frequency | 3.3 5.0 | 90 100 | 100 125 | | 65 90 | | 70 100 | MHz | |
| t _{PLH} | Propagation Delay CP to Q _n | 3.3 5.0 | 2.0 1.5 | 9.0 6.0 | 11.5 8.5 | 1.0 1.5 | 14.0 10.5 | 1.5 1.0 | 12.5 9.5 | ns |
| t _{PHL} | Propagation Delay CP to Q _n | 3.3 5.0 | 2.0 1.5 | 8.5 6.0 | 11.0 8.0 | 1.0 1.5 | 13.0 10.0 | 1.5 1.0 | 12.0 9.0 | ns |
| t _{PHL} | Propagation Delay \overline{MR} to Q _n | 3.3 5.0 | 2.5 1.5 | 9.0 7.0 | 11.5 9.0 | 1.0 1.5 | 13.5 11.0 | 2.0 1.5 | 12.5 10.5 | ns |

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

| Symbol | Parameter | V _{CC} * (V) | 74AC | | 54AC | | 74AC | | Units |
|------------------|---|--------------------------|--|--------------------|---|------------|--|----|-------|
| | | | T _A = +25°C C _L = 50 pF | | T _A = -55°C to +125°C C _L = 50 pF | | T _A = -40°C to +85°C C _L = 50 pF | | |
| | | | Typ | Guaranteed Minimum | | | | | |
| t _s | Setup Time, HIGH or LOW D _n to CP | 3.3 5.0 | 2.5 2.0 | 6.5 5.0 | 7.5 5.5 | 7.0 5.5 | 7.0 5.5 | ns | |
| t _h | Hold Time, HIGH or LOW D _n to CP | 3.3 5.0 | 1.0 0.5 | 3.0 3.0 | 3.0 3.0 | 3.0 3.0 | 3.0 3.0 | ns | |
| t _w | \overline{MR} Pulse Width, LOW | 3.3 5.0 | 1.0 1.0 | 5.5 5.0 | 7.0 5.0 | 7.0 5.0 | 7.0 5.0 | ns | |
| t _w | CP Pulse Width | 3.3 5.0 | 1.0 1.0 | 5.5 5.0 | 7.0 5.0 | 7.0 5.0 | 7.0 5.0 | ns | |
| t _{rec} | Recovery Time \overline{MR} to CP | 3.3 5.0 | 0 0 | 2.5 2.0 | 3.0 2.0 | 2.5 2.0 | 2.5 2.0 | ns | |

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics

| Symbol | Parameter | V _{CC} * (V) | 74ACT | | | 54ACT | | 74ACT | | Units |
|------------------|--|--------------------------|--|-----|------|---|------|--|------|-------|
| | | | T _A = +25°C C _L = 50 pF | | | T _A = -55°C to +125°C C _L = 50 pF | | T _A = -40°C to +85°C C _L = 50 pF | | |
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| f _{max} | Maximum Clock Frequency | 5.0 | 165 | 200 | | 95 | | 140 | MHz | |
| t _{PLH} | Propagation Delay CP to Q _n | 5.0 | 1.5 | 7.0 | 10.5 | 1.5 | 12.5 | 1.5 | 11.5 | ns |
| t _{PHL} | Propagation Delay CP to Q _n | 5.0 | 1.5 | 7.0 | 10.5 | 1.5 | 13.0 | 1.5 | 11.5 | ns |
| t _{PHL} | Propagation Delay \overline{MR} to Q _n | 5.0 | 1.5 | 6.5 | 9.5 | 1.5 | 12.0 | 1.5 | 11.0 | ns |

*Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

| Symbol | Parameter | V _{CC} * (V) | 74ACT | 54ACT | 74ACT | Units | |
|------------------|---|--------------------------|--|---|--|-------|----|
| | | | T _A = +25°C C _L = 50 pF | T _A = -55°C to +125°C C _L = 50 pF | T _A = -40°C to +85°C C _L = 50 pF | | |
| | | | Typ | Guaranteed Minimum | | | |
| t _s | Setup Time, HIGH or LOW D _n to CP | 5.0 | 0.5 | 1.5 | 3.0 | 1.5 | ns |
| t _h | Hold Time, HIGH or LOW D _n to CP | 5.0 | 1.0 | 2.0 | 2.0 | 2.0 | ns |
| t _w | \overline{MR} Pulse Width, LOW | 5.0 | 1.5 | 3.0 | 5.0 | 3.5 | ns |
| t _w | CP Pulse Width, HIGH OR LOW | 5.0 | 1.5 | 3.0 | 5.0 | 3.5 | ns |
| t _{rec} | Recovery Time \overline{MR} to CP | 5.0 | -1.0 | 0.5 | 1.0 | 0.5 | ns |

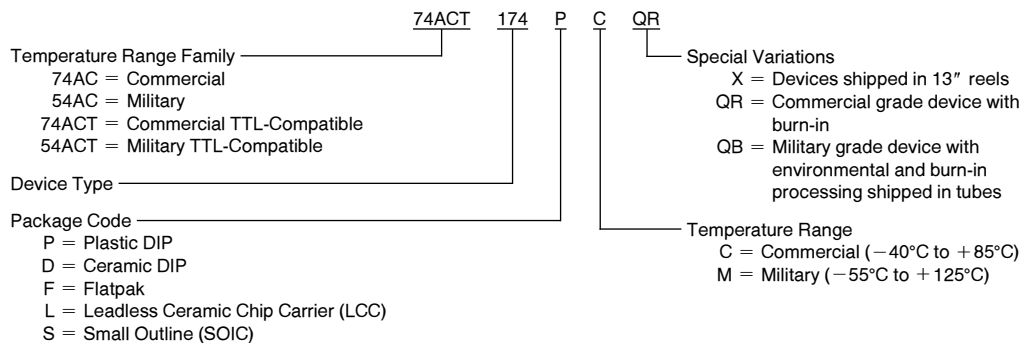
*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

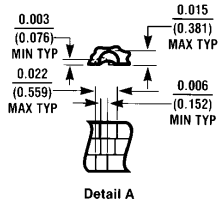
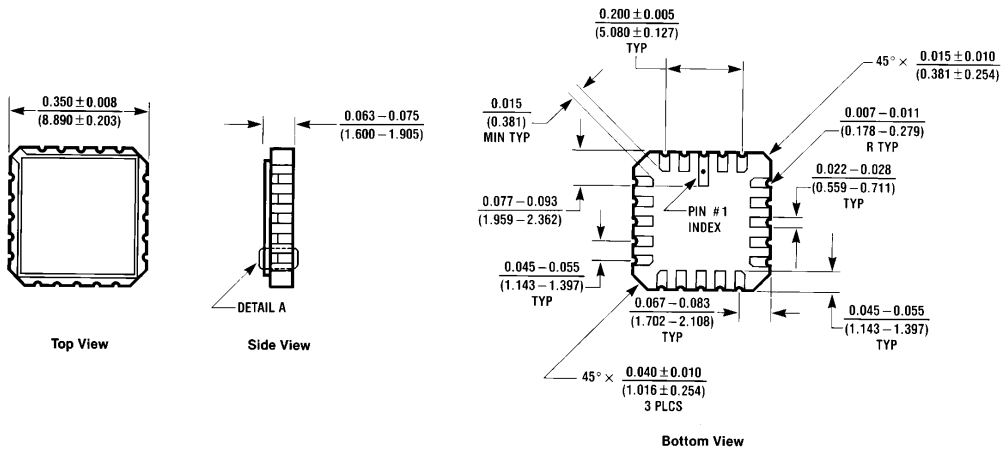
| Symbol | Parameter | Typ | Units | Conditions |
|-----------------|----------------------------------|------|-------|------------------------|
| C _{IN} | Input Capacitance | 4.5 | pF | V _{CC} = OPEN |
| C _{PD} | Power Dissipation Capacitance | 85.0 | pF | V _{CC} = 5.0V |

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

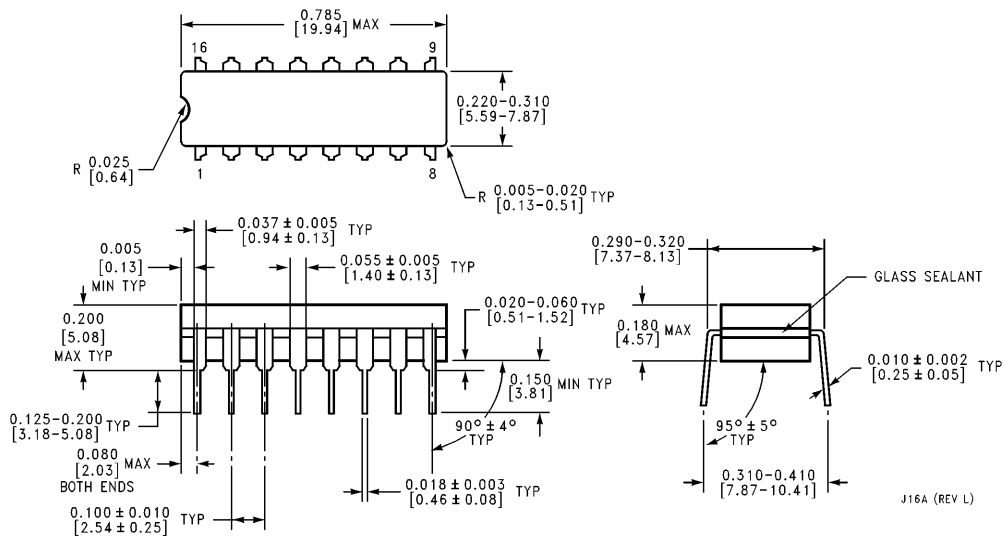


Physical Dimensions inches (millimeters)



**20-Terminal Ceramic Leadless Chip Carrier (L)
 NS Package Number E20A**

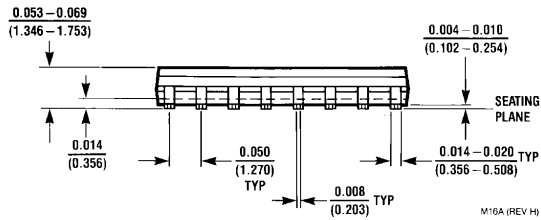
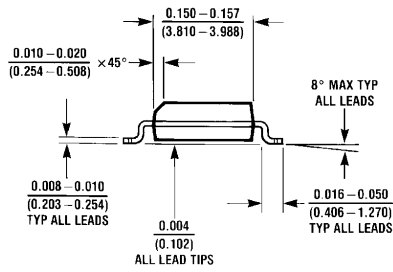
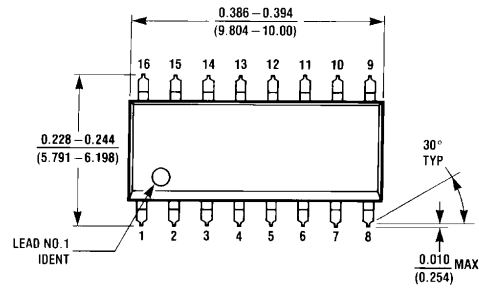
E20A (REV D)



**16-Lead Ceramic Dual-In-Line Package (D)
 NS Package Number J16A**

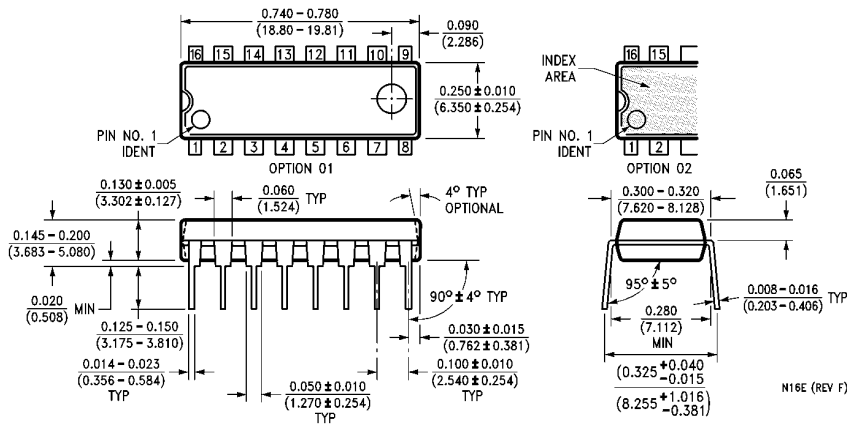
J16A (REV L)

Physical Dimensions inches (millimeters) (Continued)



M16A (REV H)

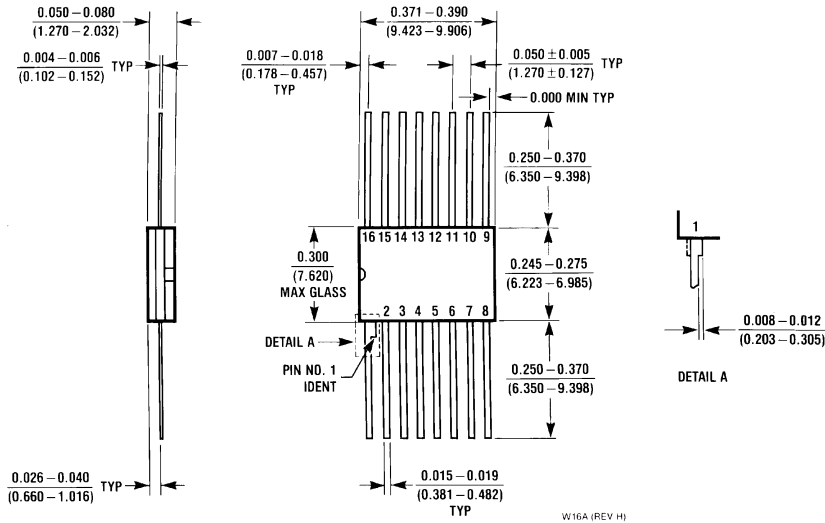
**16-Lead Small Outline Integrated Circuit (S)
NS Package Number M16A**



N16E (REV F)

**16-Lead Plastic Dual-In-Line Package (P)
NS Package Number N16E**

Physical Dimensions inches (millimeters) (Continued)



**16-Lead Ceramic Flatpak (F)
NS Package Number W16A**

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



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