

# 74HC4851

## 8-channel analog multiplexer/demultiplexer with injection-current effect control

Rev. 01 — 9 March 2007

Product data sheet

### 1. General description

---

The 74HC4851 is a high-speed Si-gate CMOS device and is specified in compliance with JEDEC standard no. 7A.

The 74HC4851 is an 8-channel analog multiplexer/demultiplexer with three digital select inputs (S0 to S2), an active-LOW enable input ( $\bar{E}$ ), eight independent inputs/outputs (Y0 to Y7) and a common input/output (Z). The device features injection-current effect control, which has excellent value in automotive applications where voltages in excess of the supply voltage are common.

With  $\bar{E}$  LOW, one of the eight switches is selected (low impedance ON-state) by S0 to S2. With  $\bar{E}$  HIGH, all switches are in the high-impedance OFF-state, independent of S0 to S2.

The injection-current effect control allows signals at disabled analog input channels to exceed the supply voltage without affecting the signal of the enabled analog channel. This eliminates the need for external diode/resistor networks typically used to keep the analog channel signals within the supply-voltage range.

### 2. Features

---

- Injection-current cross coupling < 1 mV/mA
- Wide supply voltage range from 2.0 V to 6.0 V
- ESD protection:
  - ◆ HBM JESD22-A114D Class 2. Exceeds 2000 V
  - ◆ MM JESD22-A115-A exceeds 200 V
  - ◆ CDM JESD22-C101C exceeds 1000 V
- Latch-up performance exceeds 100 mA per JESD 78 Class II
- Low ON-state resistance:
  - ◆ 400  $\Omega$  (typical) at  $V_{CC} = 2.0$  V
  - ◆ 215  $\Omega$  (typical) at  $V_{CC} = 3.0$  V
  - ◆ 120  $\Omega$  (typical) at  $V_{CC} = 3.3$  V
  - ◆ 76  $\Omega$  (typical) at  $V_{CC} = 4.5$  V
  - ◆ 59  $\Omega$  (typical) at  $V_{CC} = 6.0$  V

### 3. Applications

- Analog multiplexing and demultiplexing
- Digital multiplexing and demultiplexing
- Signal gating
- Automotive application

### 4. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74HC4851D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HC4851PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74HC4851BQ	-40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1

### 5. Functional diagram

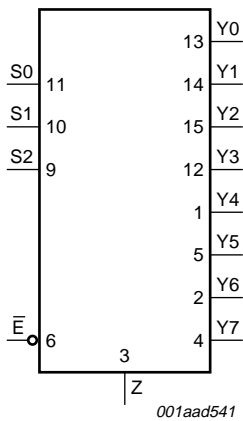


Fig 1. Logic symbol

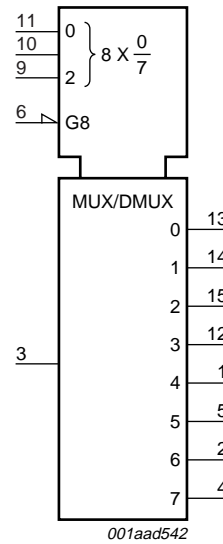


Fig 2. IEC logic symbol

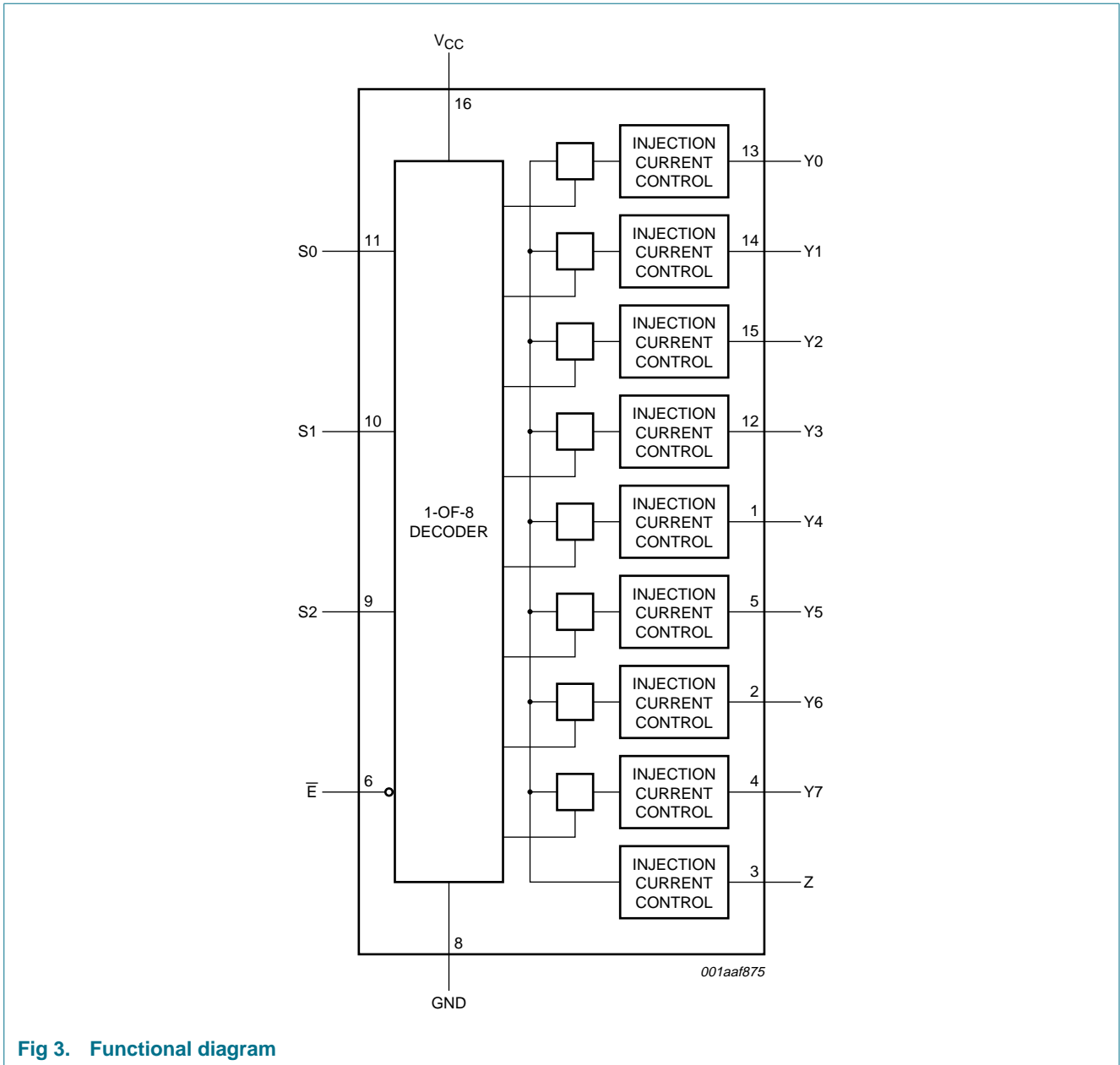
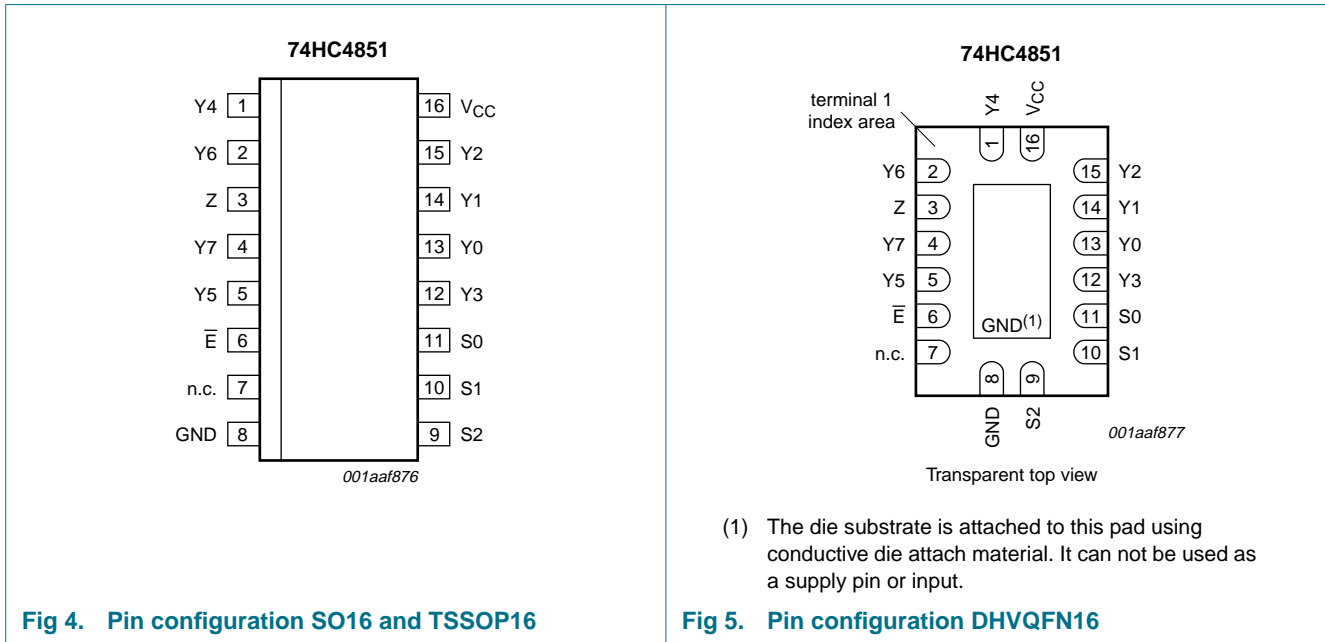


Fig 3. Functional diagram

## 6. Pinning information

### 6.1 Pinning



### 6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
Y4	1	independent input/output Y4
Y6	2	independent input/output Y6
Z	3	common input/output Z
Y7	4	independent input/output Y7
Y5	5	independent input/output Y5
$\bar{E}$	6	enable input (active LOW)
n.c.	7	not connected
GND	8	ground (0 V)
S2	9	select input S2
S1	10	select input S1
S0	11	select input S0
Y3	12	independent input/output Y3
Y0	13	independent input/output Y0
Y1	14	independent input/output Y1
Y2	15	independent input/output Y2
V <sub>CC</sub>	16	positive supply voltage

## 7. Functional description

Table 3. Function table<sup>[1]</sup>

Input				Channel ON
$\bar{E}$	S2	S1	S0	
L	L	L	L	Y0 to Z
L	L	L	H	Y1 to Z
L	L	H	L	Y2 to Z
L	L	H	H	Y3 to Z
L	H	L	L	Y4 to Z
L	H	L	H	Y5 to Z
L	H	H	L	Y6 to Z
L	H	H	H	Y7 to Z
H	X	X	X	-

- [1] H = HIGH voltage level;  
L = LOW voltage level;  
X = don't care.

## 8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7.0	V
$V_I$	input voltage		-0.5	$V_{CC} + 0.5$	V
$V_{SW}$	switch voltage	enable and disable mode	-0.5	$V_{CC} + 0.5$	V
$I_{IK}$	input clamping current	$V_I < 0\text{ V}$ or $V_I > V_{CC}$	-	$\pm 20$	mA
$I_{SK}$	switch clamping current	$V_I < 0\text{ V}$ or $V_I > V_{CC}$	-	$\pm 20$	mA
$I_{SW}$	switch current	$V_{SW} = 0\text{ V}$ to $V_{CC}$	-	$\pm 25$	mA
$I_{CC}$	supply current		-	50	mA
$I_{GND}$	ground current		-50	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40\text{ °C}$ to $+125\text{ °C}$	<sup>[1]</sup> -	500	mW

- [1] For SO16 package:  $P_{tot}$  derates linearly with 8 mW/K above 70 °C.  
For TSSOP16 package:  $P_{tot}$  derates linearly with 5.5 mW/K above 60 °C.  
For DHVQFN16 packages:  $P_{tot}$  derates linearly with 4.5 mW/K above 60 °C.

## 9. Recommended operating conditions

**Table 5.** Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC}$	supply voltage		2.0	-	6.0	V
$V_I$	input voltage		0	-	$V_{CC}$	V
$V_{SW}$	switch voltage		0	-	$V_{CC}$	V
$T_{amb}$	ambient temperature		-40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.0\text{ V}$	-	6.0	1000	ns/V
		$V_{CC} = 3.0\text{ V}$	-	6.0	800	ns/V
		$V_{CC} = 3.3\text{ V}$	-	6.0	800	ns/V
		$V_{CC} = 4.5\text{ V}$	-	6.0	500	ns/V
		$V_{CC} = 6.0\text{ V}$	-	6.0	400	ns/V

## 10. Static characteristics

**Table 6.**  $R_{ON}$  resistance  
For test circuit see [Figure 8](#).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b><math>T_{amb} = 25\text{ °C}</math></b>						
$R_{ON(peak)}$	ON resistance (peak)	$V_I = V_{CC}$ to GND; $\bar{E} = V_{IL}$				
		$V_{CC} = 2.0\text{ V}; I_{SW} = 2\text{ mA}$	-	400	650	$\Omega$
		$V_{CC} = 3.0\text{ V}; I_{SW} \leq 2\text{ mA}$	-	215	330	$\Omega$
		$V_{CC} = 3.3\text{ V}; I_{SW} \leq 2\text{ mA}$	-	120	270	$\Omega$
		$V_{CC} = 4.5\text{ V}; I_{SW} \leq 2\text{ mA}$	-	76	210	$\Omega$
		$V_{CC} = 6.0\text{ V}; I_{SW} \leq 2\text{ mA}$	-	59	195	$\Omega$
$\Delta R_{ON}$	ON resistance mismatch between channels	$V_I = 0.5 \times V_{CC}; \bar{E} = V_{IL}$				
		$V_{CC} = 2.0\text{ V}; I_{SW} = 2\text{ mA}$	-	4	10	$\Omega$
		$V_{CC} = 3.0\text{ V}; I_{SW} \leq 2\text{ mA}$	-	2	8	$\Omega$
		$V_{CC} = 3.3\text{ V}; I_{SW} \leq 2\text{ mA}$	-	2	8	$\Omega$
		$V_{CC} = 4.5\text{ V}; I_{SW} \leq 2\text{ mA}$	-	2	8	$\Omega$
		$V_{CC} = 6.0\text{ V}; I_{SW} \leq 2\text{ mA}$	-	3	9	$\Omega$
<b><math>T_{amb} = -40\text{ °C to }+85\text{ °C}</math></b>						
$R_{ON(peak)}$	ON resistance (peak)	$V_I = V_{CC}$ to GND; $\bar{E} = V_{IL}$				
		$V_{CC} = 2.0\text{ V}; I_{SW} = 2\text{ mA}$	-	-	670	$\Omega$
		$V_{CC} = 3.0\text{ V}; I_{SW} \leq 2\text{ mA}$	-	-	360	$\Omega$
		$V_{CC} = 3.3\text{ V}; I_{SW} \leq 2\text{ mA}$	-	-	305	$\Omega$
		$V_{CC} = 4.5\text{ V}; I_{SW} \leq 2\text{ mA}$	-	-	240	$\Omega$
		$V_{CC} = 6.0\text{ V}; I_{SW} \leq 2\text{ mA}$	-	-	220	$\Omega$

**Table 6.**  $R_{ON}$  resistance ...continued  
For test circuit see [Figure 8](#).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$\Delta R_{ON}$	ON resistance mismatch between channels	$V_I = 0.5 \times V_{CC}; \bar{E} = V_{IL}$				
		$V_{CC} = 2.0 \text{ V}; I_{SW} = 2 \text{ mA}$	-	-	15	$\Omega$
		$V_{CC} = 3.0 \text{ V}; I_{SW} \leq 2 \text{ mA}$	-	-	12	$\Omega$
		$V_{CC} = 3.3 \text{ V}; I_{SW} \leq 2 \text{ mA}$	-	-	12	$\Omega$
		$V_{CC} = 4.5 \text{ V}; I_{SW} \leq 2 \text{ mA}$	-	-	12	$\Omega$
		$V_{CC} = 6.0 \text{ V}; I_{SW} \leq 2 \text{ mA}$	-	-	13	$\Omega$
<b><math>T_{amb} = -40 \text{ }^\circ\text{C to } +125 \text{ }^\circ\text{C}</math></b>						
$R_{ON(peak)}$	ON resistance (peak)	$V_I = V_{CC} \text{ to GND}; \bar{E} = V_{IL}$				
		$V_{CC} = 2.0 \text{ V}; I_{SW} = 2 \text{ mA}$	-	-	700	$\Omega$
		$V_{CC} = 3.0 \text{ V}; I_{SW} \leq 2 \text{ mA}$	-	-	380	$\Omega$
		$V_{CC} = 3.3 \text{ V}; I_{SW} \leq 2 \text{ mA}$	-	-	345	$\Omega$
		$V_{CC} = 4.5 \text{ V}; I_{SW} \leq 2 \text{ mA}$	-	-	270	$\Omega$
		$V_{CC} = 6.0 \text{ V}; I_{SW} \leq 2 \text{ mA}$	-	-	250	$\Omega$
$\Delta R_{ON}$	ON resistance mismatch between channels	$V_I = 0.5 \times V_{CC}; \bar{E} = V_{IL}$				
		$V_{CC} = 2.0 \text{ V}; I_{SW} = 2 \text{ mA}$	-	-	20	$\Omega$
		$V_{CC} = 3.0 \text{ V}; I_{SW} \leq 2 \text{ mA}$	-	-	16	$\Omega$
		$V_{CC} = 3.3 \text{ V}; I_{SW} \leq 2 \text{ mA}$	-	-	16	$\Omega$
		$V_{CC} = 4.5 \text{ V}; I_{SW} \leq 2 \text{ mA}$	-	-	16	$\Omega$
		$V_{CC} = 6.0 \text{ V}; I_{SW} \leq 2 \text{ mA}$	-	-	18	$\Omega$

**Table 7.** Injection current coupling  
For test circuit see [Figure 9](#).

Symbol	Parameter	Conditions	Min	Typ <sup>[1]</sup>	Max	Unit	
<b><math>T_{amb} = -40 \text{ }^\circ\text{C to } +125 \text{ }^\circ\text{C}</math></b>							
$\Delta V_O$	output voltage variation	$ I_{SW}  \leq 1 \text{ mA}; R_S \leq 3.9 \text{ k}\Omega$					
		$V_{CC} = 3.3 \text{ V}$	-	0.05	1	mV	
		$V_{CC} = 5.0 \text{ V}$	-	0.03	1	mV	
		$ I_{SW}  \leq 10 \text{ mA}; R_S \leq 3.9 \text{ k}\Omega$					
		$V_{CC} = 3.3 \text{ V}$	-	0.55	5	mV	
		$V_{CC} = 5.0 \text{ V}$	-	0.27	5	mV	
		$ I_{SW}  \leq 1 \text{ mA}; R_S \leq 20 \text{ k}\Omega$					
		$V_{CC} = 3.3 \text{ V}$	-	0.04	2	mV	
		$V_{CC} = 5.0 \text{ V}$	-	0.03	2	mV	
		$ I_{SW}  \leq 10 \text{ mA}; R_S \leq 20 \text{ k}\Omega$					
		$V_{CC} = 3.3 \text{ V}$	-	0.56	20	mV	
		$V_{CC} = 5.0 \text{ V}$	-	0.48	20	mV	

[1] Typical values are measured at  $T_{amb} = 25 \text{ }^\circ\text{C}$ .

[2]  $\Delta V_O$  here is the maximum variation of output voltage of an enabled analog channel when current is injected into any disabled channel.

[3]  $I_{SW}$  = total current injected into all disabled channels.

**Table 8. Static characteristics**

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b><math>T_{amb} = 25\text{ }^{\circ}\text{C}</math></b>						
$V_{IH}$	HIGH-level input voltage	control inputs				
		$V_{CC} = 2.0\text{ V}$	1.5	-	-	V
		$V_{CC} = 3.0\text{ V}$	2.1	-	-	V
		$V_{CC} = 3.3\text{ V}$	2.3	-	-	V
		$V_{CC} = 4.5\text{ V}$	3.15	-	-	V
		$V_{CC} = 6.0\text{ V}$	4.2	-	-	V
$V_{IL}$	LOW-level input voltage	control inputs				
		$V_{CC} = 2.0\text{ V}$	-	-	0.5	V
		$V_{CC} = 3.0\text{ V}$	-	-	0.9	V
		$V_{CC} = 3.3\text{ V}$	-	-	1.0	V
		$V_{CC} = 4.5\text{ V}$	-	-	1.35	V
		$V_{CC} = 6.0\text{ V}$	-	-	1.8	V
$I_I$	input leakage current	control inputs; $V_I = \text{GND or } V_{CC}$				
		$V_{CC} = 6.0\text{ V}$	-	-	$\pm 0.1$	$\mu\text{A}$
$I_{S(OFF)}$	OFF-state leakage current	$\bar{E} = V_{IH}; V_I = \text{GND or } V_{CC};$ $V_O = V_{CC} \text{ or } \text{GND}; V_{CC} = 6.0\text{ V};$ see <a href="#">Figure 6</a>				
		per channel	-	-	$\pm 0.1$	$\mu\text{A}$
		all channels	-	-	$\pm 0.2$	$\mu\text{A}$
$I_{S(ON)}$	ON-state leakage current	$\bar{E} = V_{IL}; V_I = \text{GND or } V_{CC};$ $V_O = V_{CC} \text{ or } \text{GND}; V_{CC} = 6.0\text{ V};$ see <a href="#">Figure 7</a>	-	-	$\pm 0.1$	$\mu\text{A}$
$I_{CC}$	supply current	$V_I = \text{GND or } V_{CC}$				
		$V_{CC} = 6.0\text{ V}$	-	-	2.0	$\mu\text{A}$
$C_I$	input capacitance	S0, S1, S2 and $\bar{E}$	-	2	10	pF
$C_{sw}$	switch capacitance	Z; OFF-state	-	15	40	pF
		Yn; OFF-state	-	3	15	pF
<b><math>T_{amb} = -40\text{ }^{\circ}\text{C to } +85\text{ }^{\circ}\text{C}</math></b>						
$V_{IH}$	HIGH-level input voltage	control inputs				
		$V_{CC} = 2.0\text{ V}$	1.5	-	-	V
		$V_{CC} = 3.0\text{ V}$	2.1	-	-	V
		$V_{CC} = 3.3\text{ V}$	2.3	-	-	V
		$V_{CC} = 4.5\text{ V}$	3.15	-	-	V
		$V_{CC} = 6.0\text{ V}$	4.2	-	-	V
$V_{IL}$	LOW-level input voltage	control inputs				
		$V_{CC} = 2.0\text{ V}$	-	-	0.5	V
		$V_{CC} = 3.0\text{ V}$	-	-	0.9	V
		$V_{CC} = 3.3\text{ V}$	-	-	1.0	V
		$V_{CC} = 4.5\text{ V}$	-	-	1.35	V
		$V_{CC} = 6.0\text{ V}$	-	-	1.8	V

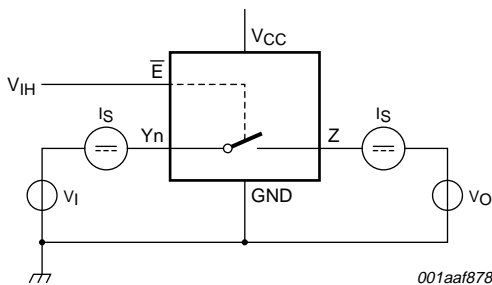


**Table 8. Static characteristics ...continued**  
 Voltages are referenced to GND (ground = 0 V).

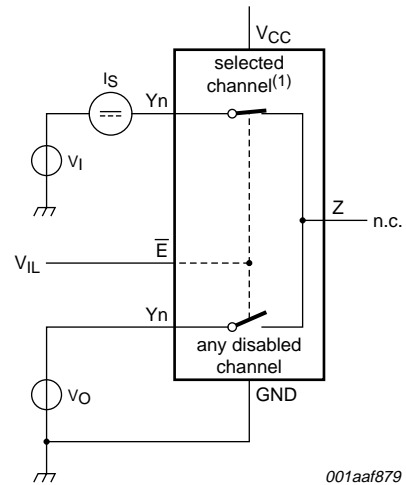
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_I$	input leakage current	control inputs; $V_I = \text{GND or } V_{CC}$ $V_{CC} = 6.0 \text{ V}$	-	-	$\pm 0.1$	$\mu\text{A}$
$I_{S(\text{OFF})}$	OFF-state leakage current	$\bar{E} = V_{IH}$ ; $V_I = \text{GND or } V_{CC}$ ; $V_O = V_{CC}$ or GND; $V_{CC} = 6.0 \text{ V}$ ; see <a href="#">Figure 6</a>				
		per channel	-	-	$\pm 0.5$	$\mu\text{A}$
		all channels	-	-	$\pm 2.0$	$\mu\text{A}$
$I_{S(\text{ON})}$	ON-state leakage current	$\bar{E} = V_{IL}$ ; $V_I = \text{GND or } V_{CC}$ ; $V_O = V_{CC}$ or GND; $V_{CC} = 6.0 \text{ V}$ ; see <a href="#">Figure 7</a>	-	-	$\pm 2.0$	$\mu\text{A}$
$I_{CC}$	supply current	$V_I = \text{GND or } V_{CC}$ $V_{CC} = 6.0 \text{ V}$	-	-	5.0	$\mu\text{A}$
$C_I$	input capacitance	S0, S1, S2 and $\bar{E}$	-	-	10	pF
$C_{sw}$	switch capacitance	Z; OFF-state	-	-	40	pF
		Yn; OFF-state	-	-	15	pF
<b><math>T_{\text{amb}} = -40 \text{ }^\circ\text{C to } +125 \text{ }^\circ\text{C}</math></b>						
$V_{IH}$	HIGH-level input voltage	control inputs				
		$V_{CC} = 2.0 \text{ V}$	1.5	-	-	V
		$V_{CC} = 3.0 \text{ V}$	2.1	-	-	V
		$V_{CC} = 3.3 \text{ V}$	2.3	-	-	V
		$V_{CC} = 4.5 \text{ V}$	3.15	-	-	V
		$V_{CC} = 6.0 \text{ V}$	4.2	-	-	V
$V_{IL}$	LOW-level input voltage	control inputs				
		$V_{CC} = 2.0 \text{ V}$	-	-	0.5	V
		$V_{CC} = 3.0 \text{ V}$	-	-	0.9	V
		$V_{CC} = 3.3 \text{ V}$	-	-	1.0	V
		$V_{CC} = 4.5 \text{ V}$	-	-	1.35	V
		$V_{CC} = 6.0 \text{ V}$	-	-	1.8	V
$I_I$	input leakage current	control inputs; $V_I = \text{GND or } V_{CC}$ $V_{CC} = 6.0 \text{ V}$	-	-	$\pm 1.0$	$\mu\text{A}$
$I_{S(\text{OFF})}$	OFF-state leakage current	$\bar{E} = V_{IH}$ ; $V_I = \text{GND or } V_{CC}$ ; $V_O = V_{CC}$ or GND; $V_{CC} = 6.0 \text{ V}$ ; see <a href="#">Figure 6</a>				
		per channel	-	-	$\pm 2.0$	$\mu\text{A}$
		all channels	-	-	$\pm 10.0$	$\mu\text{A}$
$I_{S(\text{ON})}$	ON-state leakage current	$\bar{E} = V_{IL}$ ; $V_I = \text{GND or } V_{CC}$ ; $V_O = V_{CC}$ or GND; $V_{CC} = 6.0 \text{ V}$ ; see <a href="#">Figure 7</a>	-	-	$\pm 10.0$	$\mu\text{A}$
$I_{CC}$	supply current	$V_I = \text{GND or } V_{CC}$ $V_{CC} = 6.0 \text{ V}$	-	-	20.0	$\mu\text{A}$

**Table 8. Static characteristics ...continued**  
 Voltages are referenced to GND (ground = 0 V).

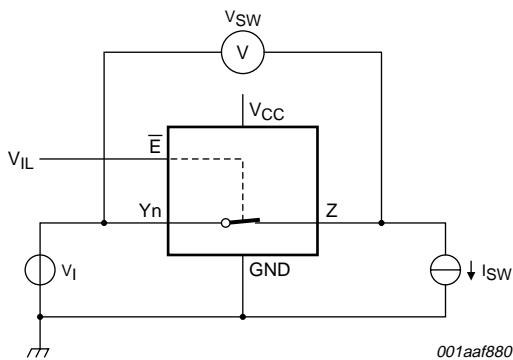
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$C_I$	input capacitance	S0, S1, S2 and $\bar{E}$	-	-	10	pF
$C_{SW}$	switch capacitance	Z; OFF-state	-	-	40	pF
		Yn; OFF-state	-	-	15	pF



**Fig 6. Test circuit for measuring OFF-state leakage current**

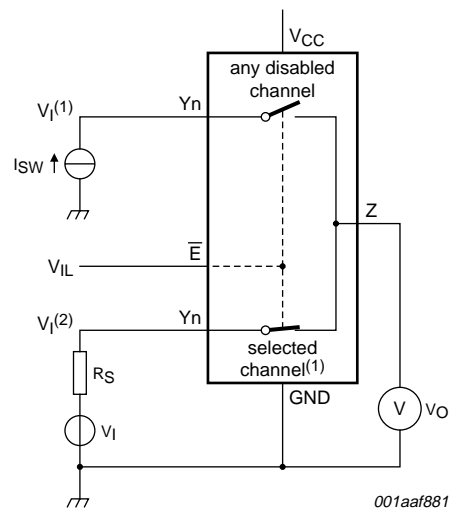


(1) Channel is selected by S0, S1 and S2.  
**Fig 7. Test circuit for measuring ON-state leakage current**



$$R_{ON} = V_{SW} / I_{SW}$$

**Fig 8. Test circuit for measuring ON resistance**



(1) Channel is selected by S0, S1 and S2.  
 $V_I(1) < GND$  or  $V_I(1) > V_{CC}$ .  
 $GND < V_I(2) < V_{CC}$ .

**Fig 9. Test circuit for injection current coupling**

## 11. Dynamic characteristics

**Table 9. Dynamic characteristics**

$GND = 0\text{ V}$ ;  $C_L = 50\text{ pF}$ ;  $R_L = 10\text{ K}\Omega$  unless specified otherwise; for test circuit see [Figure 12](#).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b><math>V_{CC} = 2.0\text{ V}</math></b>										
$t_{pd}$	propagation delay	see <a href="#">Figure 10</a>	<a href="#">[1]</a>							
		Z, Yn to Yn, Z	-	10.0	25	-	29	-	32	ns
		Sn to Z, Yn	-	18.0	32	-	35	-	40	ns
$t_{en}$	enable time	see <a href="#">Figure 11</a>	<a href="#">[2]</a>							
		$\bar{E}$ to Z, Yn	-	-	95	-	105	-	115	ns
$t_{dis}$	disable time	see <a href="#">Figure 11</a>	<a href="#">[3]</a>							
		$\bar{E}$ to Z, Yn	-	-	95	-	105	-	115	ns
<b><math>V_{CC} = 3.0\text{ V}</math></b>										
$t_{pd}$	propagation delay	see <a href="#">Figure 10</a>	<a href="#">[1]</a>							
		Z, Yn to Yn, Z	-	6.0	15.5	-	17.5	-	19.5	ns
		Sn to Z, Yn	-	9.5	17.5	-	20	-	23	ns
$t_{en}$	enable time	see <a href="#">Figure 11</a>	<a href="#">[2]</a>							
		$\bar{E}$ to Z, Yn	-	-	90	-	100	-	110	ns
$t_{dis}$	disable time	see <a href="#">Figure 11</a>	<a href="#">[3]</a>							
		$\bar{E}$ to Z, Yn	-	-	90	-	100	-	110	ns
<b><math>V_{CC} = 3.3\text{ V}</math></b>										
$t_{pd}$	propagation delay	see <a href="#">Figure 10</a>	<a href="#">[1]</a>							
		Z, Yn to Yn, Z	-	5.0	14.5	-	16.5	-	18.5	ns
		Sn to Z, Yn	-	8.5	16.5	-	19	-	22	ns
$t_{en}$	enable time	see <a href="#">Figure 11</a>	<a href="#">[2]</a>							
		$\bar{E}$ to Z, Yn	-	-	85	-	95	-	105	ns
$t_{dis}$	disable time	see <a href="#">Figure 11</a>	<a href="#">[3]</a>							
		$\bar{E}$ to Z, Yn	-	-	85	-	95	-	105	ns
<b><math>V_{CC} = 4.5\text{ V}</math></b>										
$t_{pd}$	propagation delay	see <a href="#">Figure 10</a>	<a href="#">[1]</a>							
		Z, Yn to Yn, Z	-	4.0	11.5	-	12.5	-	13.5	ns
		Sn to Z, Yn	-	6.5	13	-	15	-	17	ns
$t_{en}$	enable time	see <a href="#">Figure 11</a>	<a href="#">[2]</a>							
		$\bar{E}$ to Z, Yn	-	-	80	-	90	-	100	ns
$t_{dis}$	disable time	see <a href="#">Figure 11</a>	<a href="#">[3]</a>							
		$\bar{E}$ to Z, Yn	-	-	80	-	90	-	100	ns

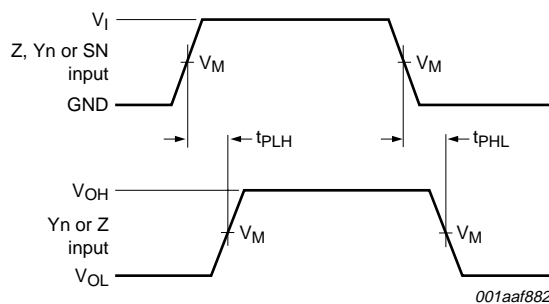
**Table 9. Dynamic characteristics ...continued**

$GND = 0\text{ V}$ ;  $C_L = 50\text{ pF}$ ;  $R_L = 10\text{ K}\Omega$  unless specified otherwise; for test circuit see [Figure 12](#).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b><math>V_{CC} = 6.0\text{ V}</math></b>										
$t_{pd}$	propagation delay	see <a href="#">Figure 10</a> [1]								
		Z, Yn to Yn, Z	-	3.0	10	-	11	-	12	ns
		Sn to Z, Yn	-	5.0	12.5	-	14.5	-	16.5	ns
$t_{en}$	enable time	see <a href="#">Figure 11</a> [2]								
		$\bar{E}$ to Z, Yn	-	-	78	-	80	-	80	ns
$t_{dis}$	disable time	see <a href="#">Figure 11</a> [3]								
		$\bar{E}$ to Z, Yn	-	-	78	-	80	-	80	ns
<b>Power dissipation capacitance</b>										
$C_{PD}$	power dissipation capacitance	per channel [4]								
		$V_{CC} = 3.3\text{ V}$	-	28	-	-	-	-	-	pF
		$V_{CC} = 5.0\text{ V}$	-	33	-	-	-	-	-	pF

- [1]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ .
- [2]  $t_{en}$  is the same as  $t_{PZH}$  and  $t_{PZL}$ .
- [3]  $t_{dis}$  is the same as  $t_{PLZ}$  and  $t_{PHZ}$ .
- [4]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ):  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum\{(C_L + C_{sw}) \times V_{CC}^2 \times f_o\}$  where:  
 $f_i$  = input frequency in MHz;  
 $f_o$  = output frequency in MHz;  
 $\sum\{(C_L + C_{sw}) \times V_{CC}^2 \times f_o\}$  = sum of outputs;  
 $C_L$  = output load capacitance in pF;  
 $C_{sw}$  = switch capacitance in pF;  
 $V_{CC}$  = supply voltage in V.

## 12. Waveforms



Measurement points are given in [Table 10](#).

Logic levels:  $V_{OL}$  and  $V_{OH}$  are typical output voltage drops that occur with the output load.

**Fig 10. Input (Z, Yn or Sn) to output (Yn, Z) propagation delays**

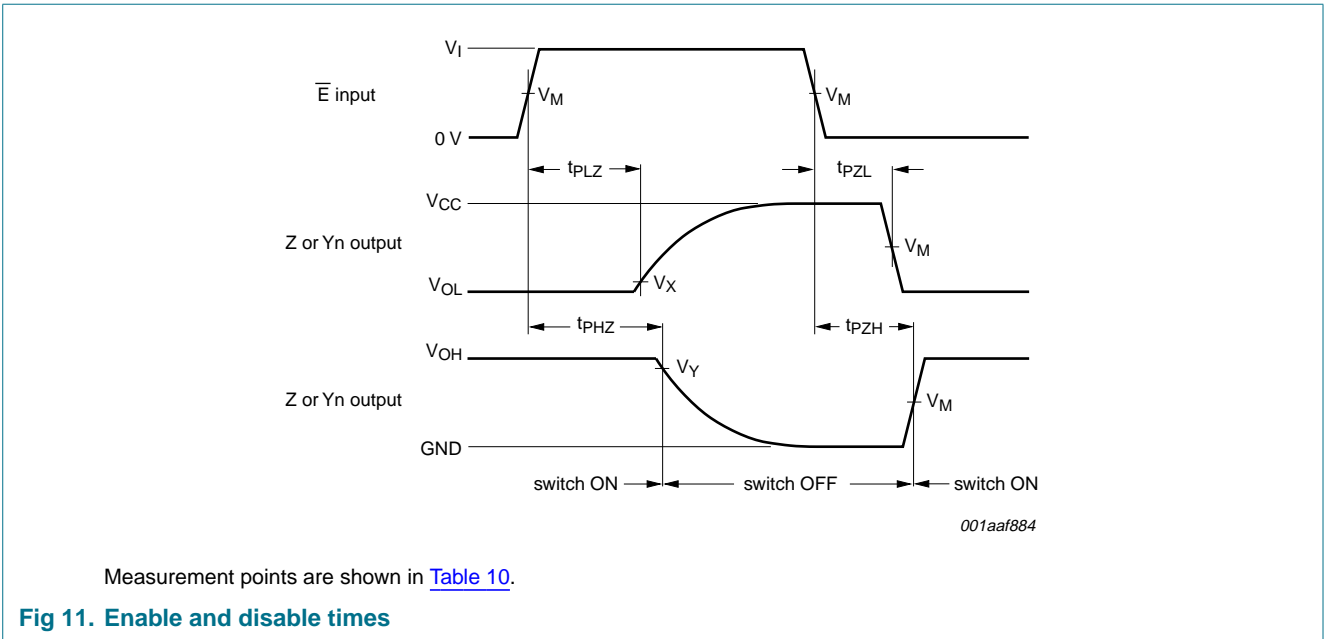
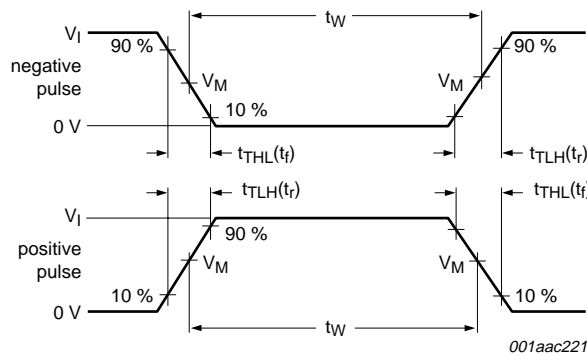
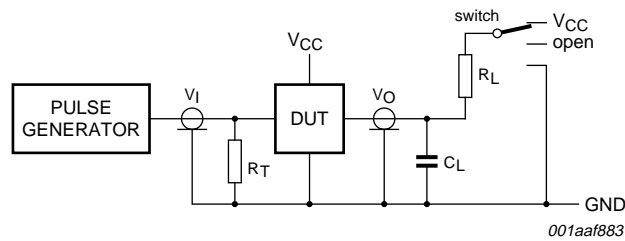


Table 10. Measurement points

Supply voltage	Input		Output		
	$V_M$	$V_I$	$V_M$	$V_X$	$V_Y$
2.0 V to 6.0 V	$0.5 \times V_{CC}$	GND to $V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.1 \times (V_{CC} - V_{OL})$	$0.9 \times V_{OH}$



a. Input pulse definition



Definitions for test circuit:

$R_L$  = load resistance.

$C_L$  = load capacitance including jig and probe capacitance.

$R_T$  = termination resistance should be equal to the output impedance  $Z_o$  of the pulse generator.

b. Load circuitry

Test data is given in [Table 11](#).

Fig 12. Switching times

Table 11. Test data

Test	Input		Switch
	$t_r, t_f$	$V_I$	
$t_{PZH}, t_{PHZ}$	6 ns	$V_{CC}$	GND
$t_{PZL}, t_{PLZ}$	6 ns	GND	$V_{CC}$
$t_{PHL}, t_{PLH}$	6 ns	pulse	open

13. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

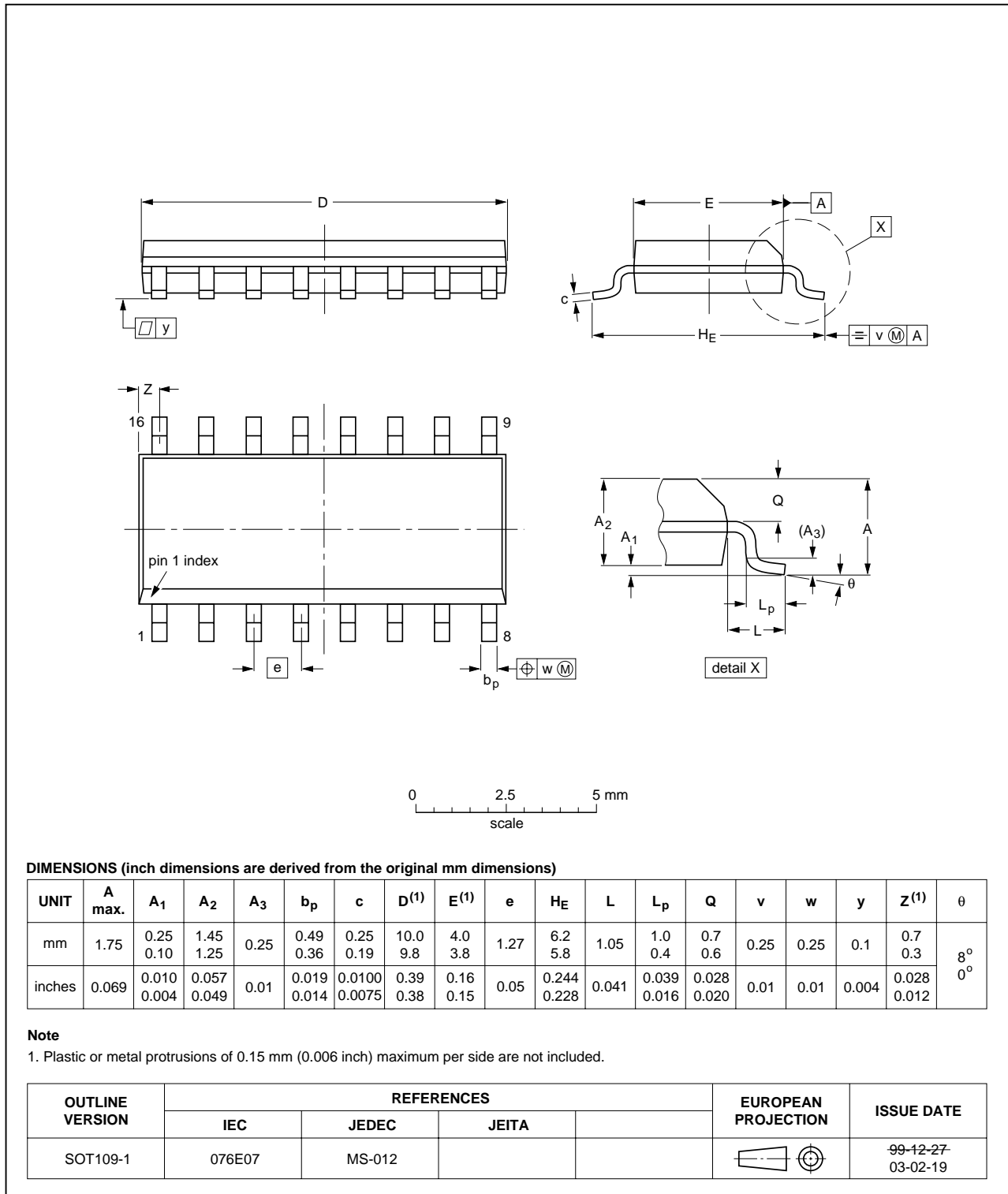


Fig 13. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

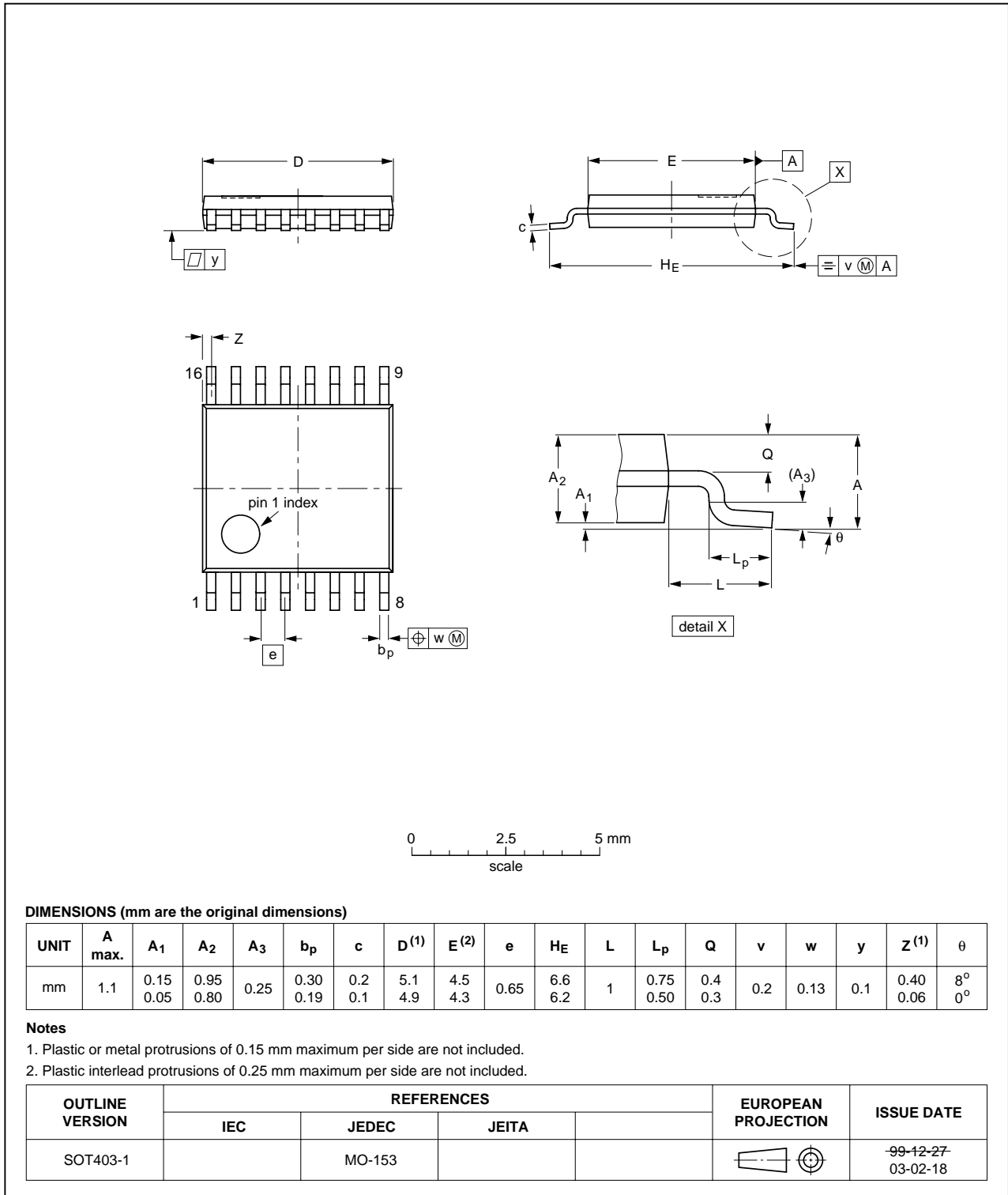


Fig 14. Package outline SOT403-1 (TSSOP16)



DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm

SOT763-1

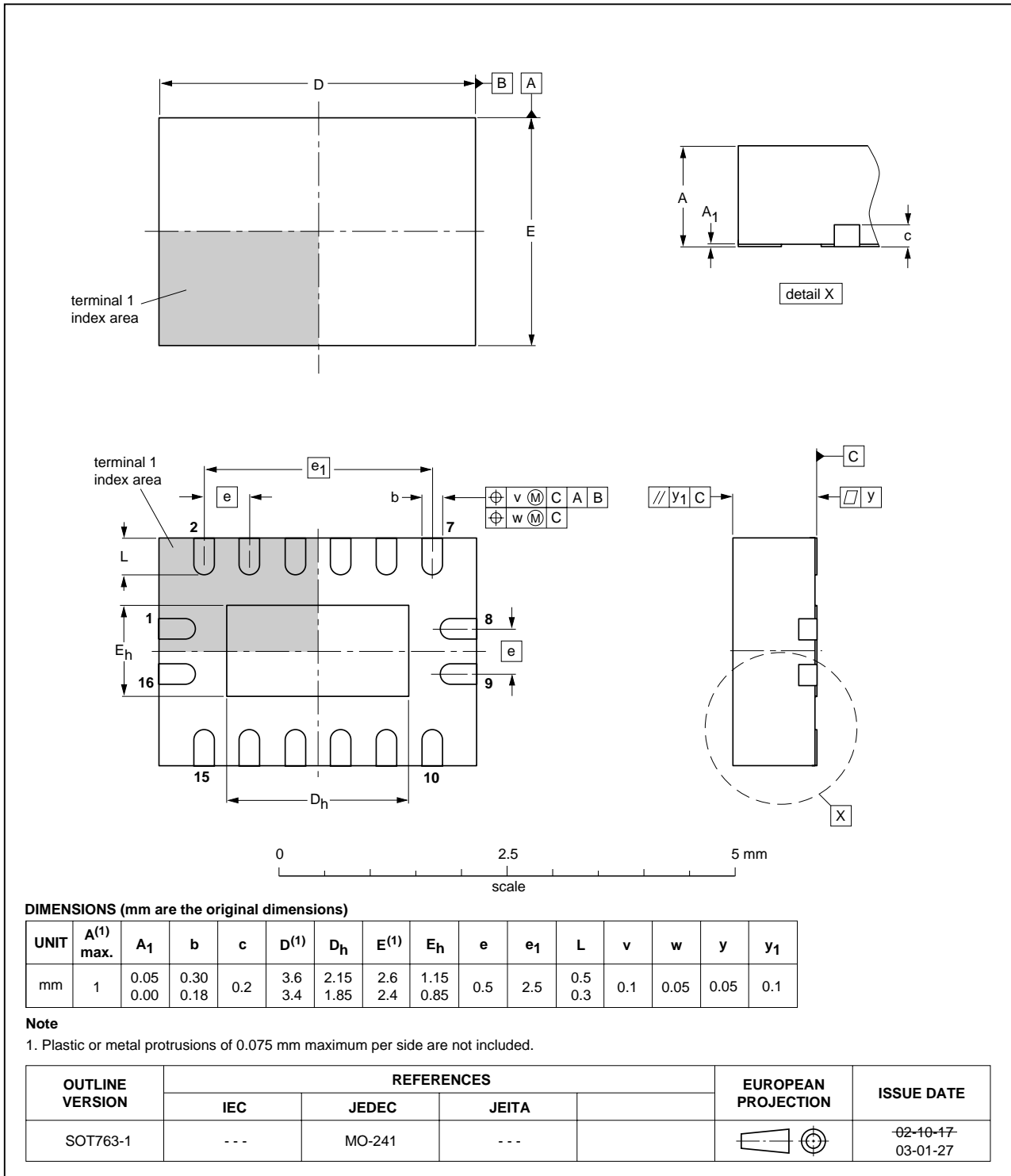


Fig 15. Package outline SOT763-1 (DHVQFN16)

## 14. Abbreviations

Table 12. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

## 15. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC4851_1	20070309	Product data sheet	-	-

## 16. Legal information

### 16.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

### 16.2 Definitions

**Draft** — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Short data sheet** — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

### 16.3 Disclaimers

**General** — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

**Right to make changes** — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use** — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or

malfunction of a NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

**Limiting values** — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

**Terms and conditions of sale** — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

**No offer to sell or license** — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

### 16.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

## 17. Contact information

For additional information, please visit: <http://www.nxp.com>

For sales office addresses, send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

## 18. Contents

<b>1</b>	<b>General description</b> .....	<b>1</b>
<b>2</b>	<b>Features</b> .....	<b>1</b>
<b>3</b>	<b>Applications</b> .....	<b>2</b>
<b>4</b>	<b>Ordering information</b> .....	<b>2</b>
<b>5</b>	<b>Functional diagram</b> .....	<b>2</b>
<b>6</b>	<b>Pinning information</b> .....	<b>4</b>
6.1	Pinning .....	4
6.2	Pin description .....	4
<b>7</b>	<b>Functional description</b> .....	<b>5</b>
<b>8</b>	<b>Limiting values</b> .....	<b>5</b>
<b>9</b>	<b>Recommended operating conditions</b> .....	<b>6</b>
<b>10</b>	<b>Static characteristics</b> .....	<b>6</b>
<b>11</b>	<b>Dynamic characteristics</b> .....	<b>11</b>
<b>12</b>	<b>Waveforms</b> .....	<b>12</b>
<b>13</b>	<b>Package outline</b> .....	<b>15</b>
<b>14</b>	<b>Abbreviations</b> .....	<b>18</b>
<b>15</b>	<b>Revision history</b> .....	<b>18</b>
<b>16</b>	<b>Legal information</b> .....	<b>19</b>
16.1	Data sheet status .....	19
16.2	Definitions .....	19
16.3	Disclaimers .....	19
16.4	Trademarks .....	19
<b>17</b>	<b>Contact information</b> .....	<b>19</b>
<b>18</b>	<b>Contents</b> .....	<b>20</b>

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.



© NXP B.V. 2007.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

Date of release: 9 March 2007

Document identifier: 74HC4851\_1