74HC4852

Dual 4-channel analog multiplexer/demultiplexer with injection-current effect control

Rev. 02 — 30 May 2007 Product data sheet

1. General description

The 74HC4852 is a high-speed Si-gate CMOS device and is specified in compliance with JEDEC standard no. 7A.

The 74HC4852 is a dual 4-channel analog multiplexer or demultiplexer with common select inputs (S0 and S1). Both multiplexers have a common active LOW enable input ($\overline{E}$), four independent inputs/outputs (pins nY0 to nY3) and a common input/output (pin nZ). The device features injection-current effect control, which has excellent value in automotive applications where voltages in excess of the supply voltage are common.

With $\overline{E}$ LOW, two of the eight switches are selected (low impedance ON-state) by S0 and S1. With $\overline{E}$ HIGH, all switches are in the high-impedance OFF-state, independent of S0 and S1.

The injection-current effect control allows signals at disabled analog input channels to exceed the supply voltage without affecting the signal of the enabled analog channel. This eliminates the need for external diode/resistor networks typically used to keep the analog channel signals within the supply-voltage range.

2. Features

- Injection-current cross coupling < 1 mV/mA
- Wide supply voltage range from 2.0 V to 6.0 V
- ESD protection:
  - HBM JESD22-A114E Class 2 exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
  - CDM JESD22-C101C exceeds 1000 V
- Latch-up performance exceeds 100 mA per JESD 78 Class II
- Low ON-state resistance:
  - 400 Ω (typical) at V_{CC} = 2.0 V
  - 215 Ω (typical) at V_{CC} = 3.0 V
  - 120 Ω (typical) at V_{CC} = 3.3 V
  - 76 Ω (typical) at V_{CC} = 4.5 V
  - 59 Ω (typical) at V_{CC} = 6.0 V

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3. Applications

- Analog multiplexing and demultiplexing
- Digital multiplexing and demultiplexing
- Signal gating
- Automotive application

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	**Name**	**Description**	**Version**
74HC4852D	–40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HC4852PW	–40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74HC4852BQ	–40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1

5. Functional diagram

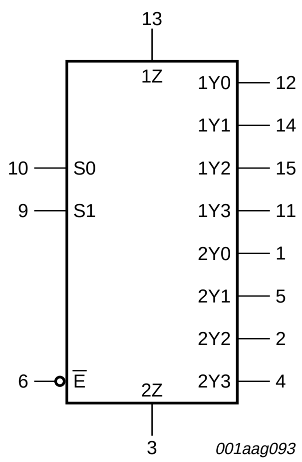


Fig 1. Logic symbol

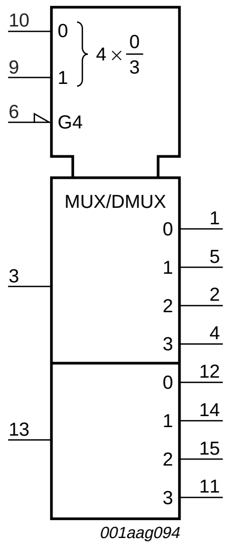


Fig 2. IEC logic symbol

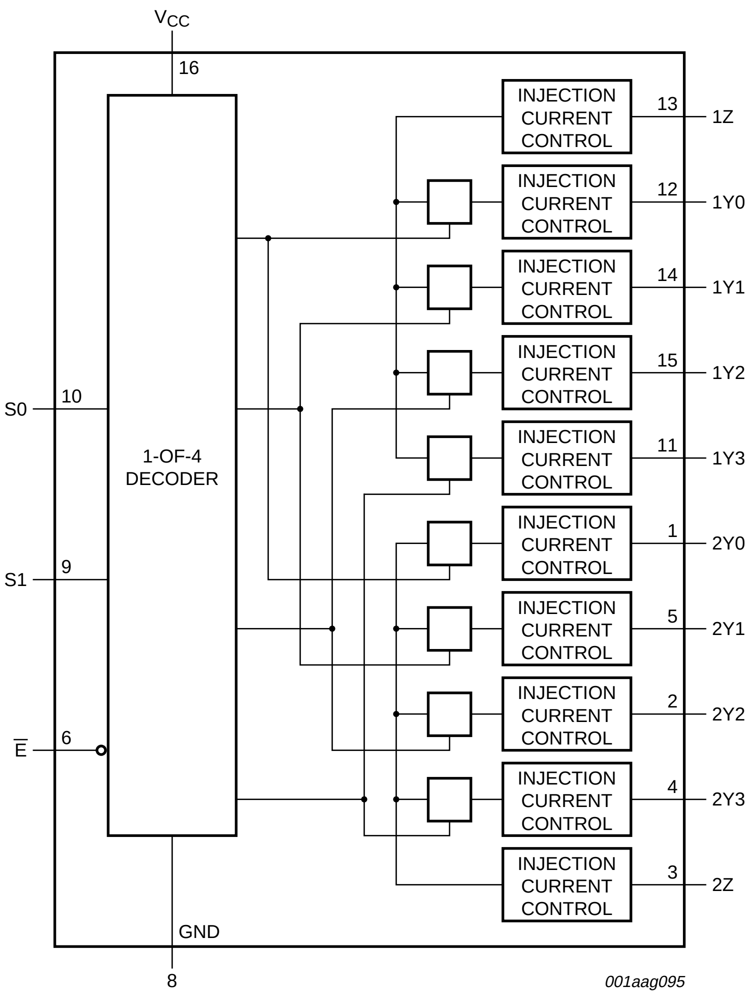


Fig 3. Functional diagram

6. Pinning information

6.1 Pinning

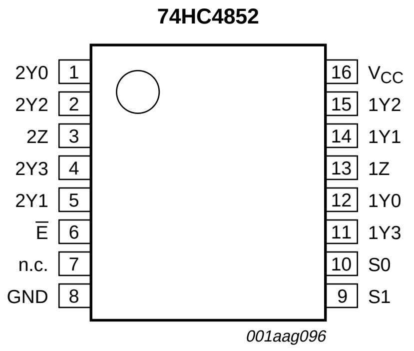
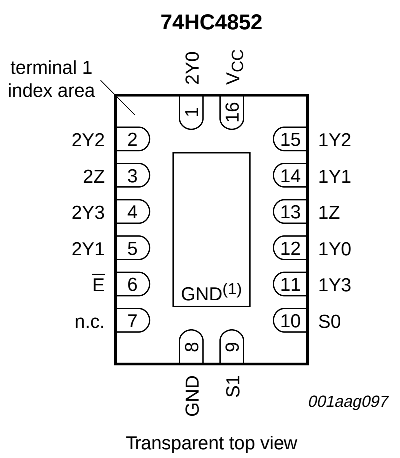


Fig 4. Pin configuration SO16 and TSSOP16



(1) The die substrate is attached to this pad using conductive die attach material. It can not be used as a supply pin or input.

Fig 5. Pin configuration DHVQFN16

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
2Y0	1	independent input/output
2Y2	2	independent input/output
2Z	3	common input/output
2Y3	4	independent input/output
2Y1	5	independent input/output
$\overline{E}$	6	enable input (active LOW)
n.c.	7	not connected
GND	8	ground (0 V)
S1	9	select input
S0	10	select input
1Y3	11	independent input/output
1Y0	12	independent input/output
1Z	13	common input/output
1Y1	14	independent input/output
1Y2	15	independent input/output
V_{CC}	16	positive supply voltage

7. Functional description

Table 3. Function table[1]

Input			Channel ON
$\overline{E}$	S1	S0	
L	L	L	nY0 to nZ
L	L	H	nY1 to nZ
L	H	L	nY2 to nZ
L	H	H	nY3 to nZ
H	X	X	-

[1] H = HIGH voltage level;
L = LOW voltage level;
X = don't care.

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+7.0	V
V_I	input voltage			–0.5	V_{CC} + 0.5	V
V_{SW}	switch voltage	enable and disable mode		–0.5	V_{CC} + 0.5	V
I_{IK}	input clamping current	$V_I < 0$ V or $V_I > V_{CC}$		-	±20	mA
I_{SK}	switch clamping current	$V_I < 0$ V or $V_I > V_{CC}$		-	±20	mA
I_{SW}	switch current	V_{SW} = 0 V to V_{CC}		-	±25	mA
I_{CC}	supply current			-	50	mA
I_{GND}	ground current			–50	-	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation	T_{amb} = –40 °C to +125 °C	[1]	-	500	mW

[1] For SO16 package: P_{tot} derates linearly with 8 mW/K above 70 °C.
For TSSOP16 package: P_{tot} derates linearly with 5.5 mW/K above 60 °C.
For DHVQFN16 packages: P_{tot} derates linearly with 4.5 mW/K above 60 °C.

9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		2.0	-	6.0	V
V_I	input voltage		0	-	V_{CC}	V
V_{SW}	switch voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		–40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V_{CC} = 2.0 V	-	6.0	1000	ns/V
		V_{CC} = 3.0 V	-	6.0	800	ns/V
		V_{CC} = 3.3 V	-	6.0	800	ns/V
		V_{CC} = 4.5 V	-	6.0	500	ns/V
		V_{CC} = 6.0 V	-	6.0	400	ns/V

10. Static characteristics

Table 6. R_{ON} resistance

For test circuit see Figure 8.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
$R_{ON(peak)}$	ON resistance (peak)	$V_I = V_{CC}$ to GND; $\overline{E} = V_{IL}$				
		V_{CC} = 2.0 V; I_{SW} = 2 mA	-	400	650	Ω
		V_{CC} = 3.0 V; $I_{SW} \leq$ 2 mA	-	215	330	Ω
		V_{CC} = 3.3 V; $I_{SW} \leq$ 2 mA	-	120	270	Ω
		V_{CC} = 4.5 V; $I_{SW} \leq$ 2 mA	-	76	210	Ω
		V_{CC} = 6.0 V; $I_{SW} \leq$ 2 mA	-	59	195	Ω
ΔR_{ON}	ON resistance mismatch between channels	$V_I = 0.5 \times V_{CC}$; $\overline{E} = V_{IL}$				
		V_{CC} = 2.0 V; I_{SW} = 2 mA	-	4	10	Ω
		V_{CC} = 3.0 V; $I_{SW} \leq$ 2 mA	-	2	8	Ω
		V_{CC} = 3.3 V; $I_{SW} \leq$ 2 mA	-	2	8	Ω
		V_{CC} = 4.5 V; $I_{SW} \leq$ 2 mA	-	2	8	Ω
		V_{CC} = 6.0 V; $I_{SW} \leq$ 2 mA	-	3	9	Ω
T_{amb} = –40 °C to +85 °C						
$R_{ON(peak)}$	ON resistance (peak)	$V_I = V_{CC}$ to GND; $\overline{E} = V_{IL}$				
		V_{CC} = 2.0 V; I_{SW} = 2 mA	-	-	670	Ω
		V_{CC} = 3.0 V; $I_{SW} \leq$ 2 mA	-	-	360	Ω
		V_{CC} = 3.3 V; $I_{SW} \leq$ 2 mA	-	-	305	Ω
		V_{CC} = 4.5 V; $I_{SW} \leq$ 2 mA	-	-	240	Ω
		V_{CC} = 6.0 V; $I_{SW} \leq$ 2 mA	-	-	220	Ω

Table 6. R_{ON} resistance *…continued*

For test circuit see Figure 8.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ΔR_{ON}	ON resistance mismatch between channels	$V_I = 0.5 \times V_{CC}$; $\overline{E} = V_{IL}$				
		$V_{CC} = 2.0$ V; $I_{SW} = 2$ mA	-	-	15	Ω
		$V_{CC} = 3.0$ V; $I_{SW} \leq 2$ mA	-	-	12	Ω
		$V_{CC} = 3.3$ V; $I_{SW} \leq 2$ mA	-	-	12	Ω
		$V_{CC} = 4.5$ V; $I_{SW} \leq 2$ mA	-	-	12	Ω
		$V_{CC} = 6.0$ V; $I_{SW} \leq 2$ mA	-	-	13	Ω
T_{amb} = −40 °C to +125 °C						
$R_{ON(peak)}$	ON resistance (peak)	$V_I = V_{CC}$ to GND; $\overline{E} = V_{IL}$				
		$V_{CC} = 2.0$ V; $I_{SW} = 2$ mA	-	-	700	Ω
		$V_{CC} = 3.0$ V; $I_{SW} \leq 2$ mA	-	-	380	Ω
		$V_{CC} = 3.3$ V; $I_{SW} \leq 2$ mA	-	-	345	Ω
		$V_{CC} = 4.5$ V; $I_{SW} \leq 2$ mA	-	-	270	Ω
		$V_{CC} = 6.0$ V; $I_{SW} \leq 2$ mA	-	-	250	Ω
ΔR_{ON}	ON resistance mismatch between channels	$V_I = 0.5 \times V_{CC}$; $\overline{E} = V_{IL}$				
		$V_{CC} = 2.0$ V; $I_{SW} = 2$ mA	-	-	20	Ω
		$V_{CC} = 3.0$ V; $I_{SW} \leq 2$ mA	-	-	16	Ω
		$V_{CC} = 3.3$ V; $I_{SW} \leq 2$ mA	-	-	16	Ω
		$V_{CC} = 4.5$ V; $I_{SW} \leq 2$ mA	-	-	16	Ω
		$V_{CC} = 6.0$ V; $I_{SW} \leq 2$ mA	-	-	18	Ω

Table 7. Injection current coupling

For test circuit see Figure 9.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
T_{amb} = −40 °C to +125 °C							
ΔV_O	output voltage variation	$\lvert I_{SW}\rvert \leq 1$ mA; $R_S \leq 3.9$ kΩ	[2][3]				
		$V_{CC} = 3.3$ V		-	0.05	1	mV
		$V_{CC} = 5.0$ V		-	0.03	1	mV
		$\lvert I_{SW}\rvert \leq 10$ mA; $R_S \leq 3.9$ kΩ					
		$V_{CC} = 3.3$ V		-	0.55	5	mV
		$V_{CC} = 5.0$ V		-	0.27	5	mV
		$\lvert I_{SW}\rvert \leq 1$ mA; $R_S \leq 20$ kΩ					
		$V_{CC} = 3.3$ V		-	0.04	2	mV
		$V_{CC} = 5.0$ V		-	0.03	2	mV
		$\lvert I_{SW}\rvert \leq 10$ mA; $R_S \leq 20$ kΩ					
		$V_{CC} = 3.3$ V		-	0.56	20	mV
		$V_{CC} = 5.0$ V		-	0.48	20	mV

[1] Typical values are measured at T_{amb} = 25 °C.

[2] ΔV_O here is the maximum variation of output voltage of an enabled analog channel when current is injected into any disabled channel.

[3] I_{SW} = total current injected into all disabled channels.

Table 8. Static characteristics

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
V_{IH}	HIGH-level input voltage	control inputs				
		V_{CC} = 2.0 V	1.5	-	-	V
		V_{CC} = 3.0 V	2.1	-	-	V
		V_{CC} = 3.3 V	2.3	-	-	V
		V_{CC} = 4.5 V	3.15	-	-	V
		V_{CC} = 6.0 V	4.2	-	-	V
V_{IL}	LOW-level input voltage	control inputs				
		V_{CC} = 2.0 V	-	-	0.5	V
		V_{CC} = 3.0 V	-	-	0.9	V
		V_{CC} = 3.3 V	-	-	1.0	V
		V_{CC} = 4.5 V	-	-	1.35	V
		V_{CC} = 6.0 V	-	-	1.8	V
I_I	input leakage current	control inputs; V_I = GND or V_{CC}				
		V_{CC} = 6.0 V	-	-	±0.1	µA
$I_{S(OFF)}$	OFF-state leakage current	$\overline{E}$ = V_{IH}; V_I = GND or V_{CC}; V_O = V_{CC} or GND; V_{CC} = 6.0 V; see Figure 6				
		nYn; per channel	-	-	±0.1	µA
		nZ; all channels	-	-	±0.2	µA
$I_{S(ON)}$	ON-state leakage current	$\overline{E}$ = V_{IL}; V_I = GND or V_{CC}; V_O = V_{CC} or GND; V_{CC} = 6.0 V; see Figure 7	-	-	±0.1	µA
I_{CC}	supply current	V_I = GND or V_{CC}				
		V_{CC} = 6.0 V	-	-	2.0	µA
C_I	input capacitance	S0, S1 and $\overline{E}$	-	2	10	pF
C_{sw}	switch capacitance	nZ; OFF-state	-	9	40	pF
		nYn; OFF-state	-	3	15	pF
T_{amb} = −40 °C to +85 °C						
V_{IH}	HIGH-level input voltage	control inputs				
		V_{CC} = 2.0 V	1.5	-	-	V
		V_{CC} = 3.0 V	2.1	-	-	V
		V_{CC} = 3.3 V	2.3	-	-	V
		V_{CC} = 4.5 V	3.15	-	-	V
		V_{CC} = 6.0 V	4.2	-	-	V
V_{IL}	LOW-level input voltage	control inputs				
		V_{CC} = 2.0 V	-	-	0.5	V
		V_{CC} = 3.0 V	-	-	0.9	V
		V_{CC} = 3.3 V	-	-	1.0	V
		V_{CC} = 4.5 V	-	-	1.35	V
		V_{CC} = 6.0 V	-	-	1.8	V

Table 8. Static characteristics *...continued*

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_I	input leakage current	control inputs; V_I = GND or V_{CC}				
		V_{CC} = 6.0 V	-	-	±0.1	µA
$I_{S(OFF)}$	OFF-state leakage current	$\overline{E}$ = V_{IH}; V_I = GND or V_{CC}; V_O = V_{CC} or GND; V_{CC} = 6.0 V; see Figure 6				
		nYn; per channel	-	-	±0.5	µA
		nZ; all channels	-	-	±2.0	µA
$I_{S(ON)}$	ON-state leakage current	$\overline{E}$ = V_{IL}; V_I = GND or V_{CC}; V_O = V_{CC} or GND; V_{CC} = 6.0 V; see Figure 7	-	-	±2.0	µA
I_{CC}	supply current	V_I = GND or V_{CC}				
		V_{CC} = 6.0 V	-	-	5	µA
C_I	input capacitance	S0, S1 and $\overline{E}$	-	-	10	pF
C_{sw}	switch capacitance	nZ; OFF-state	-	-	40	pF
		nYn; OFF-state	-	-	15	pF
T_{amb} = −40 °C to +125 °C						
V_{IH}	HIGH-level input voltage	control inputs				
		V_{CC} = 2.0 V	1.5	-	-	V
		V_{CC} = 3.0 V	2.1	-	-	V
		V_{CC} = 3.3 V	2.3	-	-	V
		V_{CC} = 4.5 V	3.15	-	-	V
		V_{CC} = 6.0 V	4.2	-	-	V
V_{IL}	LOW-level input voltage	control inputs				
		V_{CC} = 2.0 V	-	-	0.5	V
		V_{CC} = 3.0 V	-	-	0.9	V
		V_{CC} = 3.3 V	-	-	1.0	V
		V_{CC} = 4.5 V	-	-	1.35	V
		V_{CC} = 6.0 V	-	-	1.8	V
I_I	input leakage current	control inputs; V_I = GND or V_{CC}				
		V_{CC} = 6.0 V	-	-	±1.0	µA
$I_{S(OFF)}$	OFF-state leakage current	$\overline{E}$ = V_{IH}; V_I = GND or V_{CC}; V_O = V_{CC} or GND; V_{CC} = 6.0 V; see Figure 6				
		nYn; per channel	-	-	±2.0	µA
		nZ; all channels	-	-	±10.0	µA
$I_{S(ON)}$	ON-state leakage current	$\overline{E}$ = V_{IL}; V_I = GND or V_{CC}; V_O = V_{CC} or GND; V_{CC} = 6.0 V; see Figure 7	-	-	±10.0	µA
I_{CC}	supply current	V_I = GND or V_{CC}				
		V_{CC} = 6.0 V	-	-	20.0	µA

Table 8. Static characteristics *...continued*

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_I	input capacitance	S0, S1 and $\overline{E}$	-	-	10	pF
C_{sw}	switch capacitance	nZ; OFF-state	-	-	40	pF
		nYn; OFF-state	-	-	15	pF

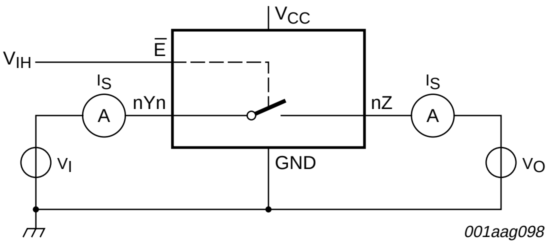
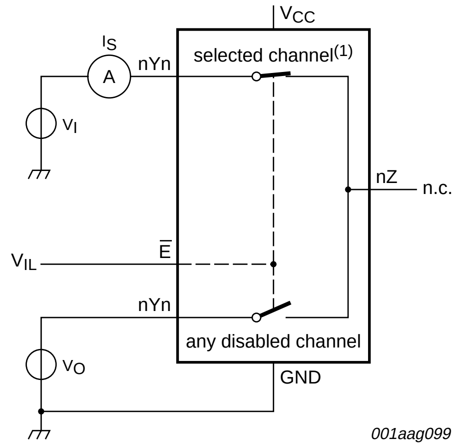
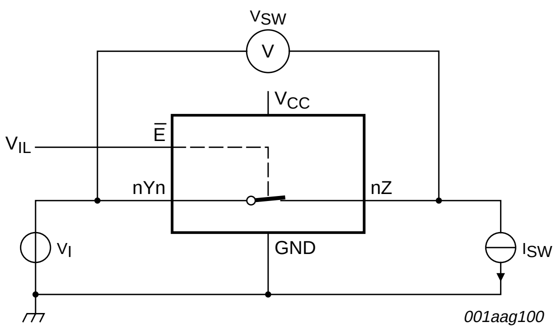


Fig 6. Test circuit for measuring OFF-state leakage current



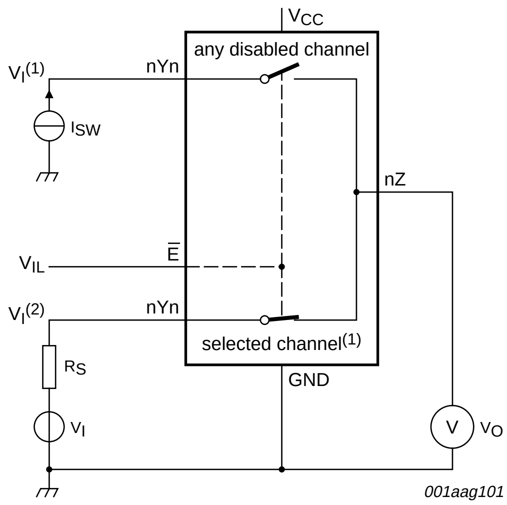
(1) Channel is selected by S0 and S1.

Fig 7. Test circuit for measuring ON-state leakage current



$R_{ON} = V_{SW} / I_{SW}$.

Fig 8. Test circuit for measuring ON resistance



(1) Channel is selected by S0 and S1.

$V_I^{(1)}$ < GND or $V_I^{(1)} > V_{CC}$.

GND < $V_I^{(2)} < V_{CC}$.

Fig 9. Test circuit for injection current coupling

11. Dynamic characteristics

Table 9. Dynamic characteristics

GND = 0 V; C_L = 50 pF; R_L = 10 kΩ unless specified otherwise; for test circuit see Figure 12.

Symbol	Parameter	Conditions		25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
V_{CC} = 2.0 V											
t_{pd}	propagation delay	see Figure 10	[1]								
		nZ, nYn to nYn, nZ		2.2	9.3	33	2.2	34	2.2	35	ns
		Sn to nZ, nYn		7.7	16.8	38	6.3	40	6.3	42	ns
t_{en}	enable time	see Figure 11	[2]								
		$\overline{E}$ to nZ, nYn		10.5	20.5	47.5	8.5	52.5	8.5	57.5	ns
t_{dis}	disable time	see Figure 11	[3]								
		$\overline{E}$ to nZ, nYn		39.5	75.4	100	39.3	105	39	115	ns
V_{CC} = 3.0 V											
t_{pd}	propagation delay	see Figure 10	[1]								
		nZ, nYn to nYn, nZ		2.2	4.9	16.5	1.9	18	1.9	19.5	ns
		Sn to nZ, nYn		4.9	8.8	20	3.9	21.5	3.9	23	ns
t_{en}	enable time	see Figure 11	[2]								
		$\overline{E}$ to nZ, nYn		6.2	10.6	45	5.2	50	5.2	55	ns
t_{dis}	disable time	see Figure 11	[3]								
		$\overline{E}$ to nZ, nYn		35.2	69.5	90	35.5	100	35	110	ns
V_{CC} = 3.3 V											
t_{pd}	propagation delay	see Figure 10	[1]								
		nZ, nYn to nYn, nZ		2.0	4.4	15.0	1.6	16.5	1.6	18.5	ns
		Sn to nZ, nYn		4.4	7.9	17.5	3.4	19	3.4	22	ns
t_{en}	enable time	see Figure 11	[2]								
		$\overline{E}$ to nZ, nYn		5.6	9.4	42.5	4.6	47.5	4.6	52.5	ns
t_{dis}	disable time	see Figure 11	[3]								
		$\overline{E}$ to nZ, nYn		34.6	68.1	85	34.6	95	34.5	105	ns
V_{CC} = 4.5 V											
t_{pd}	propagation delay	see Figure 10	[1]								
		nZ, nYn to nYn, nZ		1.6	3.2	11.6	1.1	12.5	1.1	13.5	ns
		Sn to nZ, nYn		3.2	5.8	14	2.3	15	2.3	17	ns
t_{en}	enable time	see Figure 11	[2]								
		$\overline{E}$ to nZ, nYn		4.2	6.9	40	3	45	3	50	ns
t_{dis}	disable time	see Figure 11	[3]								
		$\overline{E}$ to nZ, nYn		28.5	63	80	28.2	90	28	100	ns

Table 9. Dynamic characteristics *...continued*
GND = 0 V; C_L = 50 pF; R_L = 10 kΩ unless specified otherwise; for test circuit see Figure 12.

Symbol	Parameter	Conditions		25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
V_{CC} = 6.0 V											
t_{pd}	propagation delay	see Figure 10	[1]								
		nZ, nYn to nYn, nZ		1.5	2.5	10.2	0.9	11	0.9	12	ns
		Sn to nZ, nYn		2.4	4.8	12.6	1.6	14.5	1.6	16.5	ns
t_{en}	enable time	see Figure 11	[2]								
		$\overline{E}$ to nZ, nYn		3.2	5.6	39	2.2	40	2.2	40	ns
t_{dis}	disable time	see Figure 11	[3]								
		$\overline{E}$ to nZ, nYn		14.4	57.9	78	13.5	80	13.0	80	ns
Power dissipation capacitance											
C_{PD}	power dissipation capacitance	per channel	[4]								
		V_{CC} = 3.3 V		-	42	-	-	-	-	-	pF
		V_{CC} = 5.0 V		-	47	-	-	-	-	-	pF

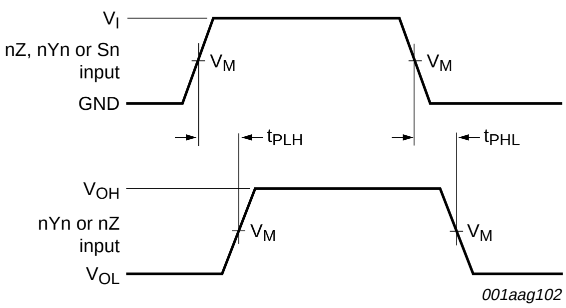
[1] t_{pd} is the same as t_{PLH} and t_{PHL}.

[2] t_{en} is the same as t_{PZH} and t_{PZL}.

[3] t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum\{(C_L + C_{sw}) \times V_{CC}^2 \times f_o\}$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
$\sum\{(C_L + C_{sw}) \times V_{CC}^2 \times f_o\}$ = sum of outputs;
C_L = output load capacitance in pF;
C_{sw} = switch capacitance in pF;
V_{CC} = supply voltage in V.

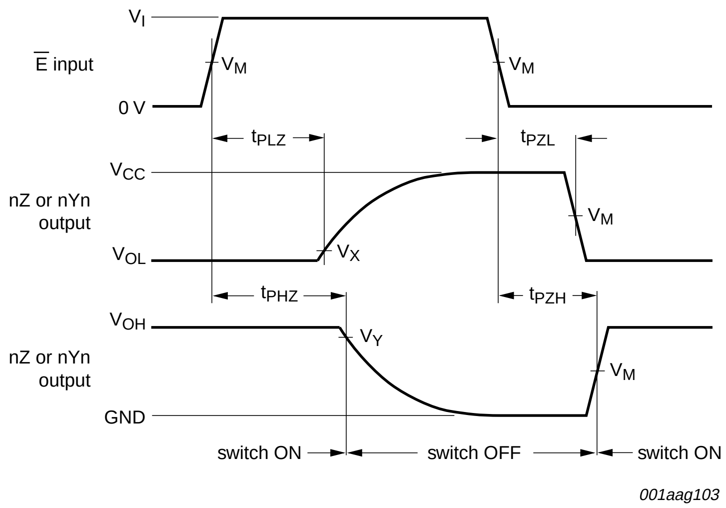
12. Waveforms



Measurement points are given in Table 10.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 10. Input (nZ, nYn or Sn) to output (nYn, nZ) propagation delays



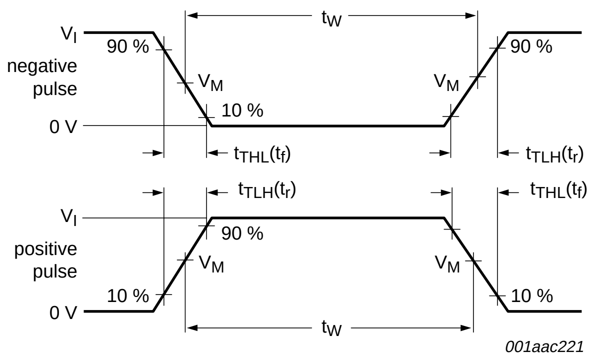
Test data is given in Table 10.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

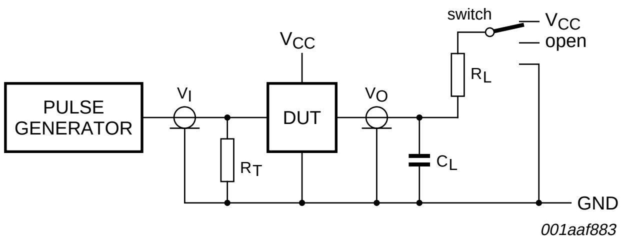
Fig 11. Enable and disable times

Table 10. Measurement points

Supply voltage	Input		Output		
V_{CC}	V_M	V_I	V_M	V_X	V_Y
2.0 V to 6.0 V	$0.5 \times V_{CC}$	GND to V_{CC}	$0.5 \times V_{CC}$	$V_{OL} + 0.1 \times (V_{CC} - V_{OL})$	$0.9 \times V_{OH}$



a. Input pulse definition



Definitions for test circuit:

R_L = load resistance.

C_L = load capacitance including jig and probe capacitance.

R_T = termination resistance should be equal to the output impedance Z_o of the pulse generator.

b. Load circuitry

Test data is given in Table 11.

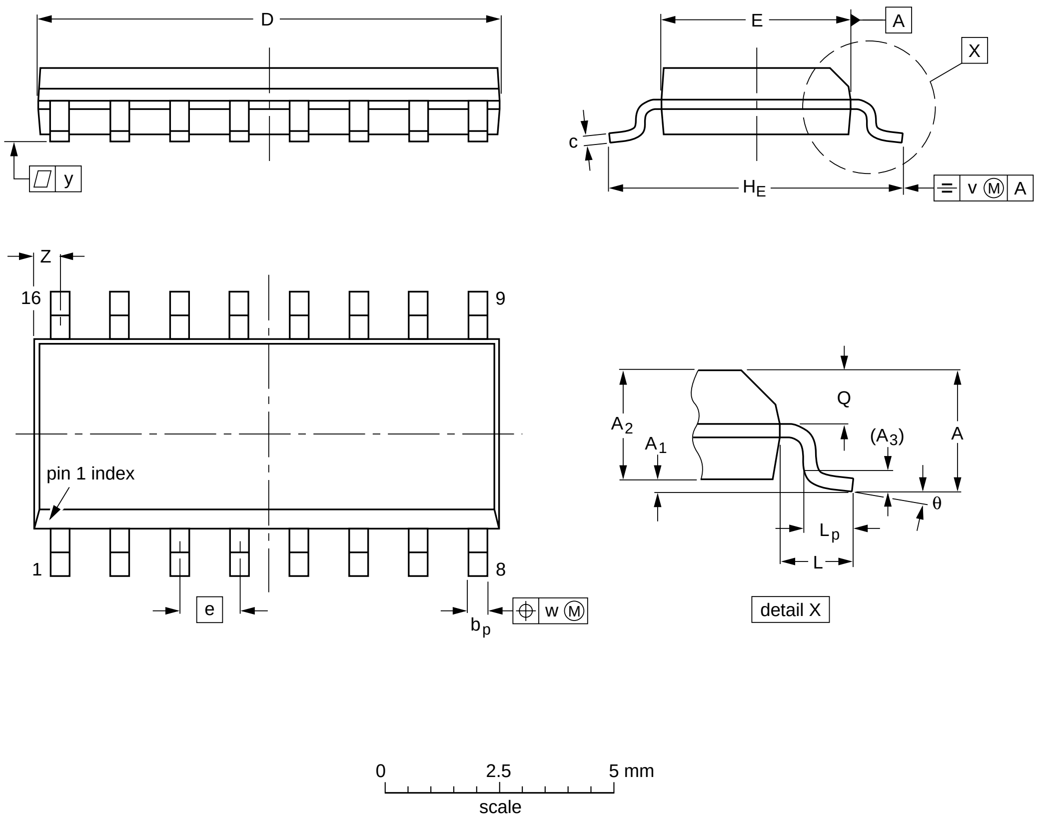
Fig 12. Load circuitry for switching times

Table 11. Test data

Test	Input		Switch
	t_r, t_f	V_I	
t_{PZH}, t_{PHZ}	6 ns	V_{CC}	GND
t_{PZL}, t_{PLZ}	6 ns	GND	V_{CC}
t_{PHL}, t_{PLH}	6 ns	pulse	open

13. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D [(1)]	E [(1)]	e	H_E	L	L_p	Q	v	w	y	Z [(1)]	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

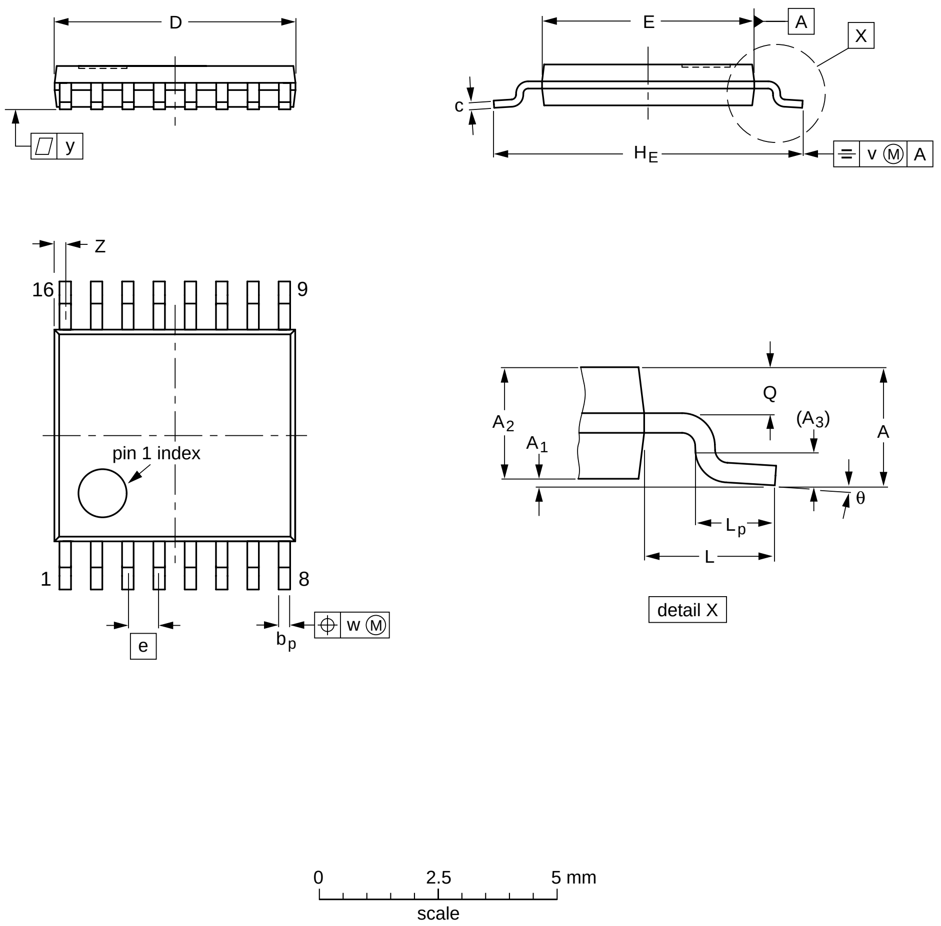
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig 13. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8^{o} 0^{o}

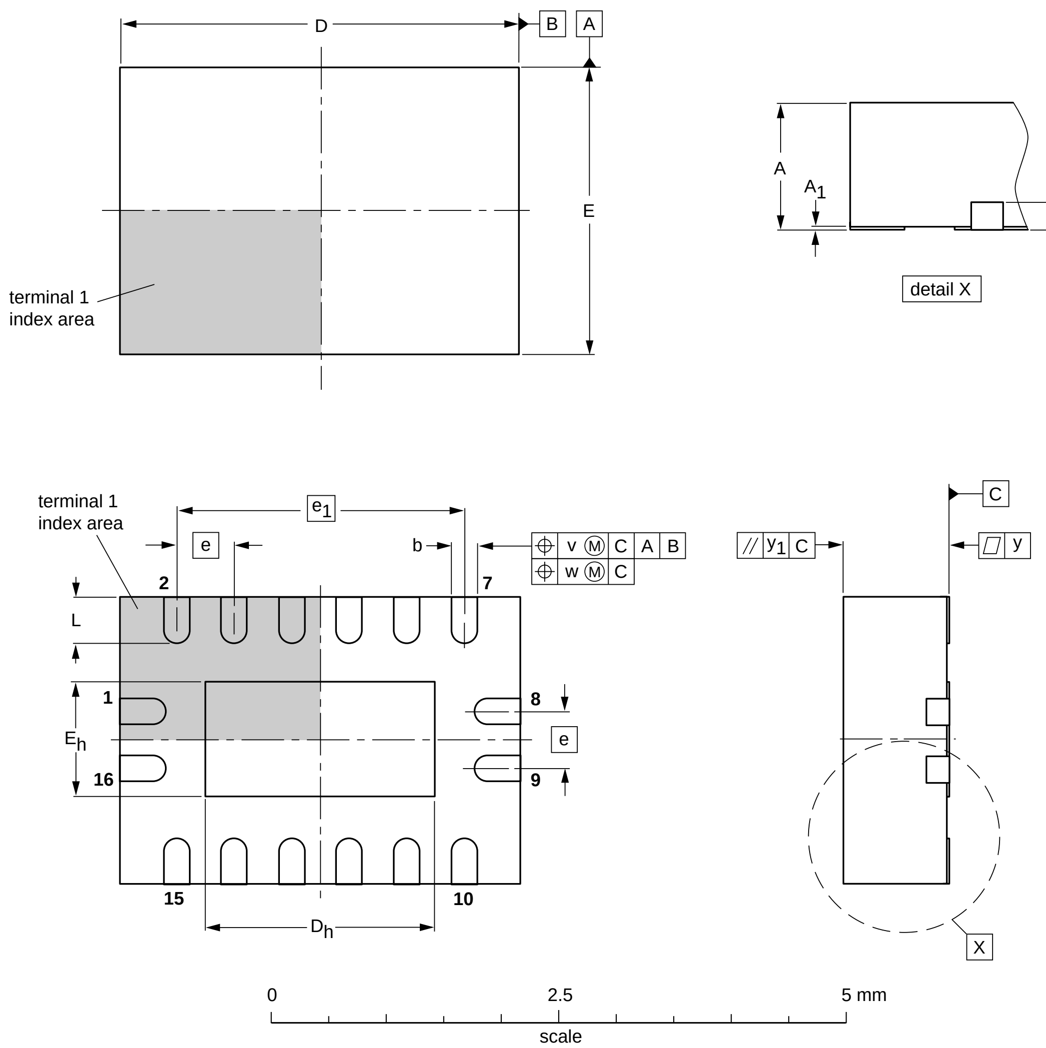
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Fig 14. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm **SOT763-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	3.6 3.4	2.15 1.85	2.6 2.4	1.15 0.85	0.5	2.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT763-1	- - -	MO-241	- - -			~~02-10-17~~ 03-01-27

Fig 15. Package outline SOT763-1 (DHVQFN16)

14. Abbreviations

Table 12. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

15. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC4852_2	20070530	Product data sheet		74HC4852_1
Modifications:	• Typo corrected (“one of the eight switches” to “two of the eight switches”) in Section 1 “General description”.			
74HC4852_1	20070323	Product data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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