

# 16-bit bus transceiver with direction pin; 5V tolerant (3-State)

**74LVC16245A/  
74LVCH16245A**

## FEATURES

- 5 volt tolerant inputs/outputs for interfacing with 5V logic
- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A
- CMOS low power consumption
- MULTIBYTE™ flow-through standard pin-out architecture
- Low inductance multiple power and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- High impedance when  $V_{CC} = 0$
- All data inputs have bus hold (74LVCH16245A only)

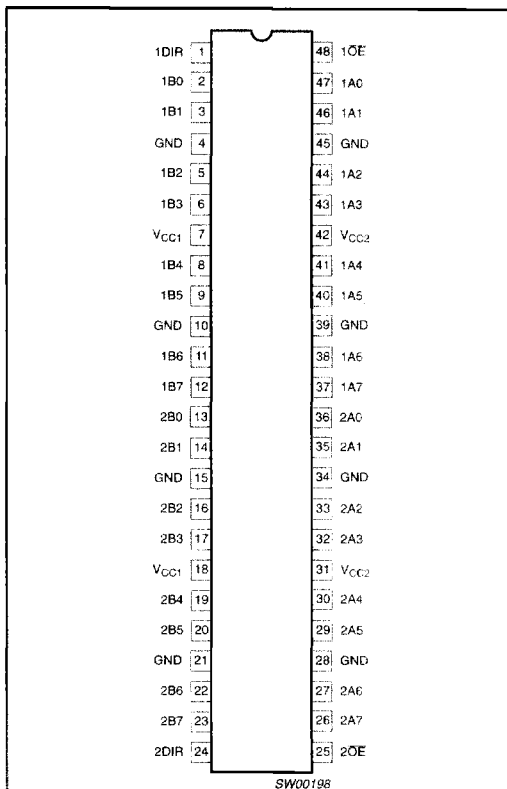
## DESCRIPTION

The 74LVC(H)16245A is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families. Inputs can be driven from either 3.3V or 5V devices. In 3-State operation, outputs can handle 5V. These features allow the use of these devices in a mixed 3.3V/5V environment.

The 74LVC(H)16245A is a 16-bit transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. The 74LVC(H)16245A features two output enable ( $n\bar{O}E$ ) inputs for easy cascading and two send/receive ( $n\bar{D}IR$ ) inputs for direction control.  $n\bar{O}E$  controls the outputs so that the buses are effectively isolated. This device can be used as two 8-bit transceivers or one 16-bit transceiver.

The 74LVCH16245A bus hold data inputs eliminates the need for extreme pull up resistors to hold unused inputs.

## PIN CONFIGURATION



## ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
48-Pin Plastic SSOP Type III	-40°C to +85°C	74LVC16245A DL	VC16245A DL	SOT370-1
48-Pin Plastic TSSOP Type II	-40°C to +85°C	74LVC16245A DGG	VC16245A DGG	SOT362-1
48-Pin Plastic SSOP Type III	-40°C to +85°C	74LVCH16245A DL	VCH16245A DL	SOT370-1
48-Pin Plastic TSSOP Type II	-40°C to +85°C	74LVCH16245A DGG	VCH16245A DGG	SOT362-1

## QUICK REFERENCE DATA

GND = 0V;  $T_{amb} = 25^\circ\text{C}$ ;  $t_r = t_f \leq 2.5\text{ns}$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
$t_{PHL}/t_{PLH}$	Propagation delay An to Bn; Bn to An	$C_L = 50\text{pF}$ $V_{CC} = 3.3\text{V}$	3.0	ns
$C_i$	Input capacitance		5.0	pF
$C_{i/O}$	Input/output capacitance		10	pF
$C_{PD}$	Power dissipation capacitance per buffer	$V_i = \text{GND to } V_{CC}^1$	30	pF

### NOTES:

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ):  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$  where:  
 $f_i$  = input frequency in MHz;  $C_L$  = output load capacity in pF;  
 $f_o$  = output frequency in MHz;  $V_{CC}$  = supply voltage in V;  
 $\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.

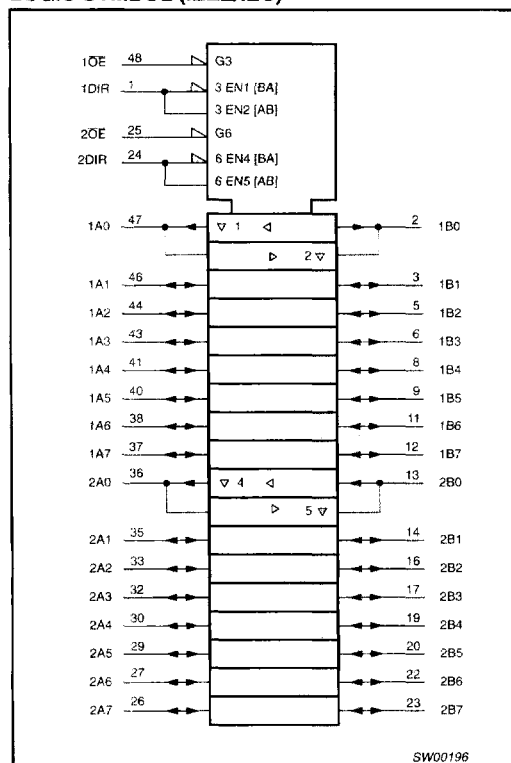
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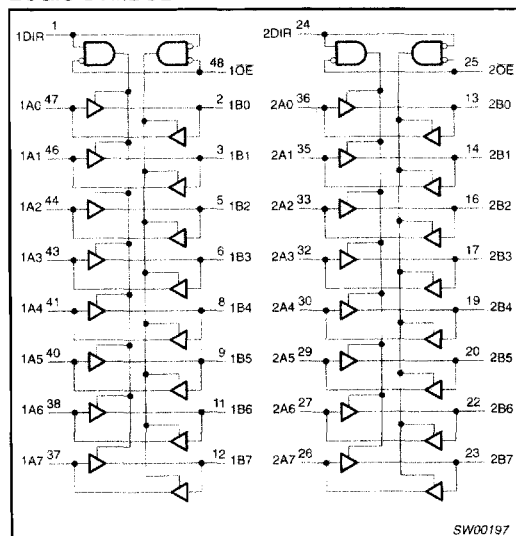
## PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	1DIR	Direction control
2, 3, 5, 6, 8, 9, 11, 12	1B0 to 1B7	Data inputs/outputs
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V <sub>CC</sub>	Positive supply voltage
13, 14, 16, 17, 19, 20, 22, 23	2B0 to 2B7	Data inputs/outputs
24	2DIR	Direction control
25	2OE	Output enable input (active LOW)
36, 35, 33, 32, 30, 29, 27, 26	2A0 to 2A7	Data inputs/outputs
47, 46, 44, 43, 41, 40, 38, 37	1A0 to 1A7	Data inputs/outputs
48	1OE	Output enable input (active LOW)

## LOGIC SYMBOL (IEEE/IEC)



## LOGIC SYMBOL

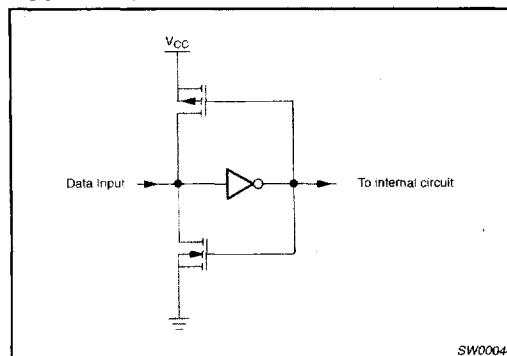


## FUNCTION TABLE

INPUTS		INPUTS/OUTPUT	
nOE	nDIR	nAn	nBn
L	L	A = B	inputs
L	H	inputs	B = A
H	X	Z	Z

H = HIGH voltage level  
L = LOW voltage level  
X = don't care  
Z = high impedance OFF-state

## BUS HOLD CIRCUIT



# 16-bit bus transceiver with direction pin; 5V tolerant (3-State)

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### RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN.	MAX.	
$V_{CC}$	DC supply voltage (for max. speed performance)		2.7	3.6	V
$V_{CC}$	DC supply voltage (for low-voltage applications)		1.2	3.6	V
$V_I$	DC input voltage range		0	5.5	V
$V_O$	DC output voltage range; output HIGH or LOW state		0	$V_{CC}$	V
$V_O$	DC output voltage range; output 3-State		0	5.5	V
$T_{amb}$	Operating ambient temperature range in free air		-40	+85	°C
$t_r, t_f$	Input rise and fall times	$V_{CC} = 1.2$ to $2.7V$ $V_{CC} = 2.7$ to $3.6V$	0	20 10	ns/V

### ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

In accordance with the Absolute Maximum Rating System (IEC 134) Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
$V_{CC}$	DC supply voltage		-0.5	+6.5	V
$I_{IK}$	DC input diode current	$V_I < 0$	-	-50	mA
$V_I$	DC input voltage	Note 2	-0.5	+6.5	V
$I_{OK}$	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	-	±50	mA
$V_O$	DC output voltage; output HIGH or LOW state	Note 2	-0.5	$V_{CC} + 0.5$	V
$V_O$	DC output voltage; output 3-State	Note 2	-0.5	6.5	V
$I_O$	DC output source or sink current	$V_O = 0$ to $V_{CC}$	-	±50	mA
$I_{GND}, I_{CC}$	DC $V_{CC}$ or GND current		-	±100	mA
$T_{stg}$	Storage temperature range		-65	+150	°C
$P_{tot}$	Power dissipation per package - SO package - SSOP and TSSOP package	Above +70°C derate linearly 8mW/K Above +60°C derate linearly 5.5mW/K		500 500	mW

#### NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output voltage ratings may be exceeded if the input and output clamp current ratings are observed.

# 16-bit bus transceiver with direction pin; 5V tolerant (3-State)

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### DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP <sup>1</sup>	MAX	
V <sub>IH</sub>	HIGH level Input voltage	V <sub>CC</sub> = 1.2V	V <sub>CC</sub>			V
		V <sub>CC</sub> = 2.7 to 3.6V	2.0			
V <sub>IL</sub>	LOW level Input voltage	V <sub>CC</sub> = 1.2V			GND	V
		V <sub>CC</sub> = 2.7 to 3.6V			0.8	
V <sub>OH</sub>	HIGH level output voltage	V <sub>CC</sub> = 2.7V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -12mA	V <sub>CC</sub> - 0.5			V
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -100μA	V <sub>CC</sub> - 0.2	V <sub>CC</sub>		
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -18mA	V <sub>CC</sub> - 0.6			
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -24mA	V <sub>CC</sub> - 0.8			
V <sub>OL</sub>	LOW level output voltage	V <sub>CC</sub> = 2.7V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 12mA			0.40	V
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 100μA			0.20	
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 24mA			0.55	
I <sub>I</sub>	Input leakage current	V <sub>CC</sub> = 3.6V; V <sub>I</sub> = 5.5V or GND		±0.1	±5	μA
I <sub>OZ</sub>	3-State output OFF-state current <sup>7</sup>	V <sub>CC</sub> = 3.6V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = 5.5V or GND		0.1	±5	μA
I <sub>off</sub>	Power off leakage supply	V <sub>CC</sub> = 0.0V; V <sub>I</sub> or V <sub>O</sub> = 5.5V		0.1	±10	μA
I <sub>CC</sub>	Quiescent supply current	V <sub>CC</sub> = 3.6V; V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0		0.1	20	μA
ΔI <sub>CC</sub>	Additional quiescent supply current per input pin	V <sub>CC</sub> = 2.7V to 3.6V; V <sub>I</sub> = V <sub>CC</sub> - 0.6V; I <sub>O</sub> = 0		5	500	μA
I <sub>BHL</sub>	Bus hold LOW sustaining current	V <sub>CC</sub> = 3.0V; V <sub>I</sub> = 0.8V <sup>2, 3, 4</sup>	75			μA
I <sub>BHH</sub>	Bus hold HIGH sustaining current	V <sub>CC</sub> = 3.0V; V <sub>I</sub> = 2.0V <sup>2, 3, 4</sup>	-75			μA
I <sub>BHLO</sub>	Bus hold LOW overdrive current	V <sub>CC</sub> = 3.6V <sup>2, 3, 5</sup>	500			μA
I <sub>BHHO</sub>	Bus hold HIGH overdrive current	V <sub>CC</sub> = 3.6V <sup>2, 3, 5</sup>	-500			μA

#### NOTES:

- All typical values are at V<sub>CC</sub> = 3.3V and T<sub>amb</sub> = 25°C.
- Valid for data inputs of bus hold parts (LVCH16-A) only.
- For data inputs only, control inputs do not have a bus hold circuit.
- The specified sustaining current at the data input holds the input below the specified V<sub>I</sub> level.
- The specified overdrive current at the data input forces the data input to the opposite logic input state.
- For bus hold parts, the bus hold circuit is switched off when V<sub>I</sub> exceeds V<sub>CC</sub> allowing 5.5V on the input terminal.
- For I/O ports the parameter I<sub>OZ</sub> includes the input leakage current.

### AC CHARACTERISTICS

GND = 0V; t<sub>R</sub> = t<sub>F</sub> = 2.5ns; C<sub>L</sub> = 50pF; R<sub>L</sub> = 500Ω; T<sub>amb</sub> = -40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS						UNIT
			V <sub>CC</sub> = 3.3V ±0.3V			V <sub>CC</sub> = 2.7V		V <sub>CC</sub> = 1.2V	
			MIN	TYP <sup>1</sup>	MAX	MIN	MAX	TYP	
t <sub>PHL</sub> t <sub>PLH</sub>	Propagation delay nAn to nBn; nBn to nAn	1	1.5	3	4.5	1.5	5.5	13	ns
t <sub>PZH</sub> t <sub>PZL</sub>	3-State output enable time nOE to nAn; nOE to nBn	2, 3	1.5	4	6.1	1.5	7.1	15	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	3-State output disable time nOE to nAn; nOE to nBn	2, 3	1.5	4	5.6	1.5	6.6	11	ns

#### NOTE:

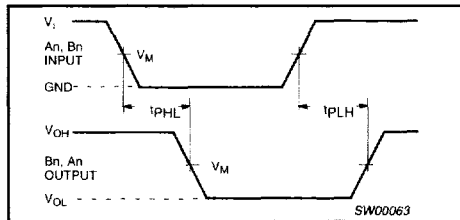
- All typical values are at V<sub>CC</sub> = 3.3V and T<sub>amb</sub> = 25°C.

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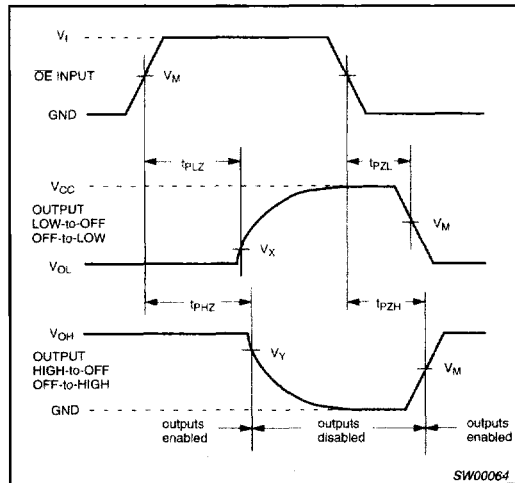
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### AC WAVEFORMS

$V_M = 1.5V$  at  $V_{CC} \geq 2.7V$ ;  $V_M = 0.5 V_{CC}$  at  $V_{CC} < 2.7V$ .  
 $V_{OL}$  and  $V_{OH}$  are the typical output voltage drop that occur with the output load.  
 $V_X = V_{OL} + 0.3V$  at  $V_{CC} \geq 2.7V$ ;  $V_X = V_{OL} + 0.1 V_{CC}$  at  $V_{CC} < 2.7V$   
 $V_Y = V_{OH} - 0.3V$  at  $V_{CC} \geq 2.7V$ ;  $V_Y = V_{OH} - 0.1 V_{CC}$  at  $V_{CC} < 2.7V$

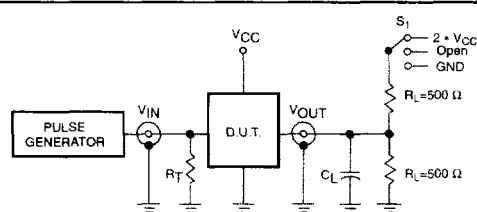


**Waveform 1. Input (nAn, nBn) to output (nBn, nAn) propagation delay times**



**Waveform 2. 3-State enable and disable times**

### TEST CIRCUIT



**Test Circuit for 3-State Outputs**

#### SWITCH POSITION

TEST	SWITCH
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$2 * V_{CC}$
$t_{PHZ}/t_{PZH}$	GND

$V_{CC}$	$V_{IN}$
$< 2.7V$	$V_{CC}$
$2.7 - 3.6V$	$2.7V$

#### DEFINITIONS

- $R_L$  = Load resistor
- $C_L$  = Load capacitance includes jig and probe capacitance
- $R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.

SW00047

**Waveform 3. Load circuitry for switching times**