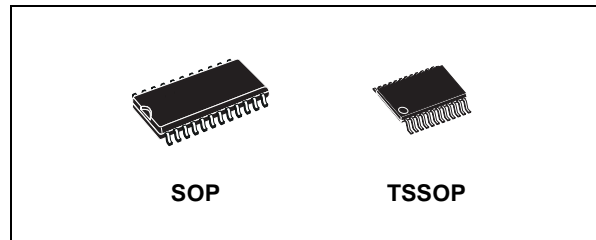




74LVXC3245

OCTAL DUAL SUPPLY BUS TRANSCEIVER

- HIGH SPEED :
 $t_{PD} = 8\text{ns (MAX.)}$ at $T_A=25^\circ\text{C}$
 $V_{CCA} = 3.3\text{V}, V_{CCB} = 5.0\text{V}$
- LOW POWER DISSIPATION:
 $I_{CCA} = I_{CCB} = 5\mu\text{A (MAX.)}$ at $T_A=25^\circ\text{C}$
- LOW NOISE: $V_{OLP} = 0.3\text{V (TYP.)}$ at
 $V_{CCA}=3.3\text{V}$
- SYMMETRICAL OUTPUT IMPEDANCE:
 $|I_{OH}| = I_{OL} = 24\text{mA (MIN)}$
- BALANCED PROPAGATION DELAYS:
 $t_{PLH} \cong t_{PHL}$
- OPERATING VOLTAGE RANGE:
 $V_{CCA}(\text{OPR})=2.7\text{V to }3.6\text{V (1.2V Data Retention)}$
 $V_{CCB}(\text{OPR})=2.7\text{V to }5.5\text{V (1.2V Data Retention)}$
 PIN AND FUNCTION COMPATIBLE WITH
 74 SERIES C3245
- IMPROVED LATCH-UP IMMUNITY



ORDER CODES

PACKAGE	TUBE	T & R
SOP	74LVXC3245M	74LVXC3245MTR
TSSOP		74LVXC3245TTR

This IC is intended for two-way asynchronous communication between data buses and the direction of data transmission is determined by DIR input. The enable input \bar{G} can be used to disable the device so that the buses are effectively isolated.

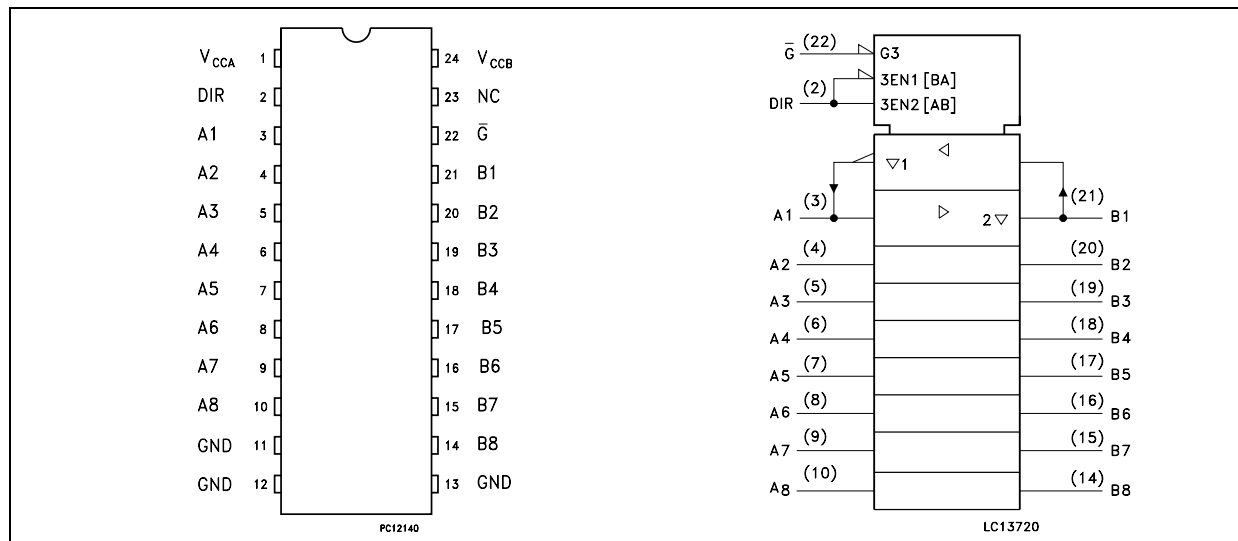
The A-port interfaces with the 3V bus, the B-port with the 5V bus.

All inputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

DESCRIPTION

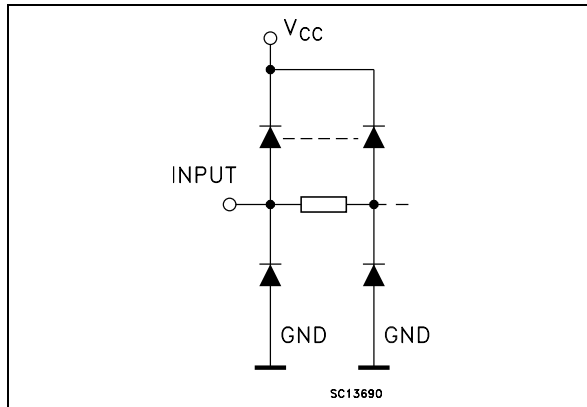
The 74LVXC3245 is a dual supply 8 bit configurable low voltage CMOS OCTAL BUS TRANSCEIVER fabricated with sub-micron silicon gate and double-layer metal wiring C²MOS technology. Designed for use as an interface between a 3.3V bus and a 3.3V to 5V bus in a mixed 3.3V/5V supply systems, it achieves high speed operation while maintaining the CMOS low power dissipation.

PIN CONNECTION AND IEC LOGIC SYMBOLS



74LVXC3245

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
2	DIR	Directional Control
3, 4, 5, 6, 7, 8, 9, 10	A1 to A8	Data Inputs/Outputs
21, 20, 19, 18, 17, 16, 15, 14	B1 to B8	Data Inputs/Outputs
22	G	Output Enable Input
11, 12, 13	GND	Ground (0V)
23	NC	Not Connected
1	V _{CCA}	Positive Supply Voltage
24	V _{CCB}	Positive Supply Voltage

TRUTH TABLE

INPUTS		FUNCTION		OUTPUT
\overline{G}	DIR	A BUS	B BUS	
L	L	OUTPUT	INPUT	A = B
L	H	INPUT	OUTPUT	B = A
H	X	Z	Z	Z

X : Don't Care
Z : High Impedance

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CCA}	Supply Voltage	-0.5 to +7.0	V
V _{CCB}	Supply Voltage	-0.5 to +7.0	V
V _I	DC Input Voltage	-0.5 to V _{CCA} + 0.5	V
V _{I/OA}	DC I/O Voltage	-0.5 to V _{CCA} + 0.5	V
V _{I/OB}	DC I/O Voltage	-0.5 to V _{CCB} + 0.5	V
I _{IK}	DC Input Diode Current	± 20	mA
I _{OK}	DC Output Diode Current	± 50	mA
I _{OA}	DC Output Current	± 50	mA
I _{OB}	DC Output Current	± 50	mA
I _{CCA}	DC V _{CC} or Ground Current	± 200	mA
I _{CCB}	DC V _{CC} or Ground Current	± 100	mA
P _d	Power Dissipation	180	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CCA}	Supply Voltage (note 1)	2.7 to 3.6	V
V_{CCB}	Supply Voltage (note 1)	2.7 to 5.5	V
V_I	Input Voltage	0 to V_{CCA}	V
$V_{I/OA}$	I/O Voltage	0 to V_{CCA}	V
$V_{I/OB}$	I/O Voltage	0 to V_{CCB}	V
T_{op}	Operating Temperature	-55 to 125	°C
dt/dv	Input Rise and Fall Time (note 2)	0 to 10	ns/V

1) V_{IN} from 30% to 70% of V_{CC}
2) $V_{CCA} = 2.7$ to $3.6V$; $V_{CCB} = 2.7$ to $5.5V$;

DC SPECIFICATIONS FOR V_{CCA}

Symbol	Parameter	Test Condition			Value						Unit	
		V_{CCA} (V)	V_{CCB} (V)		$T_A = 25\text{ }^\circ\text{C}$			$-40\text{ to }85\text{ }^\circ\text{C}$		$-55\text{ to }125\text{ }^\circ\text{C}$		
					Min.	Typ.	Max.	Min.	Max.	Min.		Max.
V_{IHA}	High Level Input Voltage	2.7	3.0		2.0			2.0		2.0		V
		3.0	3.6		2.0			2.0		2.0		
		3.6	5.5		2.0			2.0		2.0		
V_{ILA}	Low Level Input Voltage	2.7	3.0				0.8		0.8		0.8	V
		3.0	3.6				0.8		0.8		0.8	
		3.6	5.5				0.8		0.8		0.8	
V_{OHA}	High Level Output Voltage	3.0	3.0	$I_O = -100\text{ }\mu\text{A}$	2.9	2.99		2.9		2.9		V
		3.0	3.0	$I_O = -12\text{ mA}$	2.56	2.85		2.46		2.46		
		3.0	3.0	$I_O = -24\text{ mA}$	2.35	2.65		2.25		2.25		
		2.7	3.0	$I_O = -12\text{ mA}$	2.3	2.5		2.2		2.2		
		2.7	4.5	$I_O = -24\text{ mA}$	2.1	2.3		2.0		2.0		
V_{OLA}	Low Level Output Voltage	3.0	3.0	$I_O = 100\text{ }\mu\text{A}$		0.0	0.1		0.1		0.1	V
		3.0	3.0	$I_O = 24\text{ mA}$		0.21	0.36		0.44		0.44	
		2.7	3.0	$I_O = 12\text{ mA}$		0.11	0.36		0.44		0.44	
		2.7	4.5	$I_O = 24\text{ mA}$		0.22	0.42		0.5		0.5	
I_{IA}	Input Leakage Current	3.6	5.5	$V_I = V_{CC}$ or GND			± 0.1		± 1		± 1	μA
I_{OZA}	High Impedance Output Leakage Current	3.6	5.5	$V_{IA} = V_{IHA}$ or V_{ILA} $V_{IB} = V_{IHB}$ or V_{ILB} $V_{I/OA} = V_{CCA}$ or GND			± 0.5		± 5		± 5	μA
I_{CCIA}	Quiescent Supply Current	3.6	5.5	$V_{IA} = V_{CCA}$ or GND $V_{IB} = V_{CCB}$ or GND			5		50		50	μA
I_{CCIAF}	Quiescent V_{CCA} Supply Current as B Port Floats	3.6	Open	$V_{IA} = \overline{V_{CCA}}$ or GND $\overline{G} = \text{DIR} = V_{CCA}$ $V_{IB} = \text{Open}$			5		50		50	μA
ΔI_{CCIA}	Maximum Quiescent Supply Current / Input (An, DIR, \overline{G})	3.6	5.5	$V_{IA} = V_{CCA} - 0.6\text{V}$ $V_{IB} = V_{CCB}$ or GND			0.35		0.5		0.5	mA

DC SPECIFICATIONS FOR V_{CCB}

Symbol	Parameter	Test Condition			Value						Unit	
		V_{CCA} (V)	V_{CCB} (V)		$T_A = 25\text{ }^\circ\text{C}$			$-40\text{ to }85\text{ }^\circ\text{C}$		$-55\text{ to }125\text{ }^\circ\text{C}$		
					Min.	Typ.	Max.	Min.	Max.	Min.		Max.
V_{IHB}	High Level Input Voltage	2.7	3.0		2.0			2.0		2.0		V
		3.0	3.6		2.0			2.0		2.0		
		3.6	5.5		3.85			3.85		3.85		
V_{ILB}	Low Level Input Voltage	2.7	3.0				0.8		0.8		0.8	V
		3.0	3.6				0.8		0.8		0.8	
		3.6	5.5				1.65		1.65		1.65	
V_{OHB}	High Level Output Voltage	3.0	3.0	$I_O = -100\text{ }\mu\text{A}$	2.9	3.0		2.9		2.9		V
		3.0	3.0	$I_O = -12\text{ mA}$	2.56	2.85		2.46		2.46		
		3.0	3.0	$I_O = -24\text{ mA}$	2.35	2.65		2.25		2.25		
		3.0	4.5	$I_O = -24\text{ mA}$	3.86	4.25		3.76		3.76		
V_{OLB}	Low Level Output Voltage	3.0	3.0	$I_O = 100\text{ }\mu\text{A}$		0.00	0.1		0.1		0.1	V
		3.0	3.0	$I_O = 24\text{ mA}$		0.21	0.36		0.44		0.44	
		3.0	4.5	$I_O = 24\text{ mA}$		0.18	0.36		0.44		0.44	
I_{IB}	Input Leakage Current	3.6	5.5	$V_I = V_{CCA}$ or GND			± 0.1		± 1		± 1	μA
I_{OZB}	High Impedance Output Leakage Current	3.6	5.5	$V_{IA} = V_{IHA}$ or V_{ILA} $V_{IOB} = V_{CCB}$ or GND			± 0.5		± 5		± 5	μA
I_{CCtB}	Quiescent Supply Current	3.6	5.5	$V_{IA} = V_{CCA}$ or GND $V_{IB} = V_{CCB}$ or GND			5		50		50	μA
ΔI_{CCtB}	Maximum Quiescent Supply Current / Input	3.6	5.5	$V_{IA} = V_{CCA}$ or GND $V_{IB} = V_{CCB} - 2.1\text{V}$			1.35		1.5		1.5	mA

DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Condition			Value						Unit	
		V _{CCA} (V)	V _{CCB} (V)		T _A = 25 °C			-40 to 85 °C		-55 to 125 °C		
					Min.	Typ.	Max.	Min.	Max.	Min.		Max.
V _{OLPA}	Dynamic Low Level Quiet Output (note 1, 2)	3.3	5.5			1.0	1.5					V
		3.3	5.5		-1.2	-0.6						
V _{OLPB}	Dynamic Low Level Quiet Output (note 1, 2)	3.3	5.5			0.8	1.2					V
		3.3	5.5		-0.8	-0.5						
V _{IHDA}	Dynamic High Voltage Input (note 1, 3)	3.3	5.5				2					V
V _{ILDA}	Dynamic Low Voltage Input (note 1, 3)	3.3	5.5		0.8							V
V _{IHDB}	Dynamic High Voltage Input (note 1, 3)	3.3	5.5				2					V
V _{ILDB}	Dynamic Low Voltage Input (note 1, 3)	3.3	5.5		0.8							V

1) Worst case package

2) Max number of output defined as (n). Data inputs are driven 0V to 3.3V, (n-1) outputs switching and one output at GND

3) Max number of data inputs (n) switching. (n-1) switching 0V to 3.3V. Inputs under test switching: 3V to threshold (V_{ILD}). 0V to threshold (V_{IHD}) f = 1MHz

AC ELECTRICAL CHARACTERISTICS ($C_L = 50\text{pF}$, Input $t_r = t_f = 3\text{ns}$)

Symbol	Parameter	Test Condition		Value ⁽³⁾						Unit	
				$T_A = 25^\circ\text{C}$			$-40 \text{ to } 85^\circ\text{C}$		$-55 \text{ to } 125^\circ\text{C}$		
		V_{CCB} (V)		Min.	Typ.	Max.	Min.	Max.	Min.		Max.
t_{PLH}	Propagation Delay Time (An to Bn)	3.0(*)		1.0	5.5	8.5	1.0	9.0	1.0	9.5	ns
		5.0(**)		1.0	4.8	8.0	1.0	8.5	1.0	9.	
t_{PHL}	Propagation Delay Time (An to Bn)	3.0(*)		1.0	5.2	8.0	1.0	8.5	1.0	9.0	ns
		5.0(**)		1.0	3.9	6.5	1.0	7.0	1.0	7.5	
t_{PZL}	Output Enable Time (\bar{G} to Bn)	3.0(*)		1.0	6.0	9.0	1.0	9.5	1.0	9.5	ns
		5.0(**)		1.0	4.7	8.0	1.0	8.5	1.0	8.5	
t_{PZH}	Output Enable Time (\bar{G} to Bn)	3.0(*)		1.0	6.1	9.5	1.0	10.0	1.0	10.5	ns
		5.0(**)		1.0	4.8	8.5	1.0	9.0	1.0	9.5	
t_{PLZ}	Output Disable Time (\bar{G} to Bn)	3.0(*)		1.0	6.3	9.5	1.0	10.0	1.0	10.5	ns
		5.0(**)		1.0	4.0	8.0	1.0	8.5	1.0	8.5	
t_{PHZ}	Output Disable Time (\bar{G} to Bn)	3.0(*)		1.0	4.5	8.0	1.0	8.5	1.0	8.5	ns
		5.0(**)		1.0	3.8	7.5	1.0	8.0	1.0	8.5	
t_{PLH}	Propagation Delay Time (Bn to An)	3.0(*)		1.0	4.4	7.0	1.0	7.5	1.0	7.5	ns
		5.0(**)		1.0	3.8	6.5	1.0	7.0	1.0	7.5	
t_{PHL}	Propagation Delay Time (Bn to An)	3.0(*)		1.0	5.1	7.5	1.0	8.0	1.0	8.5	ns
		5.0(**)		1.0	4.3	7.5	1.0	8.0	1.0	8.5	
t_{PZL}	Output Enable Time (\bar{G} to An)	3.0(*)		1.0	6.4	10.0	1.0	10.5	1.0	10.5	ns
		5.0(**)		1.0	5.9	9.5	1.0	10.0	1.0	10.5	
t_{PZH}	Output Enable Time (\bar{G} to An)	3.0(*)		1.0	5.8	9.0	1.0	9.5	1.0	9.5	ns
		5.0(**)		1.0	5.4	9.0	1.0	9.5	1.0	9.5	
t_{PLZ}	Output Disable Time (\bar{G} to An)	3.0(*)		1.0	5.2	9.5	1.0	10.0	1.0	10.5	ns
		5.0(**)		1.0	4.6	9.5	1.0	10.0	1.0	10.5	
t_{PHZ}	Output Disable Time (\bar{G} to An)	3.0(*)		1.0	3.4	6.5	1.0	7.0	1.0	7.5	ns
		5.0(**)		1.0	3.1	6.5	1.0	7.0	1.0	7.5	
t_{OSLH} t_{OSHL}	Output To Output Skew Time (note 1, 2)	3.0(*)			0.5	1.0		1.5		1.5	ns
		5.0(**)			0.5	1.0		1.5		1.5	

1) Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs of the same device switching in the same direction, either HIGH or LOW ($t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$)

2) Parameter guaranteed by design

3) Typical values referred at $V_{CCA} = 3.3\text{V}$, $V_{CCB} = 5.0\text{V}$ or $V_{CCA} = 3.3\text{V}$, $V_{CCB} = 3.3\text{V}$

(*) Voltage Range is $3.0\text{V} \pm 0.3$

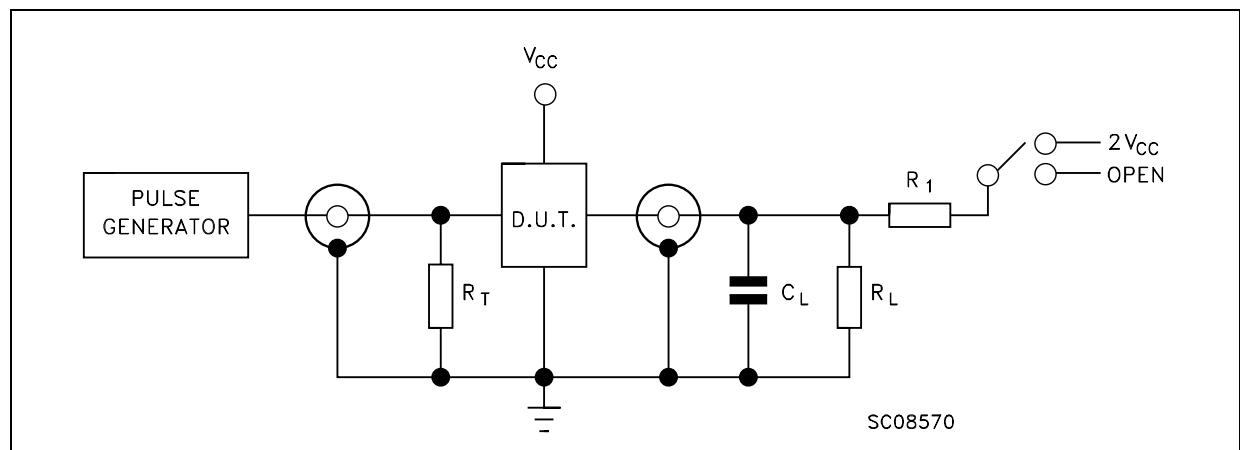
(**) Voltage Range is $5.0\text{V} \pm 0.5$

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Condition			Value						Unit	
		V _{CCA} (V)	V _{CCB} (V)		T _A = 25 °C			-40 to 85 °C		-55 to 125 °C		
					Min.	Typ.	Max.	Min.	Max.	Min.		Max.
C _{INA}	Input Capacitance	open	open			4.5	10		10		10	V
C _{I/O}	Input/Output Capacitance	3.3	5.0			10						V
C _{PD}	Dynamic Low Level Quiet Output (note 1) A to B	3.3	5.0			55						V
C _{PD}	Dynamic Low Level Quiet Output (note 1) B to A	3.3	5.0			40						V

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/8$ (per circuit)

TEST CIRCUIT

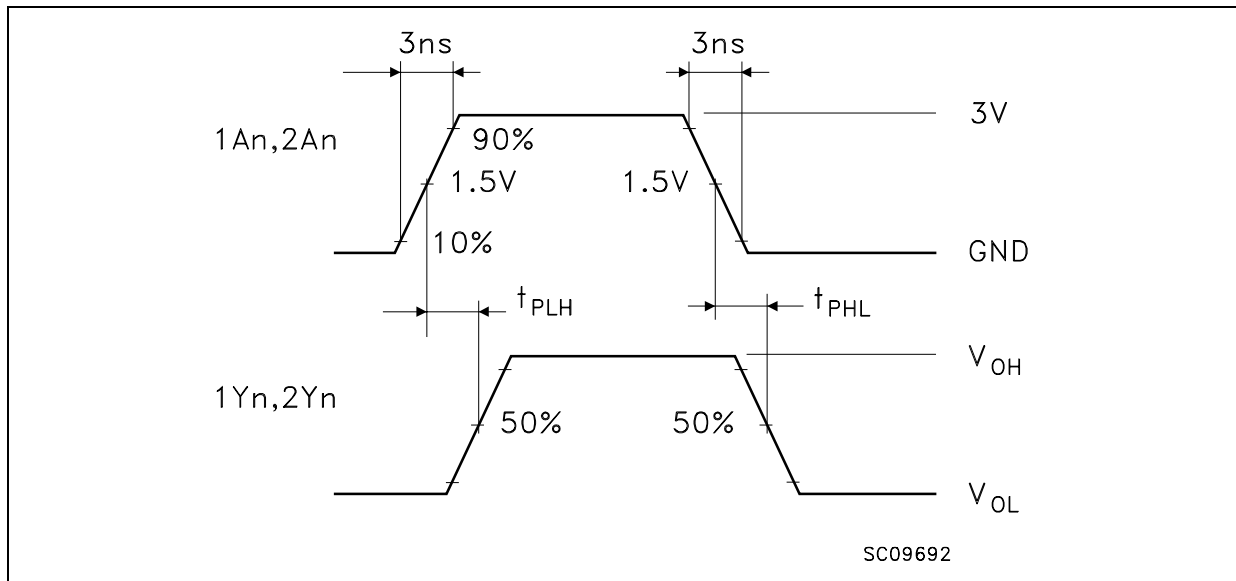
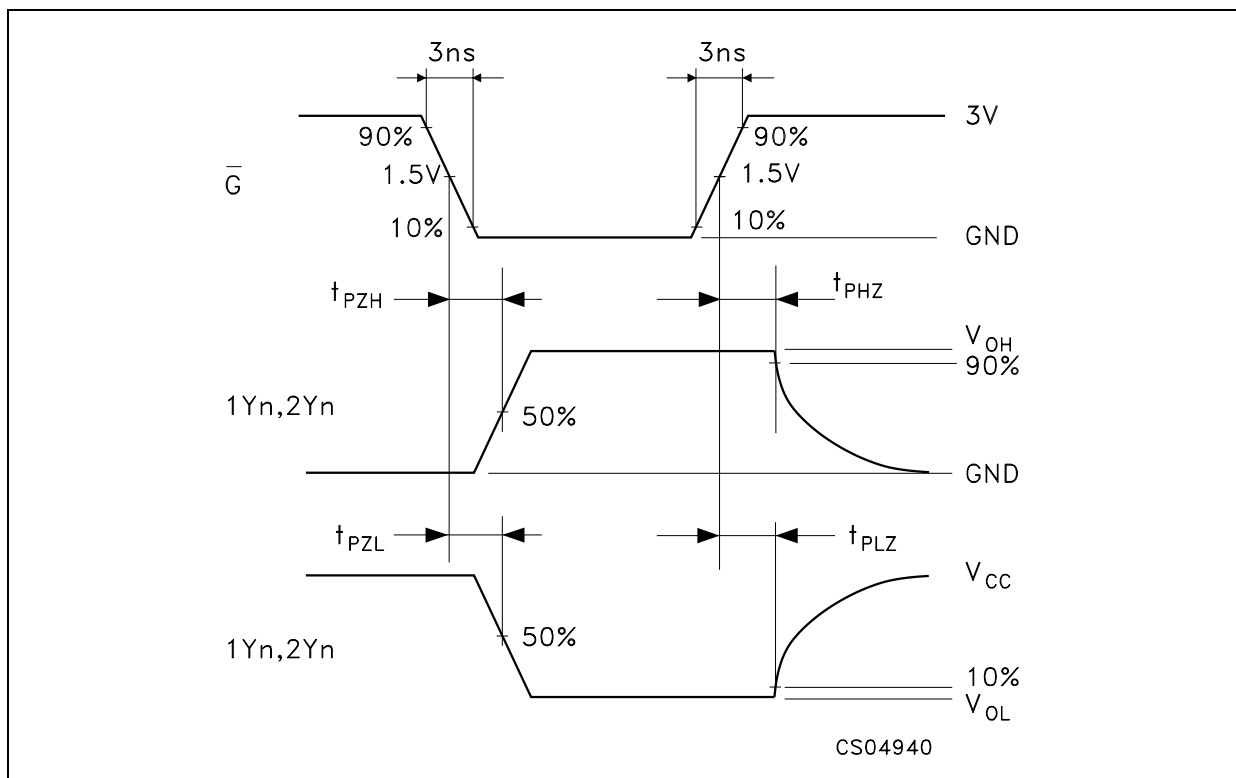


TEST	SWITCH
t _{PLH} , t _{PHL}	Open
t _{PZLH} , t _{PLZ}	2V _{CC}
t _{PZH} , t _{PHZ}	Open

C_L = 50pF or equivalent (includes jig and probe capacitance)

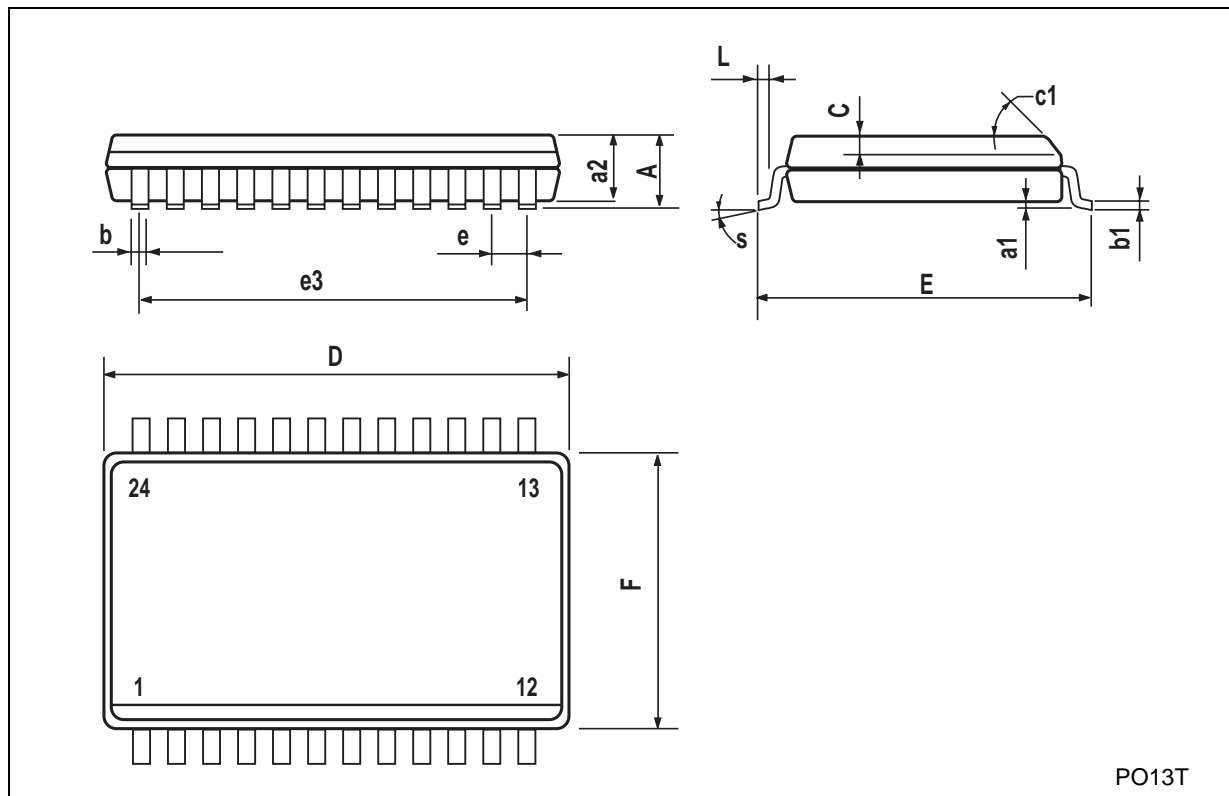
R_L = R₁ = 500Ω or equivalent

R_T = Z_{OUT} of pulse generator (typically 50Ω)

WAVEFORM 1: PROPAGATION DELAYS ($f=1\text{MHz}$; 50% duty cycle)**WAVEFORM 2: OUTPUT ENABLE AND DISABLE TIME** ($f=1\text{MHz}$; 50% duty cycle)

SO-24 MECHANICAL DATA

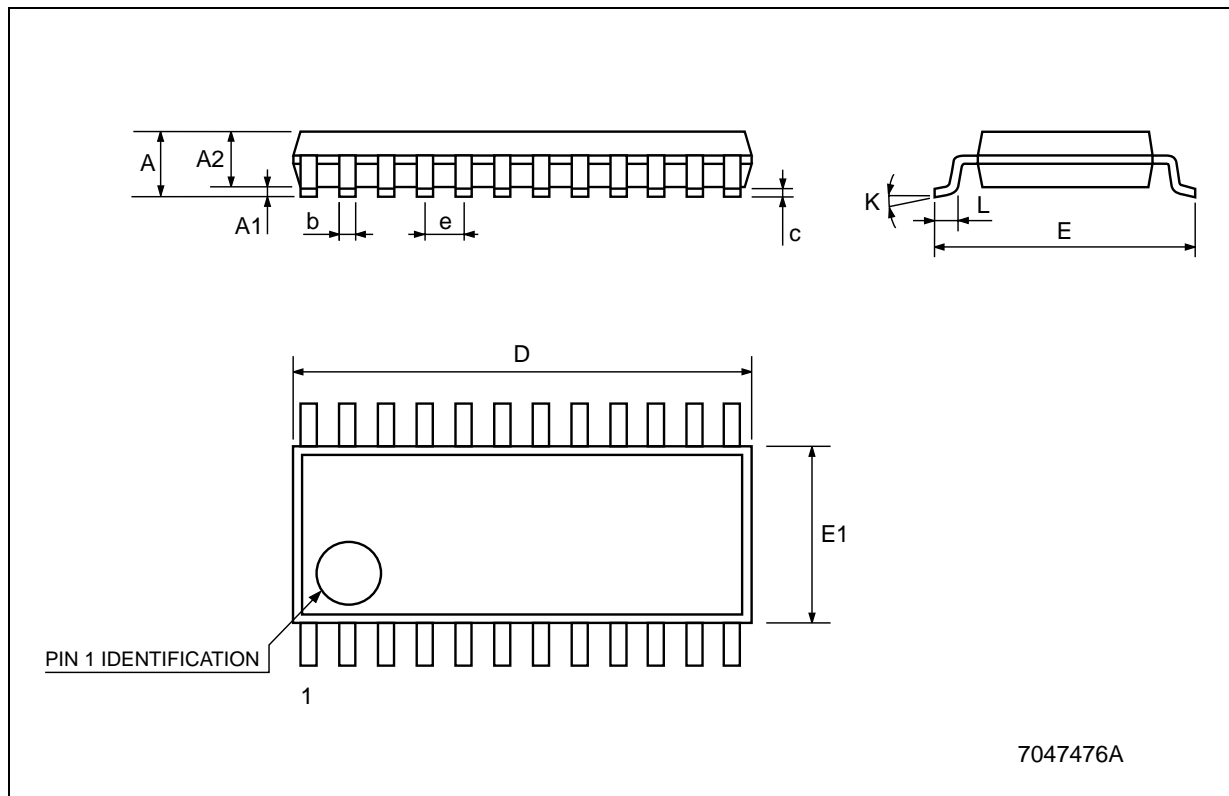
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.2	0.004		0.008
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.012
C		0.5			0.020	
c1	45° (typ.)					
D	15.20		15.60	0.598		0.614
E	10.00		10.65	0.393		0.419
e		1.27			0.050	
e3		13.97			0.550	
F	7.40		7.60	0.291		0.300
L	0.50		1.27	0.020		0.050
S	8° (max.)					



PO13T

TSSOP24 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.1			0.043
A1	0.05		0.15	0.002		0.006
A2		0.9			0.035	
b	0.19		0.30	0.0075		0.0118
c	0.09		0.20	0.0035		0.0079
D	7.7		7.9	0.303		0.311
E	6.25		6.5	0.246		0.256
E1	4.3		4.5	0.169		0.177
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.50		0.70	0.020		0.028



Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

© The ST logo is a registered trademark of STMicroelectronics

© 2001 STMicroelectronics - Printed in Italy - All Rights Reserved
STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - China - Finland - France - Germany - Hong Kong - India - Italy - Japan - Malaysia - Malta - Morocco
Singapore - Spain - Sweden - Switzerland - United Kingdom

© <http://www.st.com>