National Semiconductor

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74VHC112
Dual J-K Flip-Flops with Preset and Clear

General Description

The 'VHC112 is an advanced high speed CMOS device fabricated with silicon gate CMOS technology. It achieves the high-speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

The VHC112 contains two independent, high-speed JK flip-flops with Direct Set and Clear inputs. Synchronous state changes are initiated by the falling edge of the clock. Triggering occurs at a voltage level of the clock and is not directly related to transition time. The J and K inputs can change when the clock is in either state without affecting the flip-flop, provided that they are in the desired state during the recommended setup and hold times relative to the falling edge of the clock. The LOW signal on PR or CLR prevents clocking and forces Q and $\overline{Q}$ HIGH, respectively. Simultaneous LOW signals on PR and CLR force both Q and $\overline{Q}$ HIGH.

An input protection circuit ensures that 0V to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery backup. This circuit prevents device destruction due to mismatched supply and input voltages.

Features

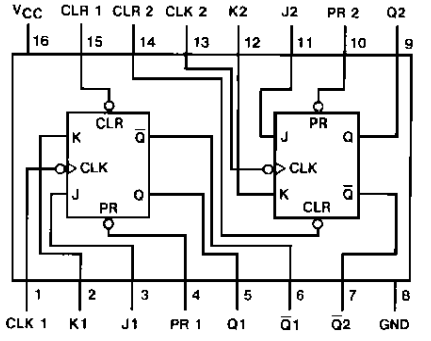
- High noise immunity
- Power down protection
- Low power dissipation
- Low noise
- Balanced propagation delays
- Pin and function compatible with 74HC112

Commercial	Package Number	Package Description
74VHC112M	M16A	16-Lead Molded JEDEC SOIC
74VHC112SJ	M16D	16-Lead Molded EIAJ SOIC
74VHC112MTC	MTC16	16-Lead Molded JEDEC Type 1 TSSOP
74VHC112N	N16E	16-Lead Molded DIP

Note: Surface mount packages are also available on Tape and Reel. Specifiy by appending the suffix letter "X" to the ordering code.

Connection Diagram

Pin Assignment for DIP, SOIC and TSSOP



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Pin Names	Description
J_1, J_2, K_1, K_2	Data Inputs
CLK_1, CLK_2	Clock Pulse Inputs (Active Falling edge)
CLR_1, CLR_2	Direct Clear Inputs (Active Low)
PR_1, PR_2	Direct Preset Inputs (Active Low)
Q_1, Q_2, $\overline{Q}_1$, $\overline{Q}_2$	

Truth Table

Inputs					Outputs	
PR	CLR	$\overline{CP}$	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H	H
H	H	⌐	h	h	$\overline{Q}_0$	Q_0
H	H	⌐	l	h	L	H
H	H	⌐	h	l	H	L
H	H	⌐	l	l	Q_0	$\overline{Q}_0$

H (h) = HIGH Voltage Level

L (l) = LOW Voltage Level

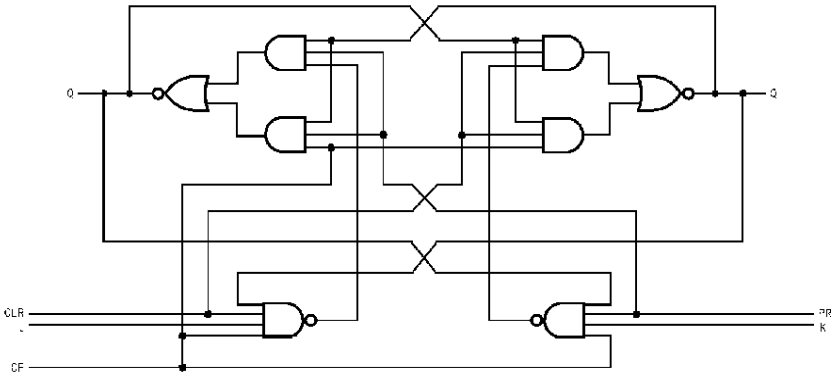
X = Immaterial

⌐ = HIGH-to-LOW Clock Transition

Q_0 ($\overline{Q}_0$ = Before HIGH-to-LOW Transition of Clock

Lower case letters indicate the state of the referenced input or output one setup time prior to the HIGH-to-LOW clock transition.

Logic Diagram (One Half Shown)



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Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−0.5V to +7.0V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC} + 0.5V
Input Diode Current (I_{IK})	−20 mA
Output Diode Current (I_{OK})	±20 mA
DC Output Current (I_{OUT})	±25 mA
DC V_{CC}/GND Current (I_{CC})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

Note 1: *Absolute Maximum Ratings are values beyond which the device may be damaged or have its useful life impaired. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation outside databook specifications.*

Recommended Operating Conditions

Supply Voltage (V_{CC})	2.0V to +5.5V
Input Voltage (V_{IN})	0V to +5.5V
Output Voltage (V_{OUT})	0V to V_{CC}
Operating Temperature (T_{OPR})	−40°C to +85°C
Input Rise and Fall Time (t_r, t_f)	
V_{CC} = 3.3V ±0.3V	0 ~ 100 ns/V
V_{CC} = 5.0V ±0.5V	0 ~ 20 ns/V

DC Characteristics for 'VHC Family Devices

Symbol	Parameter	V_{CC} (V)	74VHC					Units	Conditions	
			T_A = 25°C			T_A = −40°C to +85°C				
			Min	Typ	Max	Min	Max			
V_{IH}	High Level Input Voltage	2.0 3.0–5.5	1.50 0.7 V_{CC}			1.50 0.7 V_{CC}		V		
V_{IL}	Low Level Input Voltage	2.0 3.0–5.5			0.50 0.3 V_{CC}		0.50 0.3 V_{CC}	V		
V_{OH}	High Level Output Voltage	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		V	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50 μA
		3.0 4.5	2.58 3.94			2.48 3.80		V		I_{OH} = −4 mA I_{OH} = −8 mA
V_{OL}	Low Level Output Voltage	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1	V	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA
		3.0 4.5			0.36 0.36		0.44 0.44	V		I_{OL} = 4 mA I_{OL} = 8 mA
I_{IN}	Input Leakage Current	0–5.5			±0.1		±1.0	μA	V_{IN} = 5.5V or GND	
I_{CC}	Quiescent Supply Current	5.5			2.0		20.0	μA	V_{IN} = V_{CC} or GND	

AC Electrical Characteristics for VHC:

Symbol	Parameter	V_{CC} (V)	74VHC $T_A = 25°C$			74VHC $T_A = -40°C$ to $+85°C$		Units	Conditions
			Min	Typ	Max	Min	Max		
f_{MAX}	Maximum Clock Frequency	3.3 ± 0.3	110	150		100		MHz	$C_L = 15$ pF
			90	120		80			$C_L = 50$ pF
		5.0 ± 0.5	150	200		135		MHz	$C_L = 15$ pF
			120	185		110			$C_L = 50$ pF
t_{PLH}, t_{PHL}	Propagation Delay Time (CP to Q_n or $\overline{Q}_n$)	3.3 ± 0.3		8.5	11.0	1.0	13.4	ns	$C_L = 15$ pF
				10.0	15.0	1.0	16.5		$C_L = 50$ pF
		5.0 ± 0.5		5.1	7.3	1.0	8.8	ns	$C_L = 15$ pF
				6.3	10.5	1.0	12.0		$C_L = 50$ pF
t_{PLH}, t_{PHL}	Propagation Delay Time (PR or CLR to Q_n or $\overline{Q}_n$)	3.3 ± 0.3		6.7	10.2	1.0	11.7	ns	$C_L = 15$ pF
				9.7	13.5	1.0	15.0		$C_L = 50$ pF
		5.0 ± 0.5		4.6	6.7	1.0	8.0	ns	$C_L = 15$ pF
				6.4	9.5	1.0	11.0		$C_L = 50$ pF
C_{IN}	Input Capacitance			4	10		10	pF	V_{CC} = Open
C_{PD}	Power Dissipation Capacitance			18				pF	(Note 1)

Note 1: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained from the equation: I_{CC} (opr.) = C_{PD} * V_{CC} * f_{IN} + I_{CC}/4 (per F/F), and the total C_{PD} when n pcs of the Flip Flop operate can be calculated by the following equation: C_{PD} (total) = 30 + 14 • n

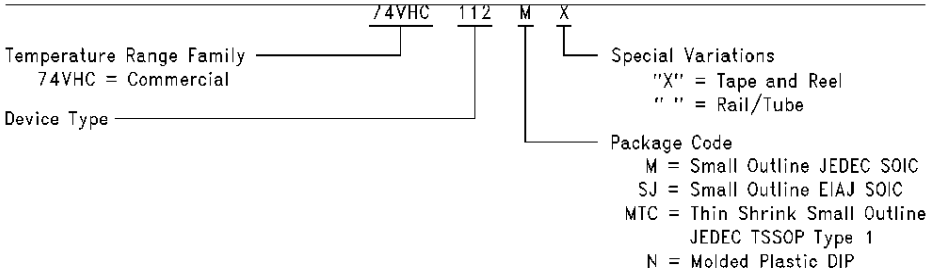
AC Operating Requirements for VHC:

Symbol	Parameter	*V_{CC} (V)	74VHC		74VHC	Units	Conditions
			$T_A = 25°C$		$T_A = -40°C$ to $+85°C$		
			Typ	Guaranteed Minimum			
t_W	Minimum Pulse Width (CP or CLR or PR)	3.3 5.0		5.0 5.0	5.0 5.0	ns	
t_S	Minimum Setup Time (J_n or K_n to CP_n)	3.3 5.0		5.0 4.0	5.0 4.0	ns	
t_H	Minimum Hold Time (J_n or K_n to CP_n)	3.3 5.0		1.0 1.0	1.0 1.0	ns	
t_{rec}	Minimum Recovery Time (CLR or PR to CP)	3.3 5.0		6.0 5.0	6.0 5.0	ns	

*V_{CC} is 3.3 ±0.3V or 5.0 ±0.5V

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



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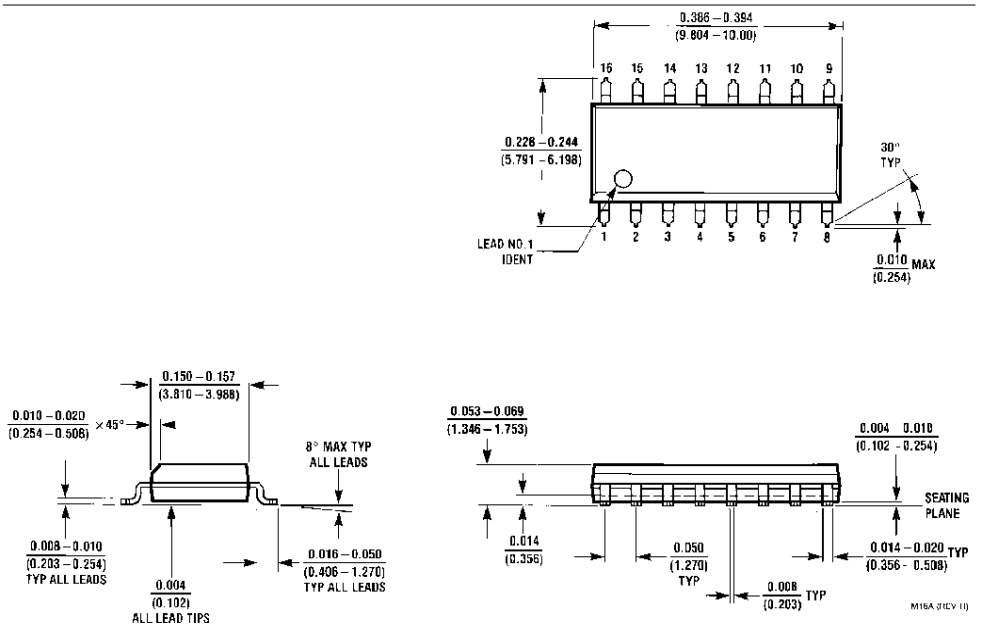
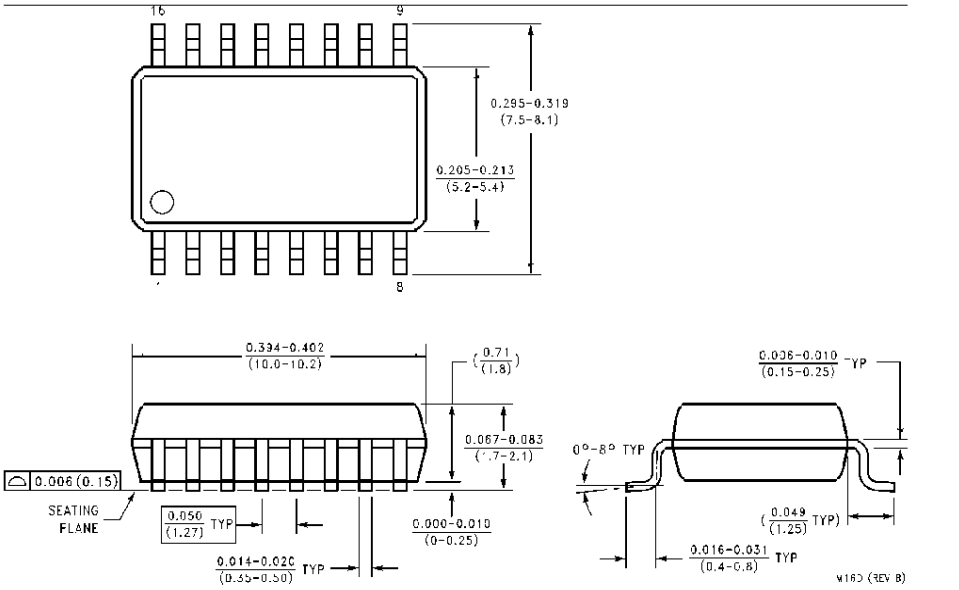
Physical Dimensions inches (millimeters) unless otherwise noted

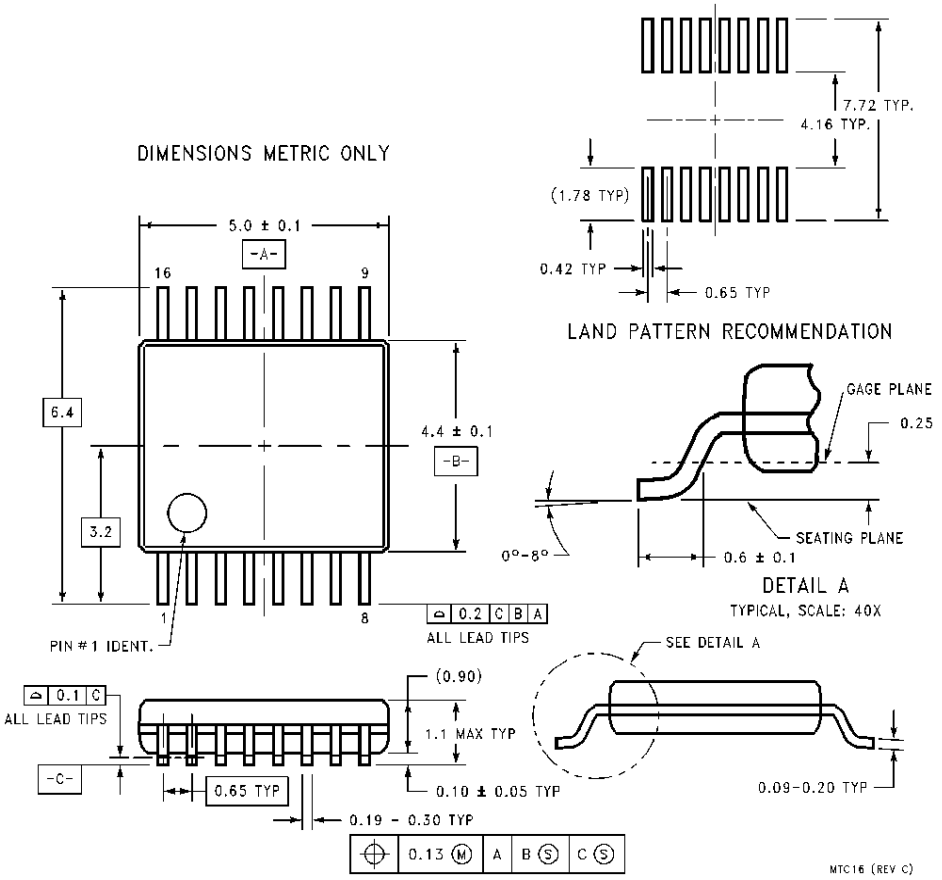


16-Lead Molded JEDEC SOIC
NS Package Number M16A



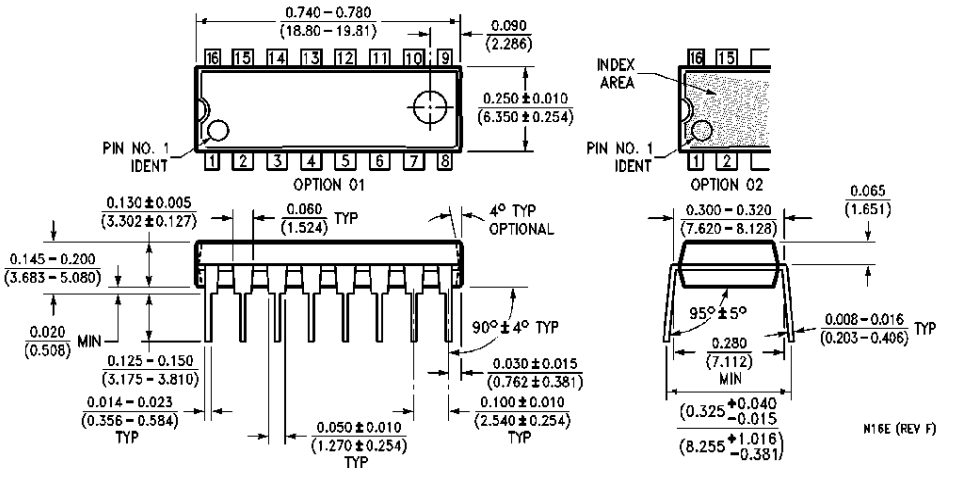
16-Lead Molded EIAJ SOIC
NS Package Number M16D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Molded JEDEC Type 1 TSSOP
NS Package Number MTC16

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead (0.300″) Molded Dual-In-Line Package
NS Package Number N16E

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