

74VHC139 Dual 2-to-4 Decoder/Demultiplexer

General Description

The VHC139 is an advanced high speed CMOS 2 to 4 line decoder/demultiplexer fabricated with silicon gate CMOS technology. It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

The active low enable input can be used for gating or it can be used as a data input for demultiplexing applications. When the enable input is held High, all four outputs are fixed at a high logic level independent of the other inputs. An input protection circuit ensures that 0V to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

Features

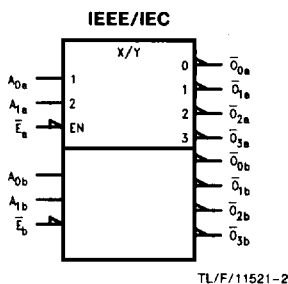
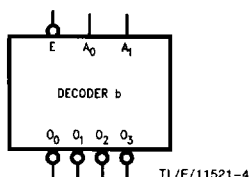
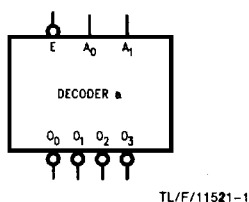
- Low power dissipation:
 $I_{CC} = 4 \mu A$ (Max.) at $T_A = 25^\circ C$
- High noise immunity: $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (Min.)
- All inputs are equipped with a power down protection function
- Balanced propagation delays: $t_{PLH} \approx t_{PHL}$
- Pin and function compatible with 74HC139

Ordering Code: See Section 6

Commercial	Package Number	Package Description
74VHC139M	M16A	16-Lead Molded JEDEC SOIC
74VHC139SJ	M16D	16-Lead Molded EIAJ SOIC
74VHC139MSC	MSC16	16-Lead Molded EIAJ Type 1 SSOP
74VHC139MTC	MTC16	16-Lead Molded JEDEC Type 1 TSSOP
74VHC139N	N16E	16-Lead Molded DIP

Note: Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.
EIAJ Type 1 SSOP available on Tape and Reel only, order MSCX.

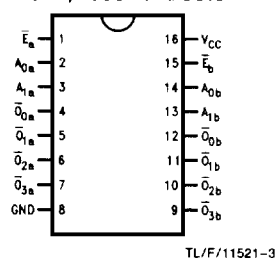
Logic Symbols



Pin Names	Description
A_0, A_1	Address Inputs
\bar{E}	Enable Inputs
$\bar{O}_0 - \bar{O}_3$	Outputs

Connection Diagrams

Pin Assignment for DIP, SSOP, TSSOP and SOIC



Functional Description

The 'VHC139 is a high-speed dual 2-to-4 decoder/demultiplexer. The device has two independent decoders, each of which accepts two binary weighted inputs (A_0 – A_1) and provides four mutually exclusive active-LOW outputs (\bar{O}_0 – \bar{O}_3). Each decoder has an active-LOW enable (\bar{E}). When \bar{E} is HIGH all outputs are forced HIGH. The enable can be used as the data input for a 4-output demultiplexer application. Each half of the 'VHC139 generates all four minterms of two variables. These four minterms are useful in some applications, replacing multiple gate functions as shown in *Figure 1*, and thereby reducing the number of packages required in a logic network.

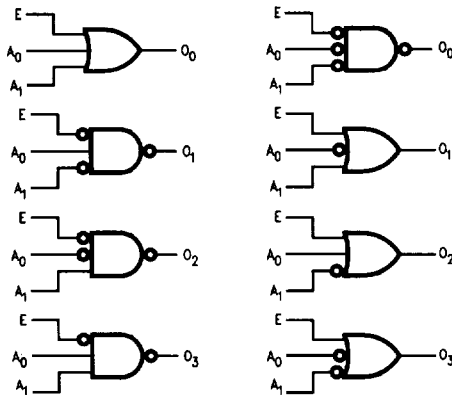
Truth Table

Inputs			Outputs			
\bar{E}	A_0	A_1	\bar{O}_0	\bar{O}_1	\bar{O}_2	\bar{O}_3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

H = HIGH Voltage Level

L = LOW Voltage Level

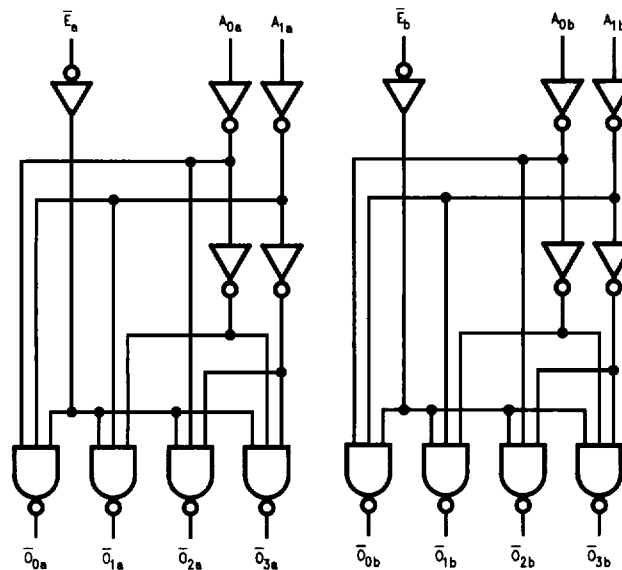
X = Immaterial



TL/F/11521-8

FIGURE 1. Gate Functions (Each Half)

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC})	-0.5V to +7.0V
DC Input Voltage (V_{IN})	-0.5V to +7.0V
DC Output Voltage (V_{OUT})	-0.5V to V_{CC} + 0.5V
Input Diode Current (I_{IK})	-20 mA
Output Diode Current (I_{OK})	±20 mA
DC Output Current (I_{OUT})	±25 mA
DC V_{CC} /GND Current (I_{CC})	±75 mA
Storage Temperature (T_{STG})	-65°C to +150°C
Lead Temperature (T_L) (Soldering, 10 sec.)	260°C

Note 1: *Absolute Maximum Ratings are values beyond which the device may be damaged or have its useful life impaired. The databook specifications should be met, without exception, to ensure that the the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation outside databook specifications.*

Recommended Operating Conditions

Supply Voltage (V_{CC})	2.0V to +5.5V
Input Voltage (V_{IN})	0V to +5.5V
Output Voltage (V_{OUT})	0V to V_{CC}
Operating Temperature (T_{OPR}) 74VHC	-40°C to +85°C
Input Rise and Fall Time (t_r, t_f) $V_{CC} = 3.3V \pm 0.3V$ $V_{CC} = 5.0V \pm 0.5V$	0 ~ 100 ns/V 0 ~ 20 ns/V

DC Characteristics for 'VHC Family Devices

Symbol	Parameter	V _{CC} (V)	74VHC			74VHC		Units	Conditions	
			T _A = 25°C			T _A = −40°C to +85°C				
			Min	Typ	Max	Min	Max			
V _{IH}	High Level Input Voltage	2.0 3.0–5.5	1.50 0.7 V _{CC}			1.50 0.7 V _{CC}		V		
V _{IL}	Low Level Input Voltage	2.0 3.0–5.5	0.50 0.3 V _{CC}			0.50 0.3 V _{CC}		V		
V _{OH}	High Level Output Voltage	2.0	1.9	2.0		1.9		V	V _{IN} = V _{IH} or V _{IL}	I _{OH} = −50 μA
		3.0	2.9	3.0		2.9				
		4.5	4.4	4.5		4.4				
		3.0 4.5	2.58 3.94			2.48 3.80		V		I _{OH} = −4 mA I _{OH} = −8 mA
V _{OL}	Low Level Output Voltage	2.0		0.0	0.1		0.1	V	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 50 μA
		3.0		0.0	0.1		0.1			
		4.5		0.0	0.1		0.1			
		3.0 4.5			0.36 0.36		0.44 0.44	V		I _{OL} = 4 mA I _{OL} = 8 mA
I _{IN}	Input Leakage Current	0–5.5	±0.1			±1.0		μA	V _{IN} = 5.5V or GND	
I _{CC}	Quiescent Supply Current	5.5	4.0			40.0		μA	V _{IN} = V _{CC} or GND	

AC Electrical Characteristics: See Section 2 for waveforms

Symbol	Parameter	V _{CC} (V)	74VHC			74VHC		Units	Conditions	Fig. No.
			T _A = 25°C			T _A = −40°C to +85°C				
			Min	Typ	Max	Min	Max			
t _{PLH} , t _{PHL}	Propagation Delay A _n to \overline{O}_n	3.3 ± 0.3	7.2	11.0	1.0	13.0	ns	C _L = 15 pF	2-5	
			9.7	14.5	1.0	16.5		C _L = 50 pF		
		5.0 ± 0.5	5.0	7.2	1.0	8.5	ns	C _L = 15 pF		
			6.5	9.2	1.0	10.5		C _L = 50 pF		
t _{PLH} , t _{PHL}	Propagation Delay \overline{E}_n to \overline{O}_n	3.3 ± 0.3	6.4	9.2	1.0	11.0	ns	C _L = 15 pF	2-6	
			8.9	12.7	1.0	14.5		C _L = 50 pF		
		5.0 ± 0.5	4.4	6.3	1.0	7.5	ns	C _L = 15 pF		
			5.9	8.3	1.0	9.5		C _L = 50 pF		
C _{IN}	Input Capacitance		4	10	10	pF	V _{CC} = Open			
C _{PD}	Power Dissipation Capacitance		26			pF	(Note 1)			

Note 1: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC} (opr.) = C_{PD} * V_{CC} * f_{IN} + I_{CC}/2 (per decoder).