LC²MOS Dual 12-Bit DACs

AD7537/AD7547

FEATURES
- Two 12-Bit DACs in One Package
- DAC Ladder Resistance Matching: 0.5%
- Space Saving Skinny DIP and Surface Mount Packages
- 4-Quadrant Multiplication
- Low Gain Error (1LSB max Over Temperature)
- Byte Loading Structure
- Fast Interface Timing

APPLICATIONS
- Automatic Test Equipment
- Programmable Filters
- Audio Applications
- Synchro Applications
- Process Control

GENERAL DESCRIPTION

The AD7537/AD7547 contains two 12-bit current output DACs on one monolithic chip. Also on-chip are the level shifters, data registers and control logic for easy microprocessor interfacing. There are 12 data inputs. The AD7537 has a 2-byte loading structure making it compatible with 8-bit processor systems. The AD7547 has a 12-bit parallel loading structure for use in 16-bit systems.

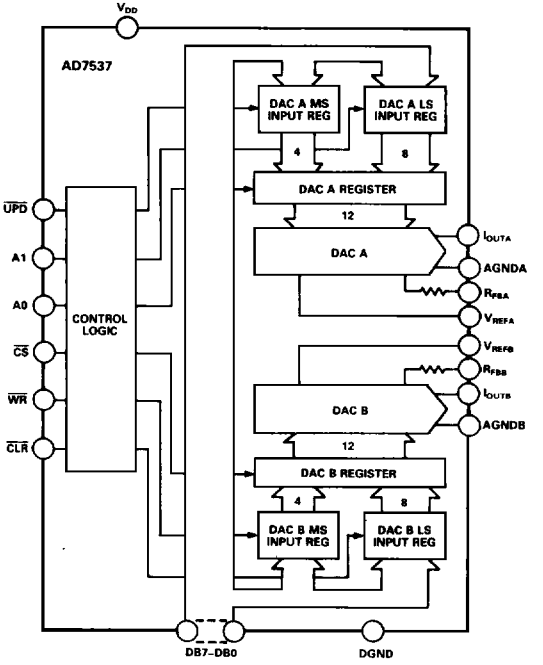
The D/A converters provide 4-quadrant multiplication capabilities with separate reference inputs and feedback resistors. Monolithic construction ensures that thermal and gain error tracking is excellent. Twelve-bit monotonicity is guaranteed for both DACs over the full temperature range.

The DACs are manufactured using the Linear Compatible CMOS (LC²MOS) process. This allows fast digital logic and precision linear circuitry to be fabricated on the same die.

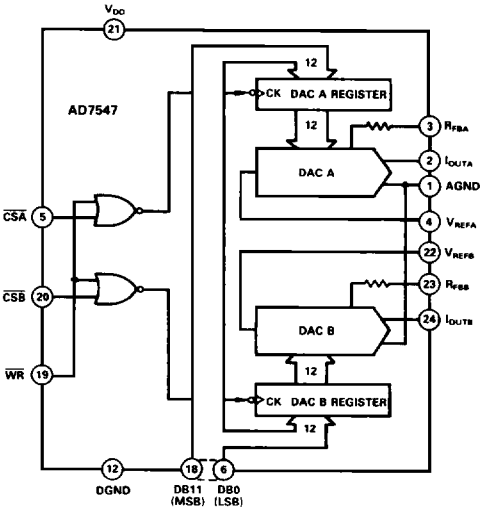
PRODUCT HIGHLIGHTS

1. DAC to DAC Matching
   Since both DACs are fabricated on the same chip, precise matching and tracking is inherent. Many applications which are not practical using two discrete DACs are now possible. Typical matching: 0.5%.
2. Wide Power Supply Tolerance
   The device operates on a +12V to +15V V_{DD}, with ±10% tolerance on this nominal figure. All specifications are guaranteed over this range.

AD7537 FUNCTIONAL BLOCK DIAGRAM



AD7547 FUNCTIONAL BLOCK DIAGRAM



This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD7537/AD7547—SPECIFICATIONS[1]

(V_{DD} = +12V to +15V, ±10%, V_{REFA} = V_{REFB} = 10V; I_{OUTA} = I_{OUTB} = AGND = 0V. All specifications T_{min} to T_{max} unless otherwise noted.)

Parameter	J, A Versions	K, B Versions	L, C Versions	S Version	T Version	U Version	Units	Test Conditions/Comments
ACCURACY								
Resolution	12	12	12	12	12	12	Bits	
Relative Accuracy	±1	±1/2	±1/2	±1	±1/2	±1/2	LSB max	
Differential Nonlinearity	±1	±1	±1	±1	±1	±1	LSB max	All grades guaranteed monotonic over temperature.
Gain Error	±6	±3	±1	±6	±3	±2	LSB max	Measured using R_{FBA}, R_{FBB}. Both DAC registers loaded with all 1's.
Gain Temperature Coefficient[2]; ΔGain/ΔTemperature	±5	±5	±5	±5	±5	±5	ppm/°C max	Typical value is 1ppm/°C
Output Leakage Current								
I_{OUTA}								
+25°C	10	10	10	10	10	10	nA max	DAC A Register loaded
T_{min} to T_{max}	150	150	150	250	250	250	nA max	with all 0's.
I_{OUTB}								
+25°C	10	10	10	10	10	10	nA max	DAC B Register loaded
T_{min} to T_{max}	150	150	150	250	250	250	nA max	with all 0's.
REFERENCE INPUT								
Input Resistance	9	9	9	9	9	9	kΩ min	Typical Input Resistance = 14kΩ
	20	20	20	20	20	20	kΩ max	
V_{REFA}, V_{REFB} Input Resistance Match	±3	±3	±1	±3	±3	±1	% max	Typically ±0.5%
DIGITAL INPUTS								
V_{IH} (Input High Voltage)	2.4	2.4	2.4	2.4	2.4	2.4	V min	
V_{IL} (Input Low Voltage)	0.8	0.8	0.8	0.8	0.8	0.8	V max	
I_{IN} (Input Current)								
+25°C	±1	±1	±1	±1	±1	±1	μA max	V_{IN} = V_{DD}
T_{min} to T_{max}	±10	±10	±10	±10	±10	±10	μA max	
C_{IN} (Input Capacitance)[2]	10	10	10	10	10	10	pF max	
POWER SUPPLY[3]								
V_{DD}	10.8/16.5	10.8/16.5	10.8/16.5	10.8/16.5	10.8/16.5	10.8/16.5	V min/V max	
I_{DD}	2	2	2	2	2	2	mA max	

AC PERFORMANCE CHARACTERISTICS

These characteristics are included for Design Guidance only and are not subject to test.

(V_{DD} = +12V to +15V; V_{REFA} = V_{REFB} = +10V, I_{OUTA} = I_{OUTB} = AGND = 0V. Output Amplifiers are AD644 except where stated.)

Parameter	T_A = +25°C	T_A = T_{min}, T_{max}	Units	Test Conditions/Comments
Output Current Settling Time	1.5	–	μs max	To 0.01% of full-scale range. I_{OUT} load = 100Ω, C_{EXT} = 13pF. DAC output measured from rising edge of $\overline{WR}$. Typical Value of Settling Time is 0.8μs.
Digital-to-Analog Glitch Impulse	7	–	nV-s typ	Measured with V_{REFA} = V_{REFB} = 0V. I_{OUTA}, I_{OUTB} load = 100Ω, C_{EXT} = 13pF. DAC registers alternately loaded with all 0's and all 1's.
AC Feedthrough[4]				
V_{REFA} to I_{OUTA}	−70	−65	dB max	V_{REFA}, V_{REFB} = 20Vp-p 10kHz sinewave. DAC
V_{REFB} to I_{OUTB}	−70	−65	dB max	registers loaded with all 0's.
Power Supply Rejection ΔGain/ΔV_{DD}	±0.01	±0.02	% per % max	ΔV_{DD} = V_{DD} max − V_{DD} min
Output Capacitance				
C_{OUTA}	70	70	pF max	DAC A, DAC B loaded with all 0's.
C_{OUTB}	70	70	pF max	
C_{OUTA}	140	140	pF max	DAC A, DAC B loaded with all 1's.
C_{OUTB}	140	140	pF max	
Channel-to-Channel Isolation				
V_{REFA} to I_{OUTB}	−84	–	dB typ	V_{REFA} = 20V p-p 10kHz sinewave, V_{REFB} = 0V. Both DACs loaded with all 1's.
V_{REFB} to I_{OUTA}	−84	–	dB typ	V_{REFB} = 20V p-p 10kHz sinewave, V_{REFA} = 0V. Both DACs loaded with all 1's.
Digital Crosstalk	7	–	nV-s typ	Measured for a Code Transition of all 0's to all 1's. I_{OUTA}, I_{OUTB} Load = 100Ω, C_{EXT} = 13pF
Output Noise Voltage Density (10Hz-100kHz)	25	–	nV/√Hz typ	Measured between R_{FBA} and I_{OUTA} or R_{FBB} and I_{OUTB}. Frequency of measurement is 10Hz–100kHz.
Total Harmonic Distortion	−82	–	dB typ	V_{IN} = 6V rms, 1kHz. Both DACs loaded with all 1's.

NOTES

[1]Temperature range as follows: J, K, L Versions: −40°C to +85°C.
A, B, C Versions: −40°C to +85°C.
S, T, U Versions: −55°C to +125°C.

[2]Sample tested at 25°C to ensure compliance.

[3]Functional at V_{DD} = 5V with degraded specifications.

[4]Pin 12 (DGND) on ceramic DIPs is connected to lid.

Specifications subject to change without notice.

AD7537 TIMING CHARACTERISTICS (V_{DD} = 10.8V to 16.5V, $V_{REFA} = V_{REFB}$ = +10V, I_{OUTA} = AGNDA = 0V, I_{OUTB} = AGNDB = 0V).

Parameter	Limit at T_A = +25°C	Limit at T_A = −40°C to +85°C	Limit at T_A = +55°C to +125°C	Units	Test Conditions/Comments
t_1	15	15	30	ns min	Address Valid to Write Setup Time
t_2	15	15	25	ns min	Address Valid to Write Hold Time
t_3	60	80	80	ns min	Data Setup Time
t_4	25	25	25	ns min	Data Hold Time
t_5	0	0	0	ns min	Chip Select or Update to Write Setup Time
t_6	0	0	0	ns min	Chip Select or Update to Write Hold Time
t_7	80	80	100	ns min	Write Pulse Width
t_8	80	80	100	ns min	Clear Pulse Width

Specifications subject to change without notice.

3

Table I. AD7537 Truth Table

$\overline{CSA}$	$\overline{CSB}$	$\overline{WR}$	FUNCTION
X	X	1	No Data Transfer
1	1	X	No Data Transfer
↓	↓	0	A Rising Edge on $\overline{CSA}$ or $\overline{CSB}$ Loads Data to the Respective DAC from the Data Bus
0	1	↓	DAC A Register Loaded from Data Bus
1	0	↓	DAC B Register Loaded from Data Bus
0	0	↓	DAC A and DAC B Registers Loaded from Data Bus

NOTES
1. X = Don't care
2. ↓ means rising edge triggered

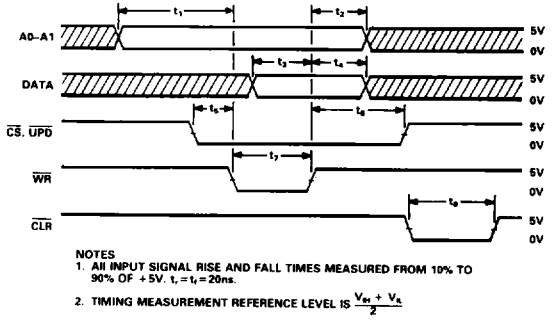


Figure 1. Timing Diagram for AD7537

AD7537 ORDERING GUIDE[1]

Model[2]	Temperature Range	Relative Accuracy	Gain Error	Package Option[3]
AD7537JN	−40°C to +85°C	±1LSB	±6LSB	N-24
AD7537KN	−40°C to +85°C	±1/2LSB	±3LSB	N-24
AD7537LN	−40°C to +85°C	±1/2LSB	±1LSB	N-24
AD7537JP	−40°C to +85°C	±1LSB	±6LSB	P-28A
AD7537KP	−40°C to +85°C	±1/2LSB	±3LSB	P-28A
AD7537LP	−40°C to +85°C	±1/2LSB	±1LSB	P-28A
AD7537AQ	−40°C to +85°C	±1LSB	±6LSB	Q-24
AD7537BQ	−40°C to +85°C	±1/2LSB	±3LSB	Q-24
AD7537CQ	−40°C to +85°C	±1/2LSB	±1LSB	Q-24
AD7537SQ	−55°C to +125°C	±1LSB	±6LSB	Q-24
AD7537TQ	−55°C to +125°C	±1/2LSB	±3LSB	Q-24
AD7537UQ	−55°C to +125°C	±1/2LSB	±2LSB	Q-24
AD7537SE	−55°C to +125°C	±1LSB	±6LSB	E-28A
AD7537TE	−55°C to +125°C	±1/2LSB	±3LSB	E-28A
AD7537UE	−55°C to +125°C	±1/2LSB	±2LSB	E-28A

NOTES
[1]Analog Devices reserves the right to ship ceramic packages (D-24A) in lieu of cerdip packages (Q-24).
[2]To order MIL-STD-883, Class B processed parts, add/883B to part number. Contact your local sales office for military data sheet.
[3]E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip. For outline information see Package Information section.

AD7547 TIMING CHARACTERISTICS (V_{DD} = 10.8V to 16.5V, $V_{REFA} = V_{REFB}$ = +10V, I_{OUTA} = AGNDA = 0V).

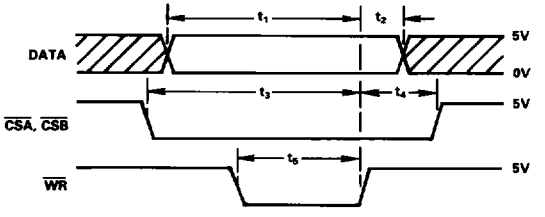
Parameter	Limit at T_A = +25°C	Limit at T_A = −40°C to +85°C	Limit at T_A = −55°C to +125°C	Units	Test Conditions/Comments
t_1	60	80	80	ns min	Data Setup Time
t_2	25	25	25	ns min	Data Hold Time
t_3	80	80	100	ns min	Chip Select to Write Setup Time
t_4	0	0	0	ns min	Chip Select to Write Hold Time
t_5	80	80	100	ns min	Write Pulse Width

Specifications subject to change without notice.

Table II. AD7547 Truth Table

$\overline{CLR}$	$\overline{UPD}$	$\overline{CS}$	$\overline{WR}$	A1	A0	FUNCTION
1	1	1	X	X	X	No Data Transfer
1	1	X	1	X	X	No Data Transfer
0	X	X	X	X	X	All Registers Cleared
1	1	0	0	0	0	DAC A LS Input Register Loaded with DB7-DB0(LSB)
1	1	0	0	0	1	DAC A MS Input Register Loaded with DB3(MSB)-DB0
1	1	0	0	1	0	DAC B LS Input Register Loaded with DB7-DB0(LSB)
1	1	0	0	1	1	DAC B MS Input Register Loaded with DB3(MSB)-DB0
1	0	1	0	X	X	DAC A, DAC B Registers Updated Simultaneously from Input Registers
1	0	0	0	X	X	DAC A, DAC B Registers are Transparent

NOTE: X = Don't care



NOTES
1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% OF +5V. $t_r = t_f$ = 20ns.
2. TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{IH}+V_{IL}}{2}$

Figure 2. Timing Diagram for AD7547

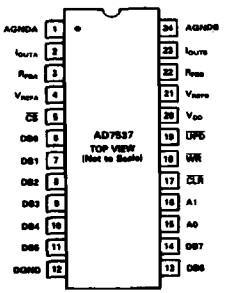
AD7547 ORDERING GUIDE[1]

Model[2]	Temperature Range	Relative Accuracy	Gain Error	Package Option[3]
AD7547JN	−40°C to +85°C	±1LSB	±6LSB	N-24
AD7547KN	−40°C to +85°C	±1/2LSB	±3LSB	N-24
AD7547LN	−40°C to +85°C	±1/2LSB	±1LSB	N-24
AD7547JP	−40°C to +85°C	±1LSB	±6LSB	P-28A
AD7547KP	−40°C to +85°C	±1/2LSB	±3LSB	P-28A
AD7547LP	−40°C to +85°C	±1/2LSB	±1LSB	P-28A
AD7547JR	−40°C to +85°C	±1LSB	±6LSB	R-24
AD7547KR	−40°C to +85°C	±1/2LSB	±3LSB	R-24
AD7547LR	−40°C to +85°C	±1/2LSB	±1LSB	R-24
AD7547AQ	−40°C to +85°C	±1LSB	±6LSB	Q-24
AD7547BQ	−40°C to +85°C	±1/2LSB	±3LSB	Q-24
AD7547CQ	−40°C to +85°C	±1/2LSB	±1LSB	Q-24
AD7547SQ	−55°C to +125°C	±1LSB	±6LSB	Q-24
AD7547TQ	−55°C to +125°C	±1/2LSB	±3LSB	Q-24
AD7547UQ	−55°C to +125°C	±1/2LSB	±2LSB	Q-24
AD7547SE	−55°C to +125°C	±1LSB	±6LSB	E-28A
AD7547TE	−55°C to +125°C	±1/2LSB	±3LSB	E-28A
AD7547UE	−55°C to +125°C	±1/2LSB	±2LSB	E-28A

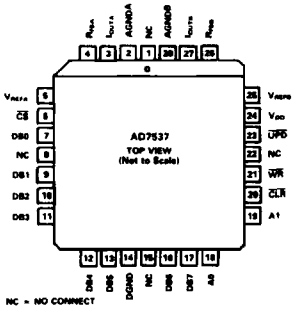
NOTES
[1]Analog Devices reserves the right to ship ceramic packages (D-24A) in lieu of cerdip packages (Q-24).
[2]To order MIL-STD-883, Class B processed parts, add /883B to part number. Contact your local sales office for military data sheets.
[3]E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = SOIC. For outline information see Package Information section.

AD7537 PIN CONFIGURATIONS

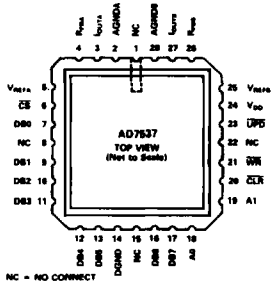
DIP



PLCC



LCCC



PIN FUNCTION DESCRIPTION (DIP)

PIN	MNEMONIC	DESCRIPTION
1	AGNDA	Analog Ground for DAC A.
2	I_{OUTA}	Current output terminal of DAC A.
3	R_{FBA}	Feedback resistor for DAC A.
4	V_{REFA}	Reference input to DAC A.
5	$\overline{CS}$	Chip Select Input. Active low.
6–14	DB0–DB7	Eight data inputs, DB0–DB7.
12	DGND	Digital Ground.
15	A0	Address Line 0.
16	A1	Address Line 1.
17	$\overline{CLR}$	Clear Input. Active low. Clears all registers.
18	$\overline{WR}$	Write Input. Active low.
19	$\overline{UPD}$	Updates DAC Registers from inputs registers.
20	V_{DD}	Power supply input. Nominally +12V to +15V, with ±10% tolerance.
21	V_{REFB}	Reference input to DAC B.
22	R_{FBB}	Feedback resistor for DAC B.
23	I_{OUTB}	Current output terminal of DAC B.
24	AGNDB	Analog Ground for DAC B.

ABSOLUTE MAXIMUM RATINGS*

(T_A = 25°C unless otherwise stated)

V_{DD} to DGND . . . . . −0.3V, +17V
V_{REFA}, V_{REFB} to AGND, ... ±25V
V_{RFBA}, V_{RFBB} to AGND, ... ±25V
Digital Input Voltage to DGND . . . . . −0.3V, V_{DD} +0.3V
I_{OUTA}, I_{OUTB} to DGND . . . . . −0.3V, V_{DD} +0.3V
AGND to DGND . . . . . −0.3V, V_{DD} +0.3V
Power Dissipation (Any Package)
To +75°C 450mW
Derates above +75°C . . . . . 6mW/°C

Operating Temperature Range
Commercial (J, K, L Versions) . . . . . −40°C to +85°C
Industrial (A, B, C Versions) . . . . . −40°C to +85°C
Extended (S, T, U Versions) . . . . . −55°C to +125°C
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10secs) . . . . . +300°C

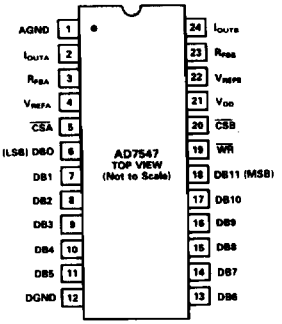
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

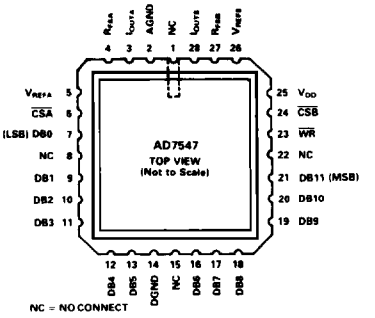
ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

AD7547 PIN CONFIGURATIONS

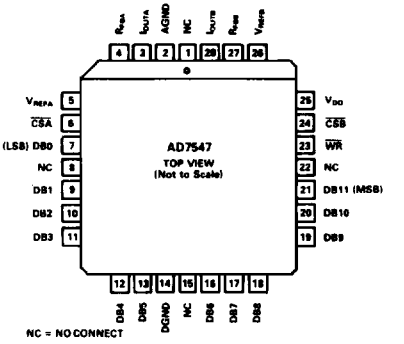
DIP, SOIC



LCCC



PLCC



PIN FUNCTION DESCRIPTION (DIP)

PIN	MNEMONIC	DESCRIPTION
1	AGND	Analog Ground.
2	I_{OUTA}	Current output terminal of DACA.
3	R_{FBA}	Feedback resistor for DACA.
4	V_{REFA}	Reference input to DACA.
5	$\overline{CSA}$	Chip Select Input for DAC A. Active low.
6-18	DB0-DB11	12 data inputs, DB0 (LSB) – DB11 (MSB).
12	DGND	Digital Ground.
19	$\overline{WR}$	Write Input. Data transfer occurs on rising edge of $\overline{WR}$. See Table I.
20	$\overline{CSB}$	Chip Select Input for DACB. Active low.
21	V_{DD}	Power supply input. Nominally + 12V to + 15V with ± 10% tolerance.
22	V_{REFB}	Reference input to DACB.
23	R_{FBB}	Feedback resistor of DACB.
24	I_{OUTB}	Current output terminal of DACB.

CIRCUIT INFORMATION

D/A SECTION

The AD7537/AD7547 contains two identical 12-bit multiplying D/A converters. Each DAC consists of a highly stable R-2R ladder and 12 N-channel current steering switches. Figure 3 shows a simplified D/A circuit for DAC A. In the R-2R ladder, binary weighted currents are steered between I_{OUTA} and AGND. The current flowing in each ladder leg is constant, irrespective of switch state. The feedback resistor R_{FBA} is used with an op-amp to convert the current flowing in I_{OUTA} to a voltage output.

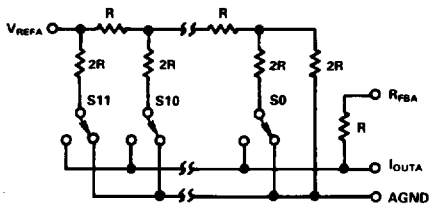


Figure 3. Simplified Circuit Diagram for DACA

EQUIVALENT CIRCUIT ANALYSIS

Figure 4 shows the equivalent circuit for one of the D/A converters (DAC A) in the AD7537/AD7547. A similar equivalent circuit can be drawn for DACB. Note that AGND is common to both DAC A and DAC B.

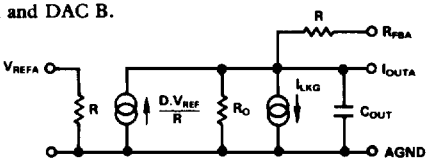


Figure 4. Equivalent Analog Circuit for DACA

C_{OUT} is the output capacitance due to the N-channel switches and varies from about 50pF to 150pF with digital input code. The current source I_{LKG} is composed of surface and junction leakages and approximately doubles every 10°C. R_O is the equivalent output resistance of the device which varies with input code.

DIGITAL CIRCUIT INFORMATION

The digital inputs are designed to be both TTL and 5V CMOS compatible. All logic inputs are static-protected MOS gates with typical input currents of less than 1nA.