19-1041; Rev 1; 8/92

MAXIM

CMOS, Complete, High-Speed, 12-Bit A/D Converter

1.0 SCOPE

1.1 This specification covers the detail requirements for a monolithic, CMOS, successive-approximation, 12-bit analog-to-digital converter with an on-chip buried-zener reference. This device features internal or external clock operation and a conversion speed of 5µs or 12.5µs. This circuit is processed in accordance with MIL-STD-883 and is fully compliant to paragraph 1.2.1.

It is highly recommended that this data sheet be used as a baseline for new military or aerospace source control drawings.

For typical applications and operating characteristics, consult Maxim's data books.

1.2 Part Numbers

Device	Part Number
-1	MX7572S(X)12/883B
-2	MX7572T(X)12/883B
-3	MX7572U(X)12/883B
-4	MX7572S(X)05/883B
-5	MX7572T(X)05/883B
-6	MX7572U(X)05/883B

1.3 Package

(X)	Package	Description
Q	Q-24	24-Pin Ceramic Dual-In-Line Package (CERDIP)
E	E-28	28-Pin Ceramic Leadless Chip Carrier (LCC)

Note: See *Package Information* section for package drawings and dimensions.

1.4 Absolute Maximum Ratings

(T_A = +25°C, unless otherwise noted.)

V_{DD} to DGND ..... -0.3V, +7V
V_{SS} to DGND ..... +0.3V, -17V
AGND to DGND ..... -0.3V, (V_{DD} +0.3V)
AIN to AGND ..... -15V, +15V
Digital Input Voltage to DGND ..... -0.3V, (V_{DD} +0.3V)
Digital Output Voltage to DGND ..... -0.3V, (V_{DD} +0.3V)
Power Dissipation (T_A = +70°C, Tj = +150°C)
  24-Pin CERDIP (derate 12.50mW/°C above +70°C) 1000mW
  28-Pin LCC (derate 10.02mW/°C above +70°C) 802mW
Operating Temperature Range ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10 sec) ..... +300°C

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1.5 Thermal Resistance Θ_{JC} = 40°C/W for Q-24
Θ_{JC} = 50°C/W for E-28
Θ_{JA} = 80°C/W for Q-24
Θ_{JA} = 98°C/W for E-28

2.0 REQUIREMENTS

2.1 Electrical performance characteristics are specified in Table 1 and apply over the full ambient operating temperature range, unless otherwise specified.

TABLE 1. ELECTRICAL PERFORMANCE CHARACTERISTICS (Note 1)

CHARACTERISTICS	SYMBOL	CONDITIONS	DEVICE TYPES	GROUP A SUB-GROUPS	LIMITS MIN	LIMITS MAX	UNITS
Resolution			All		12		Bits
Integral Nonlinearity	INL		-1, -2, -4, -5	1	-1	1	LSB
			-3, -6	1	-0.5	0.5	
			-1, -2, -4, -5	2, 3	-1	1	
			-3, -6	2, 3	-0.75	0.75	
Differential Nonlinearity	DNL		All	1, 2, 3	-1	1	LSB
Offset Error	V_{OS}		-1, -4	1	-4	4	LSB
			-2, -3, -5, -6	1	-3	3	
			-1, -4	2, 3	-6	6	
			-2, -5	2, 3	-5	5	
			-3, -6	2, 3	-4	4	
Full-Scale Error	AE	Full scale = 5V, including internal voltage reference error, ideal last code transition = FS - 3/2LSBs	-1, -4	1	-15	15	LSB
			-2, -3, -5, -6	1	-10	10	
Full-Scale Temperature Coefficient	$\Delta AE/\Delta T$	Guaranteed by internal reference temperature coefficient limits; includes internal voltage reference drift	-1			45	ppm/°C
			-2, -3, -5, -6			25	
Analog Input Current	I_{IN}	AIN = 5V	All	1, 2, 3		3.5	mA
Internal Reference Voltage Output	VREF		All	1	-5.3	-5.2	V
Internal Reference Temperature Coefficient	TC_{REF}	$\Delta VREF/\Delta T$, for +25°C to -55°C or +125°C	-1, -4	2, 3		20	ppm/°C
			-2, -3, -5, -6			40	
Internal Reference Output Current Sink Capability		Constant external load during conversion	All	1, 2, 3		550	µA
Digital Input Low Voltage	V_{INL}	$\overline{CS}$, $\overline{RD}$, HBEN, CLKIN, V_{DD} = 4.75V, V_{SS} = -15V	All	1, 2, 3		0.8	V
Digital Input High Voltage	V_{INH}	$\overline{CS}$, $\overline{RD}$, HBEN, CLKIN, V_{DD} = 4.75V, V_{SS} = -15V	All	1, 2, 3	2.4		V
Digital Input Capacitance	C_{IN}	$\overline{CS}$, $\overline{RD}$, HBEN, CLKIN, V_{DD} = 4.75V, V_{SS} = -15V	All	4		10	pF

TABLE 1. ELECTRICAL PERFORMANCE CHARACTERISTICS (Note 1) (continued)

CHARACTERISTICS	SYMBOL	CONDITIONS	DEVICE TYPES	GROUP A SUB-GROUPS	LIMITS MIN	LIMITS MAX	UNITS
Digital Input Current	I_{IN}	$\overline{CS}$, $\overline{RD}$, HBEN, CLKIN, V_{DD} = 5.25V, V_{SS} = -15V AIN = 0V to V_{DD}	All	1, 2, 3	-10	10	µA
		CLKIN, V_{DD} = 5.25V, V_{SS} = -15V, AIN = 0V to V_{DD}			-20	20	
Digital Output Low Voltage	V_{OL}	D11-D0/8, BUSY, CLKOUT, V_{DD} = 4.75V, V_{SS} = -15V, I_{SINK} = 1.6mA	All	1, 2, 3		0.4	V
Digital Output High Voltage	V_{OH}	D11-D0/8, BUSY, CLKOUT, V_{DD} = 4.75V, V_{SS} = -15V, I_{SOURCE} = 200µA	All	1, 2, 3	4.0		V
Floating State Leakage Current	I_{LKG}	D11-D0/8, V_{DD} = 5.25V, V_{SS} = -15V	All	1, 2, 3	-10	10	µA
Floating State Output Capacitance (Note 2)	C_{OUT}		All	4		15	pF
Conversion Time Using Synchronous Clock	t_{CONV}		-4, -5, -6			5	µs
			-1, -2, -3			12.5	
Conversion Time Using Asynchronous Clock	t_{CONV}		-4, -5, -6		4.8	5.2	µs
			-1, -2, -3		12.0	13.0	
Positive Supply Current	I_{DD}	V_{DD} = 5.25V, V_{SS} = -15.75V, $\overline{CS}$ = $\overline{RD}$ = $\overline{BUSY}$ = HIGH, AIN = 5V	All	1, 2, 3		7	mA
Negative Supply Current	I_{SS}	V_{DD} = 5.25V, V_{SS} = -15.75V, $\overline{CS}$ = $\overline{RD}$ = $\overline{BUSY}$ = HIGH, AIN = 5V		1, 2, 3		12	mA
$\overline{CS}$ to $\overline{RD}$ Setup Time (Note 2)	t_1		All	9	0		ns
$\overline{RD}$ to $\overline{BUSY}$ Propagation Delay (Note 3)	t_2	T_A = +25°C	All	9		190	ns
		T_A = -55°C to +125°C		9		270	
Data-Access Time After $\overline{RD}$ (Note 4)	t_3	C_L = 60pF, Figure 2	All	9		110	ns
				10, 11		150	
		C_L = 100pF, Figure 2; T_A = +25°C	All	9		125	
				10, 11		170	
$\overline{RD}$ Pulse Width	t_4		All	9	t_3		ns
$\overline{CS}$ to $\overline{RD}$ Hold Time	t_5		All	9	0		ns
Data-Setup Time After $\overline{BUSY}$ (Note 4)	t_6	C_L = 60pF, Figure 2	All	9		70	ns
				10, 11		100	
Bus-Relinquish Time (Note 5)	t_7	Figure 3	All	9		75	ns
				10, 11		90	

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TABLE 1. ELECTRICAL PERFORMANCE CHARACTERISTICS (Note 1) (continued)

CHARACTERISTICS	SYMBOL	CONDITIONS	DEVICE TYPES	GROUP A SUB-GROUPS	LIMITS MIN	LIMITS MAX	UNITS
HBEN to $\overline{RD}$ Setup Time (Note 2)	t_8		All	9	0		ns
HBEN to $\overline{RD}$ Hold Time (Note 2)	t_9		All	9	0		ns
Delay Between Successive Read Operations (Note 2)	t_{10}		All	9	200		ns

Note 1: V_{DD} = +5V, V_{SS} = -15V, AIN = 0V to +5V, slow-memory mode, f_{CLK} = 1.0MHz (-1, -2, -3)/2.5MHz (-4, -5, -6), unless otherwise noted.
Note 2: Characterisitcs supplied for use as a typical design limit, but not production tested.
Note 3: All input control signals are specified with $t_r = t_f$ = 5ns (10% to 90% of +5V) and timed from a 1.6V voltage level. Times t_6 and t_{10} are measured only for the initial test and after process or design changes which may affect switching parameters.
Note 4: Times t_5 and t_6 are measured with the load circuits of Figure 2 and defined as the time required for an output to cross 0.8V or 2.4V.
Note 5: Time t_7 is defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 3.
Note 6: Timing shown in section 4.3.

3.0 QUALITY ASSURANCE

3.1 Sampling and inspection procedures shall be in accordance with MIL-M-38510 and, to the extent specified, with MIL-STD-883.

3.2 Screening shall be in accordance with Method 5004 of MIL-STD-883. Burn-in test (Method 1015):
(1) Test condition A, B, C, or D.
(2) T_A = +125°C, minimum.
(3) Interim and final electrical test requirements shall be as specified in Table 2.

3.3 Quality conformance inspection shall be in accordance with Method 5005 of MIL-STD-883 including Groups A, B, C, and D inspection.
Group A inspection:
(1) Tests as specified in Table 2.
(2) Selected subgroups in Table 1, Method 5005 of MIL-STD-883 shall be omitted.

3.4 Groups C and D inspections:
a. End-point electrical parameters shall be specified in Table 1.
b. Steady-state life test (Method 1005 of MIL-STD-883):
(1) Test condition A, B, C, or D.
(2) T_A = +125°C, minimum.
(3) Test duration, 1000 hours, except as permitted by Method 1005 of MIL-STD-883.

TABLE 2. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 Test Requirements	Subgroups (per Method 5005, Table 1)
Interim Electrical Parameters (Method 5004)	1
Final Electrical Parameters (Method 5004)	1,* 2, 3, 9
Group A Test Requirements (Method 5005)	1, 2, 3, 4,** 9, 10,*** 11***
Groups C and D End-Point Electrical Parameters (Method 5005)	1

* PDA applies to Subgroup 1 only.
** Subgroup 4 shall be tested at initial qualification and upon redesign. Sample size will be 5 units.
*** Subgroups 10 and 11, if not tested, shall be guaranteed to the limits in Table 1.

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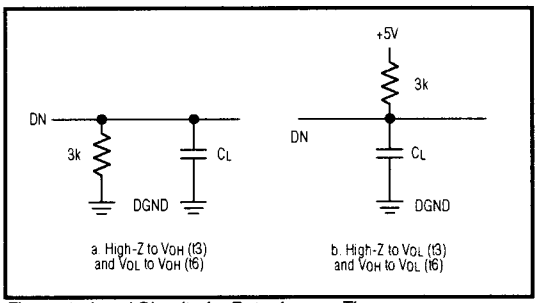


Figure 1. Load Circuits for Data-Access Time

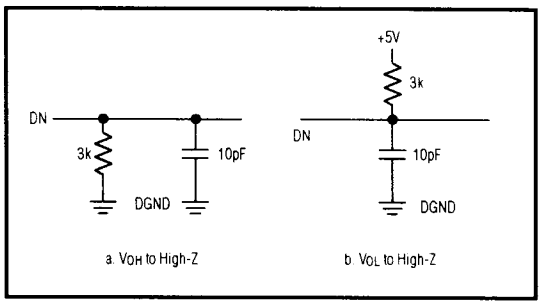
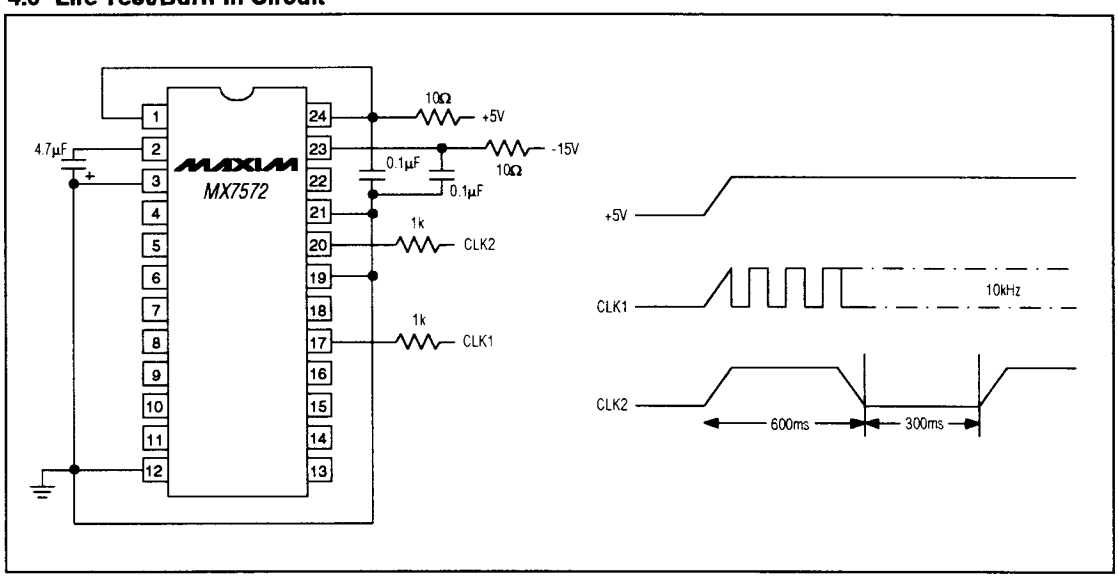
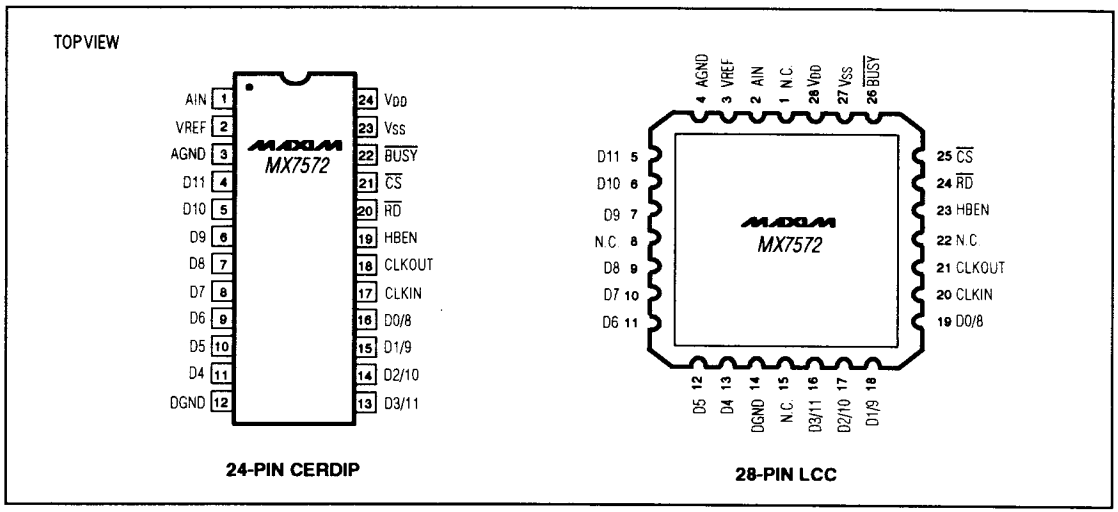


Figure 2. Load Circuits for Bus-Relinquish Time

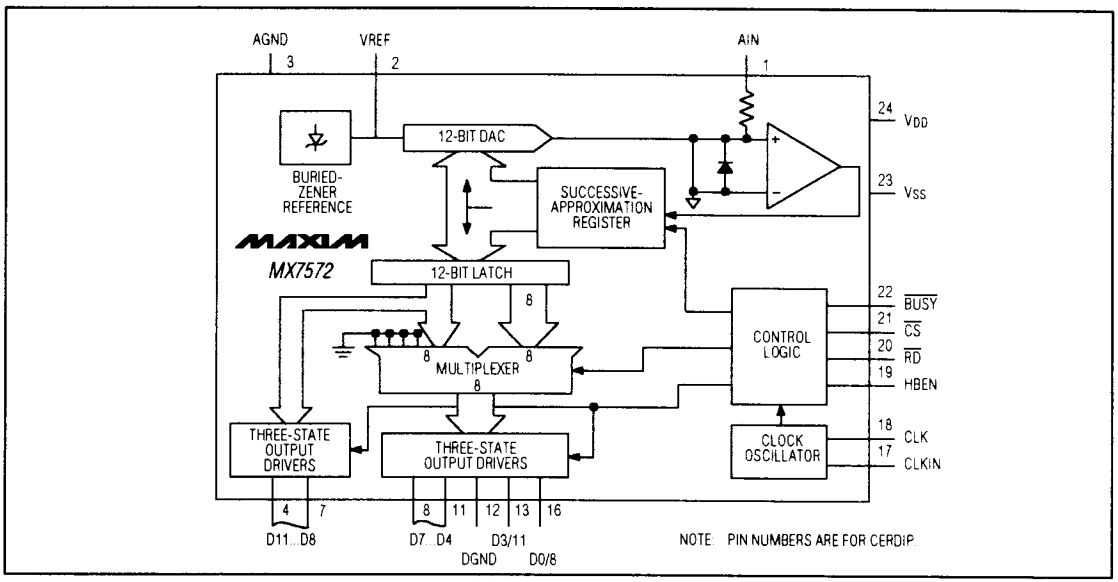
4.0 Life Test/Burn-In Circuit



4.1 Pin Configurations



4.2 Functional Diagram



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4.3 Timing Diagrams

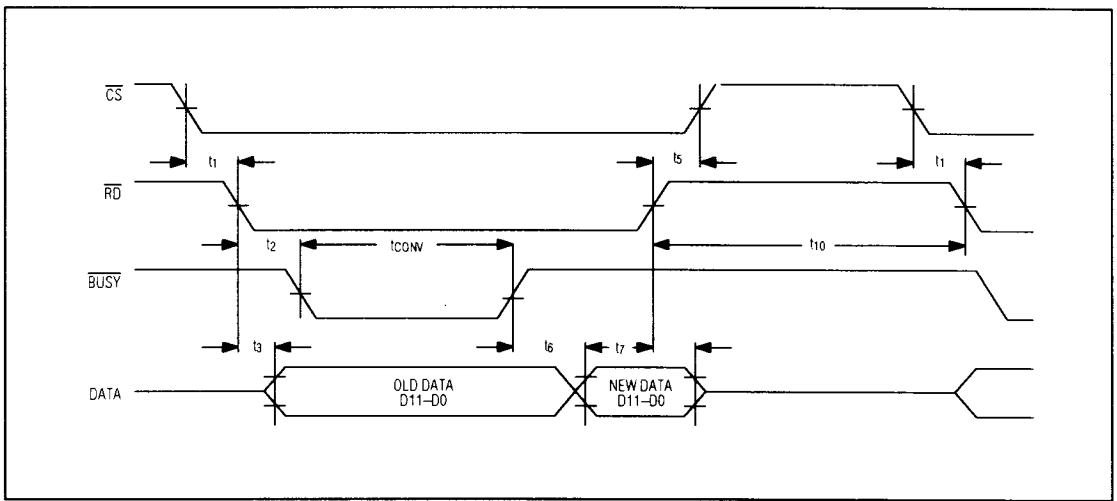

Figure 3. Slow-Memory Mode, Parallel Read

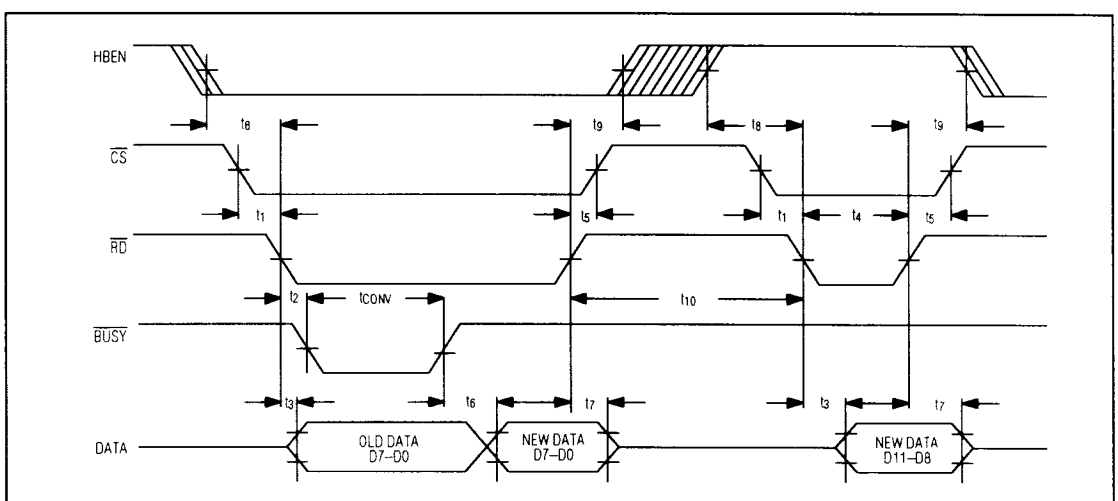

Figure 4. Slow-Memory Mode, Two-Byte Read

4.3 Timing Diagrams (continued)

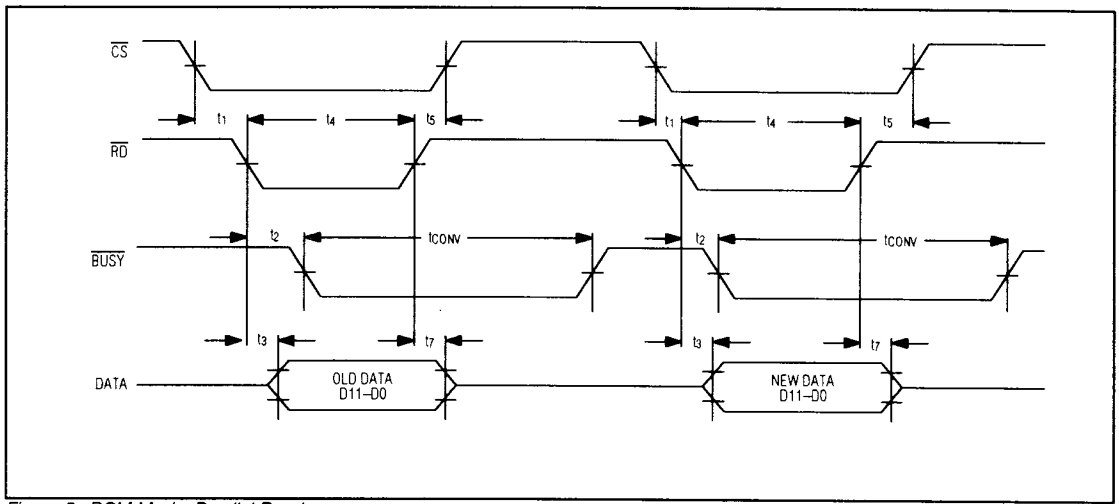

Figure 5. ROM Mode, Parallel Read

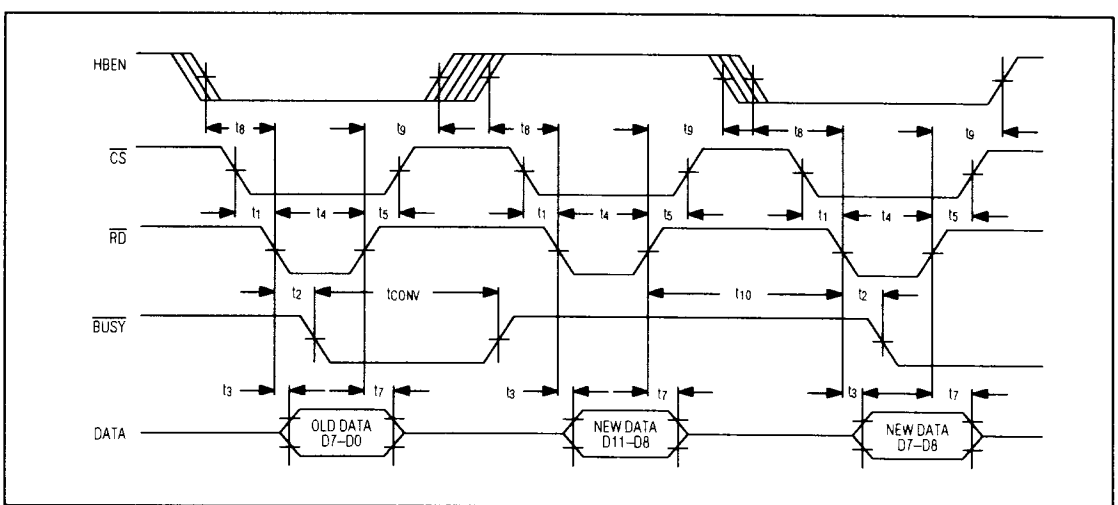

Figure 6. ROM Mode, Two-Byte Read

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4.4 Mode Control Tables

Table 1. Slow-Memory Mode, Parallel Read Data-Bus Status

MX7572 Data Outputs	D11	D10	D9	D8	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
Read	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

Table 2. Slow-Memory Mode, Two-Byte Read Data-Bus Status

MX7572 Data Outputs	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
First Read	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Second Read	Low	Low	Low	Low	DB11	DB10	DB9	DB8

Table 3. ROM Mode, Parallel Read Data-Bus Status

MX7572 Data Outputs	D11	D10	D9	D8	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
First Read (Old Data)	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Second Read	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

Table 4. ROM Mode, Two-Byte Read Data-Bus Status

MX7572 Data Outputs	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
First Read (Old Data)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Second Read	Low	Low	Low	Low	DB11	DB10	DB9	DB8
Third Read	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0