GaAs IC Saturated Power Amplifier 824–849 MHz

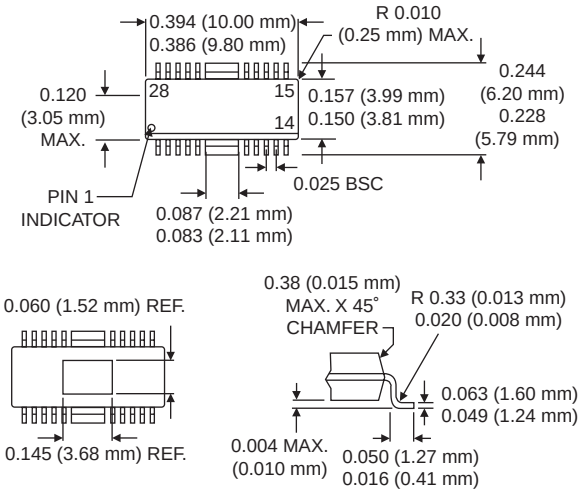
SKYWORKS

AP104-69

Features

- Output Power up to 30 dBm
- +4.8 V Operation, Single Supply
- Efficiency Greater Than 55%
- High Power SSOP-28 Batwing Package with Slug
- DC/DC Converter

SSOP-28 Slug



Description

The AP104-69 is a low cost IC power amplifier designed for the 824–849 MHz frequency band. It features 4 cell battery operation, and high efficiency. A DC/DC converter supplies -3 V to the power amplifier and can supply 1.5 mA to an external circuit. The amplifier is designed to be stable over a temperature range of -30 to 100°C and over 7:1 VSWR loads.

Output Matching Circuit

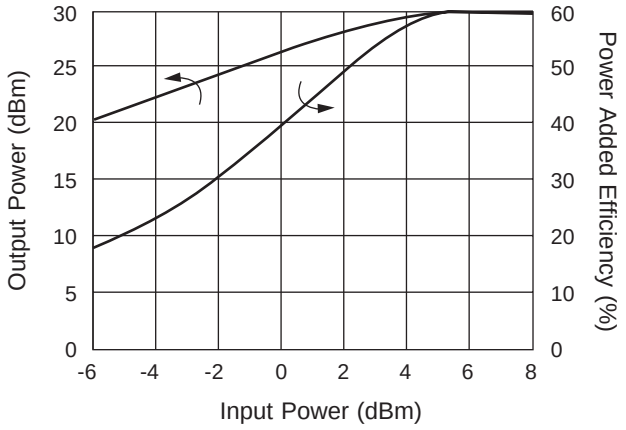
The output match for the AP104-69 is provided externally in order to improve performance, reduce cost, and add flexibility. By making use of ceramic surface mount components with better Qs than GaAs matching elements, a lower loss matching network can be made. This lower loss results in higher power and efficiency for the amplifier. Also, by keeping these elements external the GaAs die size is reduced and the overall cost is less. This approach also permits the flexibility to tweak the amplifier for optimum performance at different powers, and/or frequencies.

The board schematic demonstrates one way to present the optimum load match while providing a path for the DC bias.

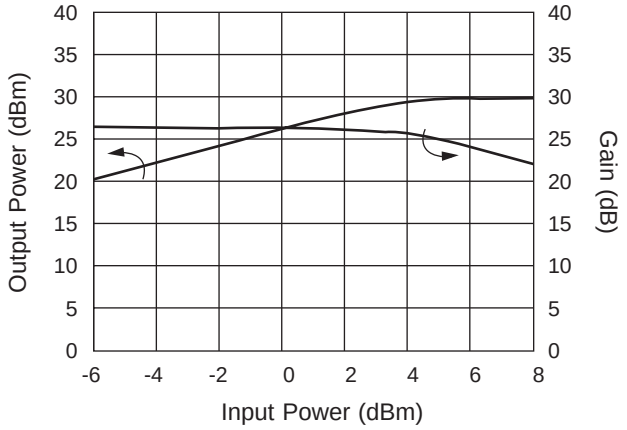
Electrical Specifications at 25°C

Characteristic	Condition	Frequency	Min.	Typ.	Max.	Unit
Output Power (Referenced at Output Pin)	$0<P_{IN}<7$	824–849 MHz		30		dBm
Efficiency	P_{OUT} = 29.5 dBm			60		%
Small Signal Gain	P_{IN} = -20 dBm			25		dB
Idle Current	P_{IN} = -60 dBm			75		mA
Noise in the Receive Band	P_{OUT} = 29.5 dBm R_X Band = 869–894 MHz R_X Bandwidth = 30 kHz			-100	-95	dBm
Reference Current	P_{OUT} = 29.5 dBm			1.0	5.0	mA
Input VSWR	P_{IN} = -30 to +7 dBm				2.5:1	
Harmonic Power	2fo 3fo			-25 -35		dBc
Input Impedance				50		Ω

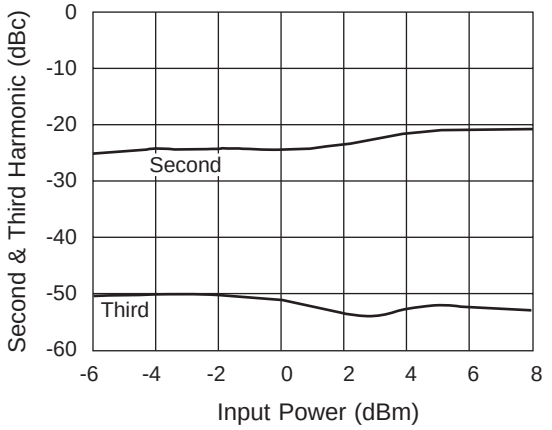
Typical Performance Data (824–849 MHz)



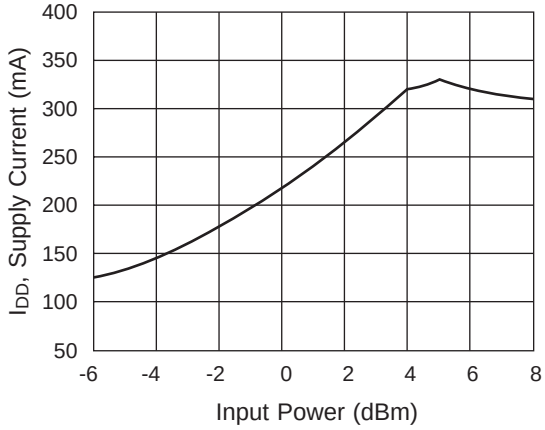
P_{OUT}, P.A.E. vs. P_{IN}



P_{OUT}, Gain vs. P_{IN}

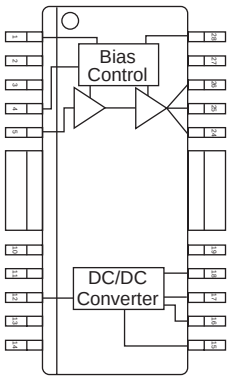


Second & Third Harmonic vs. P_{IN}



I_{DD} vs. P_{IN}

Pin Out



Pin Out Assignments

Pin 1: V_{REF}
Reference voltage for bias control circuitry. 1.2K resistor between this pin and Pin 28 needed to set nominal drain currents.

Pin 2: V_{GS2}
Second stage gate voltage tap. Should be bypassed as shown.

Pin 3: V_{DS1}
First stage drain bias feed. Requires a matching inductor with good RF bypassing and the +4.8 V nominal supply voltage.

Pin 4: V_{GS1}
First stage gate voltage tap. Requires similar RF bypassing as Pin 2 and a 22K resistor to properly bias the first stage.

Pin 5: RF In
RF input with a 33 pF series input matching capacitor.

Pin 6-14: GND
Connect to ground.

Pin 15: V_{GEN}
Supply voltage to DC/DC converter. Requires 3.75 V with 100 nF of bypassing.

Pin 16: $V_{SS\ OUT}$
Negative output voltage from DC/DC converter. Two bypassing capacitors, a 100 nF and a 33 pF capacitor, are required. This voltage should be supplied to the bias controller network at Pin 27. External circuitry (LCD display, driver amplifiers, etc.) can tap off the negative voltage at this point. A maximum of 2 mA can be supplied.

Pin 17: CB
Switched capacitor for DC/DC converter. A 100 nF capacitor must be connected between Pin 17 and Pin 18 with a minimal distance between the capacitor and the chip.

Pin 18: CA
Switched capacitor for DC/DC converter, shared with Pin 17.

Pin 19–23: GND
Connect to ground.

Pin 24–26: RF Out/V_{DD2}
RF output and bias injection for the second stage drain. Output matching circuitry is required to transform the optimum load impedance to 50 Ω. The circuit must also provide a path for the +4.8 V DC bias and have good RF bypassing.

Pin 27: $V_{SS\ IN}$
Negative voltage for the bias controller circuit. The negative voltage from the DC/DC converter, Pin 16, should be fed to this pin.

Pin 28: V_{DD}
Bias controller supply voltage. The regulated +3.75 V supply must be connected to this pin. Disconnecting this voltage will turn the PA bias off. A switch at this pin can turn the PA on or off while leaving V_{GEN} connected and the negative supply unchanged. A 1.2K resistor must be connected between this pin and Pin 1.

Pin Configuration

Terminal	Symbol	Function
1	V_{REF}	Reference Voltage
2	V_{GS2}	Gate Voltage 2
3	V_{DS1}	Drain Supply Voltage 1
4	V_{GS1}	Gate Voltage 1
5	RF In	RF Input
6	GND	Ground
7	GND	Ground
8	GND	Ground
9	GND	Ground
10	GND	Ground
11	GND	Ground
12	GND	Ground
13	GND	Ground
14	V_{REF}	Voltage Generator Ground
15	V_{GEN}	Generator Voltage
16	$V_{SS\ OUT}$	Negative Bias Voltage Out
17	CB	Generator Flying Cap
18	CA	Generator Flying Cap
19	GND	Ground
20	GND	Ground
21	GND	Ground
22	GND	Ground
23	GND	Ground
24	RF Out/V_{DS2}	RF Output/Supply Voltage 2
25	RF Out/V_{DS2}	RF Output/Supply Voltage 2
26	RF Out/V_{DS2}	RF Output/Supply Voltage 2
27	$V_{SS\ IN}$	Negative Bias Voltage In
28	V_{DD}	Positive Bias Voltage

Bias Controller Circuit

An on-chip bias controller circuit eliminates the need to individually adjust the gate bias voltages. This circuit uses 3.75 V and the negative voltage from the DC converter (-2.7 V to -3.75 V) to set the gate voltages on each stage for the proper bias current.

Standby Mode

The power amplifier should be turned off whenever possible in order to reduce the overall power consumption. The AP104 can be turned off in several ways. The simplest is to switch the bias controller supply voltage (Pin 28) open. The gate bias voltages are in turn reduced from their nominal voltages to V_{SS}, resulting in a PA bias current of less than 1 mA. Additional PMOS switches in the drain lines drop the bias-off currents to <10 µA.

Absolute Maximum Ratings

Characteristic	Value
Drain Voltage (V_{DD})	+10 V
Bias Voltage (V_{SS})	-6 V
Reference Voltage (V_{REF})	+6 V
Power Input (P_{IN})	+12 dBm
Operating Temperature (T_{OPT})	-30 to +100°C
Storage Temperature (T_{STG})	-35 to +120°C

Circuit Layout