GaAs IC Linear Power Amplifier

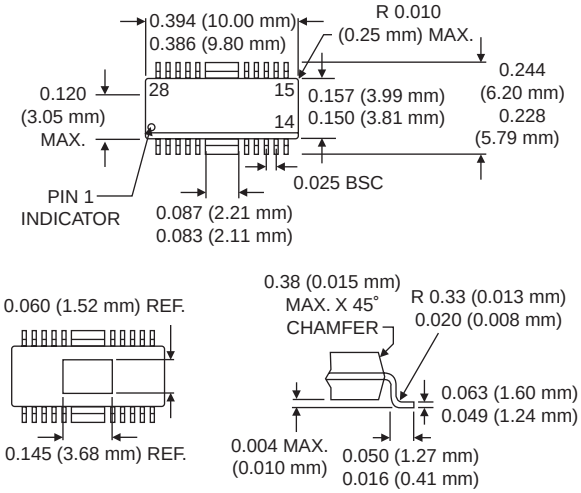
SKYWORKS

AP105-69

Features

- IS-136/54 TDMA
- IS-95 CDMA
- Linear Power up to 28 dBm Nominal
- Nominal 6 V Operation, Single Supply Operation
- Efficiency Greater Than 35%
- High Power SSOP-28 Batwing Package with Slug

SSOP-28 Slug



Description

The AP105-69 is a low cost IC power amplifier designed for the 824–849 MHz frequency band. It features 5 cell battery operation and operates from 5 V to 7.5 V with excellent linearity, and high efficiency. An integrated DC/DC converter supplies -4 V to the power amplifier and can supply 1.5 mA to an external circuit. The amplifier is designed to be stable over a temperature range of -30 to 100°C and over 3:1 VSWR loads.

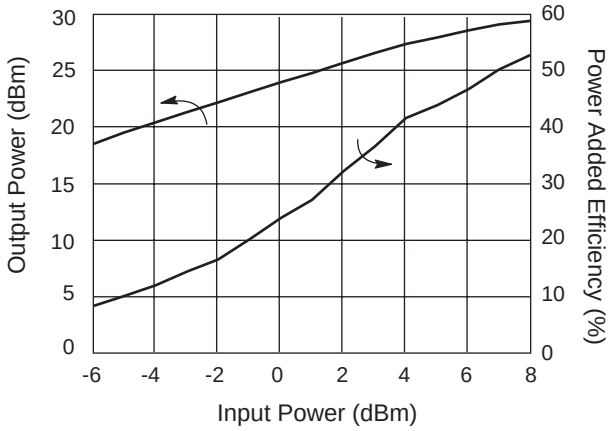
Electrical Specifications at 25°C

Characteristic	Condition	Frequency	Min.	Typ.	Max.	Unit
Digital Mode						
P_{OUT} (Reference at Output Pin Leads)	$0<P_{IN}<5$	824–849 MHz		28		dBm
Efficiency	P_{OUT} = 28 dBm			37		%
Large Signal Gain	P_{IN} = -20 dBm			26		dB
Idle Current	P_{IN} = -60 dBm			150	200	mA
Noise in the Receive Band	P_{OUT} = 28 dBm R_X Band = 869–894 MHz R_X Bandwidth = 30 kHz			-100	-95	dBm
Reference Current	P_{OUT} = 28 dBm			1	5	mA
Input VSWR	P_{IN} = -30 to +7 dBm			2.5:1		
Analog Mode						
P_{OUT}	$0<P_{IN}<5$	824–849 MHz		28		dBm
Efficiency	P_{OUT} = 28 dBm			40		%
Large Signal Gain	P_{IN} = -20 dBm			24		dB
Idle Current	P_{IN} = -60 dBm			50	90	mA

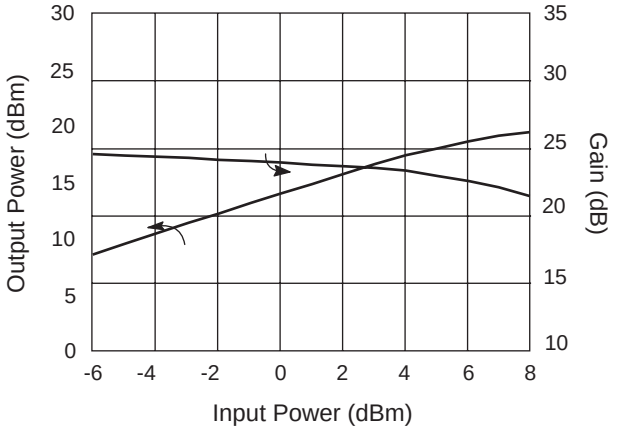
Operating Characteristics at 25°C

Characteristic	Condition	Frequency	Min.	Typ.	Max.	Unit
Voltage			5	6	7.5	V
IM3@ Rated P_{OUT}	P_{OUT} = 31 dBm PEP			-24		dBc
IM5@ Rated P_{OUT}	P_{OUT} = 31 dBm PEP			-34		dBc
IM7@ Rated P_{OUT}	P_{OUT} = 31 dBm PEP			-38		dBc
Harmonic Power	2fo 3fo			-30 -45		dBc
Modulation	Channel Spacing = 30 kHz, 832 Channels, Pi/4 QPSK					
P_{ADJ}	30 kHz 60 kHz 90 kHz			-28 -49 -60		dBc
Input Impedance				50		Ω

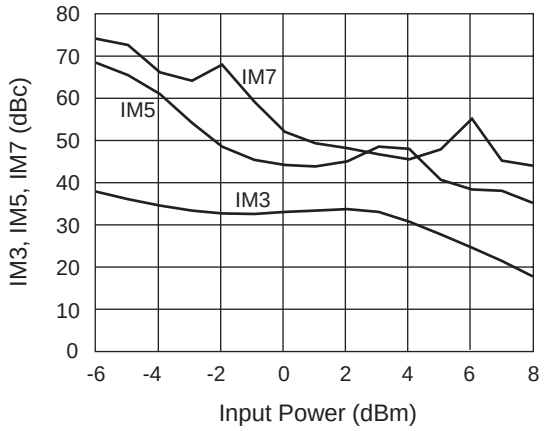
Typical Performance Data (824–849 MHz)



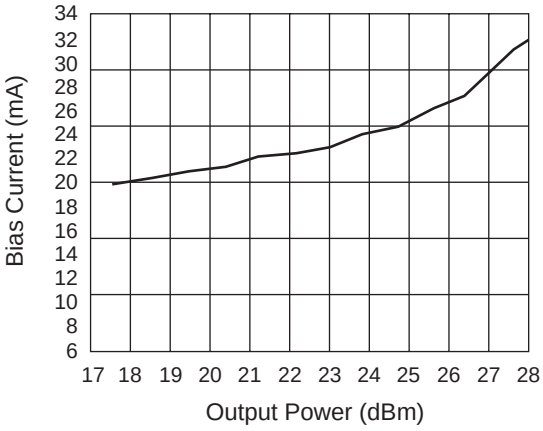
P_{OUT}, P.A.E. vs. P_{IN}



P_{OUT}, Gain vs. P_{IN}

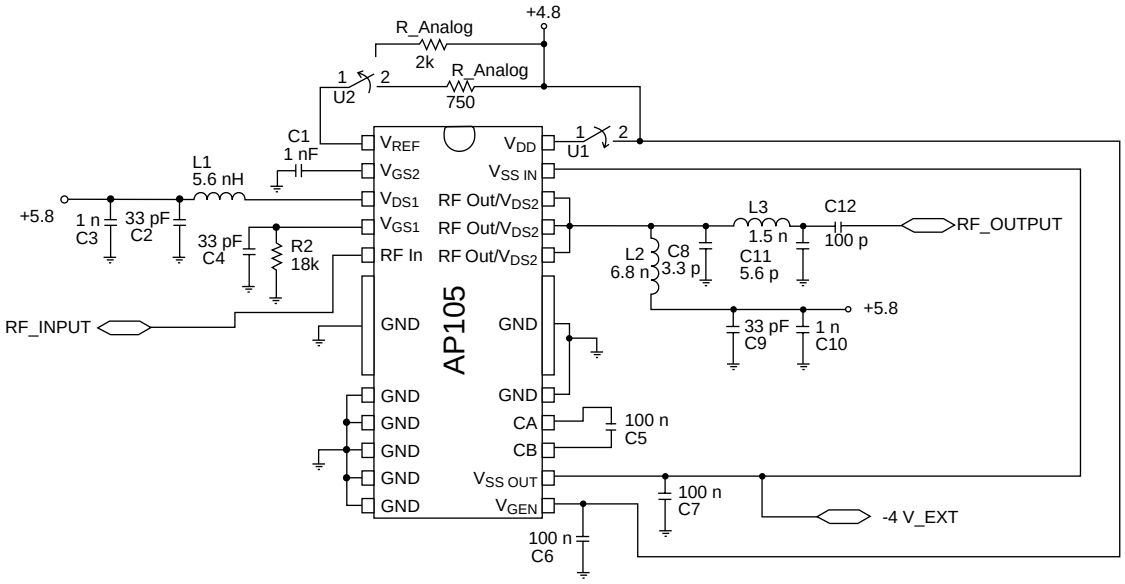


Distortion. vs. P_{IN}



Bias Current vs. P_{OUT}

Power Amplifier Typical Configuration



Output Matching Circuit

The output match for the AP105 is provided externally in order to improve performance, reduce cost, and add flexibility. By making use of ceramic surface mount components with better Qs than GaAs matching elements, a lower loss matching network can be made. This lower loss results in higher power and efficiency for the amplifier. Also, by keeping these elements external the GaAs die size is reduced and the overall cost is less. This approach also permits the flexibility to tweak the amplifier for optimum performance at different powers, and/or frequencies.

The board schematic demonstrates one way to present the optimum load match while providing a path for the DC bias.

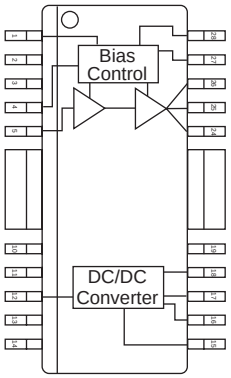
Bias Controller Circuit

An on-chip bias controller circuit eliminates the need to individually adjust the gate bias voltages. This circuit uses +4.8 V and the negative voltage from the DC converter (-3.5 V to -4.5 V) to set the gate voltages on each stage for the proper bias current. Pin 1 can be used to adjust the bias current between a linear and a saturated mode of operation. By switching resistors between this pin and +4.8 V, different quiescent currents can be selected. A current of 100-200 mA for good linearity in the digital mode, and a lower current, less than 100 mA, for better power consumption in the analog mode is optimum.

Standby Mode

The power amplifier should be turned off whenever possible in order to reduce the overall power consumption. The AP105 can be turned off in several ways. The simplest is to switch the bias controller supply voltage (Pin 1) open. This, in effect, switches the gate voltages to V_{SS}. The bias current of the PA in this condition will drop to less than 1 mA. By adding PMOS switches to the drain lines bias-off currents on the order of a few µA can be achieved.

Pin Out Assignments



Pin 1: V_{REF}

Sets the quiescent bias current. Nominally +3.5 V for a bias of 120-200 mA with best gain and linearity. Lower voltages in the range of +1 to +3.5 V will set the amplifier for less quiescent bias current. This is useful for analog or saturated operation where linearity is not critical. A resistor

divider network can be used with the +4.8 V regulated supply to achieve the nominal voltage. The input impedance of this pin is 2 kΩ. A switch can be used to change the resistance and toggle the amp between digital and analog mode.

Pin 2: V_{GS2}
Second stage gate voltage tap. Should be bypassed with a 1nF capacitor. This value is not critical.

Pin 3: V_{DS1}
First stage drain bias feed. Requires a matching inductor with good RF bypassing and the +5.8 V nominal supply voltage.

Pin 4: V_{GS1}
First stage gate voltage. Requires RF bypassing and an 18K resistor to properly bias the first stage.

Pin 5: RF In
50 Ω RF input.

Pin 6-14: GND
Connect to ground.

Pin 15: V_{GEN}
Supply voltage to DC/DC converter. Requires +4.8 V with a 100 nF bypassing capacitor.

Pin 16: $V_{SS\ OUT}$
Negative output voltage from the DC/DC converter. A 100 nF capacitor is required. This voltage should be supplied to the bias controller network at Pin 27. External circuitry (LCD display, driver amplifiers, etc.) can tap off the negative voltage at this point. Maximum current 2 mA.

Pin 17: CB
Switched capacitor for DC/DC converter. 100 nF capacitor should be connected between Pin 17 and Pin 18 with minimal distance between the capacitor and the chip.

Pin 18: CA
Switch capacitor for DC/DC converter, shared with Pin 17.

Pin 19-23: GND
Connect to ground.

Pin 24-26: RF Out/V_{DS2}
RF output and bias feed for the second stage drain. Output matching circuitry is required to transform the optimum load impedance to 50 Ω. The circuit must also provide a path for the +5.8 V nominal DC bias and have good RF bypassing.

Pin 27: $V_{SS\ IN}$
Negative voltage for the bias controller circuit. The negative voltage from the DC/DC converter (Pin 16) should be fed to this pin.

Pin 28: V_{DD}
Bias controller supply voltage. The regulated 4.8 V supply must be connected to this pin. Disconnecting this voltage will turn the PA bias off. A switch at this pin can turn the PA on or off while leaving V_{GEN} connected and the negative supply unchanged.

Pin Configuration

Terminal	Symbol	Function
1	V_{REF}	Reference Voltage
2	V_{GS2}	Gate Voltage 2
3	V_{DS1}	Supply Voltage 1
4	V_{GS1}	Gate Voltage 1
5	RF In	RF Input
6	GND	Ground
7	GND	Ground
8	GND	Ground
9	GND	Ground
10	GND	Ground
11	GND	Ground
12	GND	Ground
13	GND	Ground
14	V_{NGND}	Voltage Generator Ground
15	V_{GEN}	Generator Voltage
16	$V_{SS\ OUT}$	Bias Voltage Out
17	CB	Generator Flying Cap
18	CA	Generator Flying Cap
19	GND	Ground
20	GND	Ground
21	GND	Ground
22	GND	Ground
23	GND	Ground
24	RF Out/V_{DS2}	RF Output/Supply Voltage 2
25	RF Out/V_{DS2}	RF Output/Supply Voltage 2
26	RF Out/V_{DS2}	RF Output/Supply Voltage 2
27	$V_{SS\ IN}$	Negative Bias Voltage Input
28	V_{DD}	Positive Bias Voltage Input

Absolute Maximum Ratings

Characteristic	Value
Drain Voltage (V_{DD})	10 V
Bias Voltage (V_{SS})	-6 V
Reference Voltage (V_{REF})	6 V
Power Input (P_{IN})	12 dBm
Operating Temperature (T_{OPT})	-30 to +100°C
Storage Temperature (T_{STG})	-35 to +120°C