



# AP9A104

## 64K x 16 CMOS Static RAM

### Features

- Fast access times: 10, 12, 15, and 20 ns
- Drives a 50 pF load vs. 30 pF industry standard load
- Multiple center power and ground pins for improved noise immunity
- Low active power
- Low standby power: 11 mW (Max.)
- Individual byte controls for both Read and Write cycles
- TTL and CMOS-compatible inputs and outputs
- Single 5V  $\pm 10\%$  power supply
- Packaged in 44-pin, 400-mil SOJ, TSOP (Type II)

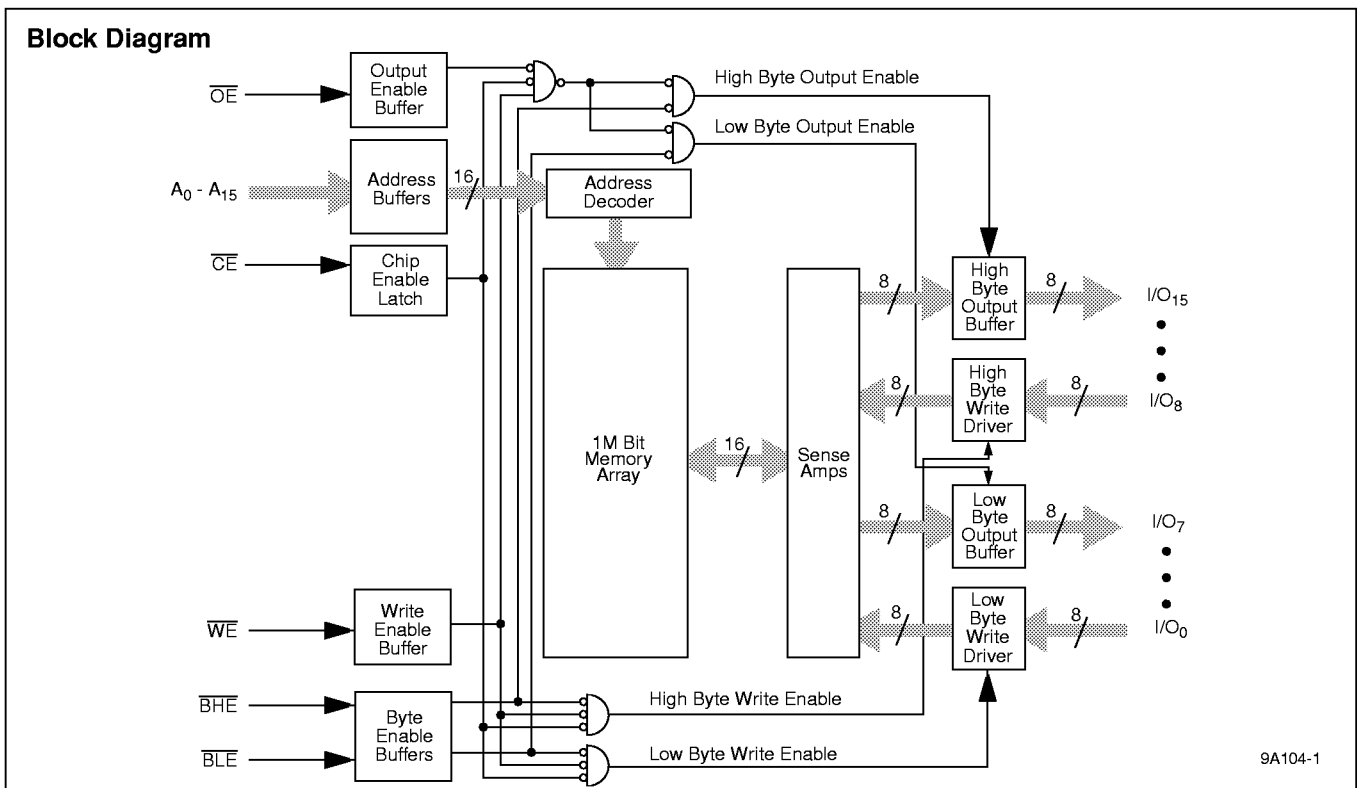
### Functional Description

The Aptos AP9A104 is a high-speed, low-power, 64K x 16 CMOS static RAM. It is fabricated using Aptos' high-performance, 0.45 $\mu$ , CMOS process technology. This highly reliable process, coupled with innovative circuit design techniques yields high performance at low power consumption. Writing to

the device is accomplished by bringing Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW. If Byte Enable Low ( $\overline{BLE}$ ) is LOW, then data from I/O<sub>0</sub> through I/O<sub>7</sub> is written into the location specified on the address pins A<sub>0</sub> through A<sub>15</sub>. If Byte Enable High ( $\overline{BHE}$ ) is LOW, then data from I/O<sub>8</sub> through I/O<sub>15</sub> is written into the location specified on the address pins A<sub>0</sub> through A<sub>15</sub>.

Reading from the AP9A104 is accomplished by taking  $\overline{CE}$  and  $\overline{OE}$  LOW while forcing  $\overline{WE}$  HIGH. If  $\overline{BLE}$  is LOW, then data from the memory location specified by the address pins will appear on I/O<sub>0</sub> through I/O<sub>7</sub>. If  $\overline{BHE}$  is LOW, then data from memory will appear on I/O<sub>8</sub> through I/O<sub>15</sub> (See Truth Table).

This device offers multiple center power and ground pins for improved noise and speed characteristics.



### Selection Guide

	AP9A104-10	AP9A104-12	AP9A104-15	AP9A104-20
Maximum Access Time (ns)	10	12	15	20
Maximum Operating Current (mA)	140	130	120	110
Maximum Standby Current (mA)	2	2	2	2





**Switching Characteristics** Over the Operating Range <sup>5, 6</sup>

Parameter	Description	9A104-10		9A104-12		9A104-15		9A104-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<i>Read Cycle</i> <sup>7</sup>										
t <sub>RC</sub>	Read Cycle Time	10		12		15		20		ns
t <sub>AA</sub>	Address Access Time		10		12		15		20	ns
t <sub>OHA</sub>	Output Hold Time	3		3		3		3		ns
t <sub>ACE</sub>	$\overline{CE}$ Access Time		10		12		15		20	ns
t <sub>DOE</sub>	$\overline{OE}$ Access Time		5		5		5		6	ns
t <sub>LZOE</sub> <sup>8</sup>	$\overline{OE}$ to Low-Z Output	0		0		0		0		ns
t <sub>HZOE</sub> <sup>8</sup>	$\overline{OE}$ to High-Z Output		3		3		5		6	ns
t <sub>LZCE</sub> <sup>8</sup>	$\overline{CE}$ to Low-Z Output	3		3		3		3		ns
t <sub>HZCE</sub> <sup>8</sup>	$\overline{CE}$ to High-Z Output		5		6		8		9	ns
t <sub>PU</sub>	$\overline{CE}$ to Power Up	0		0		0		0		ns
t <sub>PD</sub>	$\overline{CE}$ to Power Down		10		12		15		20	ns
t <sub>ABE</sub>	Byte Enable Access Time		5		5		5		6	ns
t <sub>LZBE</sub>	Byte Enable to Output Low-Z	0		0		0		0		ns
t <sub>HZBE</sub>	Byte Enable to Output High-Z		3		3		5		6	ns
<i>Write Cycle</i> <sup>9</sup>										
t <sub>WC</sub>	Write Cycle Time	10		12		15		20		ns
t <sub>SCE</sub>	$\overline{CE}$ to Write End	9		10		12		12		ns
t <sub>AW</sub>	Address to Set-up Time to Write End	9		10		12		12		ns
t <sub>HA</sub>	Address Hold to Write End	0		0		0		0		ns
t <sub>SA</sub>	Address Set-up Time to Write Start	0		0		0		0		ns
t <sub>PWE1</sub> <sup>10</sup>	$\overline{WE}$ Pulse Width ( $\overline{OE} = \text{HIGH}$ )	7		8		10		12		ns
t <sub>PWE2</sub>	$\overline{WE}$ Pulse Width ( $\overline{OE} = \text{LOW}$ )	10		12		12		15		ns
t <sub>SD</sub>	Data Set-up to Write End	6		6		7		10		ns
t <sub>HD</sub>	Data Hold from Write End	0		0		0		0		ns
t <sub>HZWE</sub> <sup>8</sup>	$\overline{WE}$ LOW to High-Z Output		5		6		7		9	ns
t <sub>LZWE</sub> <sup>8</sup>	$\overline{WE}$ HIGH to Low-Z Output	2		2		2		2		ns
t <sub>BW</sub>	Byte Enable to End of Write	9		10		12		12		ns

**Notes:**

5. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 V to 3.0 V and output loading specified in AC Test Loads and Waveforms *Figure (a)*, unless otherwise noted.

6. I/O will assume the High-Z state if  $\overline{OE} \geq V_{IH}$ .

7.  $\overline{WE}$  is HIGH for a Read Cycle.

8. Tested with the load in AC Test Loads and Waveforms *Figure (b)*. Transition is measured  $\pm 500\text{mV}$  from steady state voltage.

9. The internal write time is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. All signals must be in valid states to initiate a Write, but any can be deasserted to terminate the Write. The Data Input Set-up and Hold timing is referenced to the rising or falling edge of the signal that terminates the write.

10. Tested with  $\overline{OE}$  HIGH for a minimum of 4 ns before  $\overline{WE} = \text{LOW}$  to place I/O in High-Z state.

11. The device is continuously selected.  $\overline{OE}, \overline{CE} = V_{IL}$ .

12. Address is valid prior to, or coincident with,  $\overline{CE}$  LOW transitions.

13. At any given temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub>, t<sub>HZOE</sub> is less than t<sub>LZOE</sub> and t<sub>HZBE</sub> is less than t<sub>LZBE</sub>.

14.  $\overline{BHE}$  and  $\overline{BLE}$  are held in their asserted state (LOW).

### Pin Descriptions

#### A<sub>0</sub> - A<sub>15</sub>: Address Inputs

These 16 address inputs select one of the 65,536 16-bit words in the RAM.

#### $\overline{CE}$ : Chip Enable Input

$\overline{CE}$  is asserted LOW. The Chip Enable is asserted LOW to read from or write to the device. If Chip Enable is deasserted, the device is deselected and is in a standby power mode. The I/O pins will be in the high-impedance state when the device is deselected.

#### $\overline{OE}$ : Output Enable Input

The Output Enable input is asserted LOW. If the Output Enable is asserted LOW while  $\overline{CE}$  is asserted (LOW) and  $\overline{WE}$  is deasserted (HIGH), data from the SRAM will be

present on the I/O pins. The I/O pins will be in the high-impedance state when  $\overline{OE}$  is deasserted.

#### $\overline{WE}$ : Write Enable Input

The Write Enable input is asserted LOW and controls read and write operations. When  $\overline{CE}$  and  $\overline{WE}$  are both asserted (LOW) input data present on the I/O pins will be written into the selected memory location.

#### $\overline{BHE}$ , $\overline{BLE}$ : Byte Enables

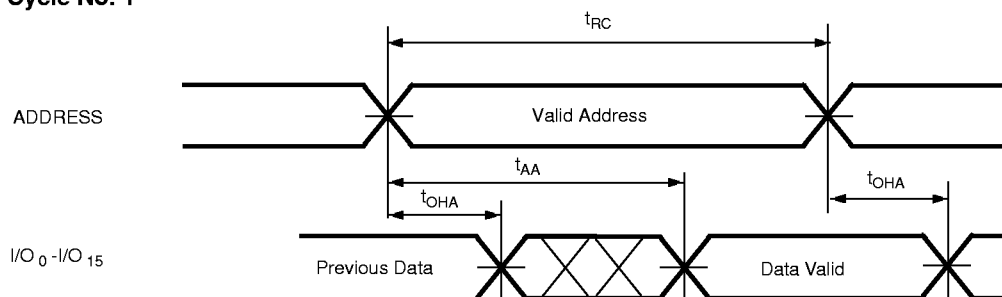
These active LOW inputs allow individual bytes to be written or read. When  $\overline{BLE}$  is LOW, data is written or read to the lower byte (I/O<sub>0</sub> - I/O<sub>7</sub>). When  $\overline{BHE}$  is LOW, data is written or read to the upper byte (I/O<sub>8</sub> - I/O<sub>15</sub>).

#### I/O<sub>0</sub> - I/O<sub>15</sub>: Common Input/Output Pins

GND: Ground

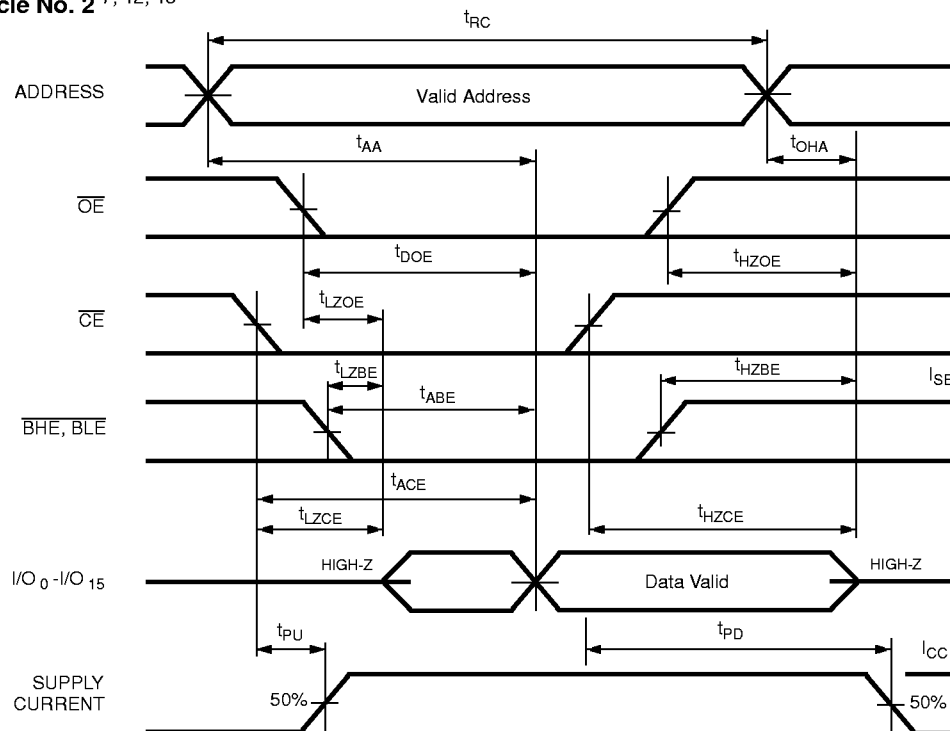
### Switching Waveforms

#### Read Cycle No. 1 7, 11, 14



9A104-5

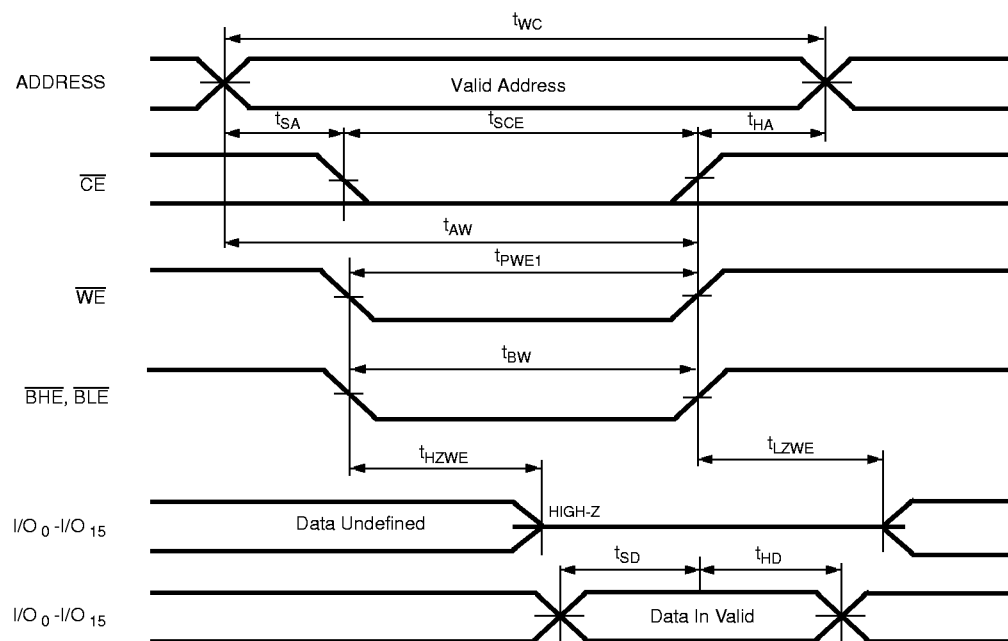
#### Read Cycle No. 2 7, 12, 13



9A104-6

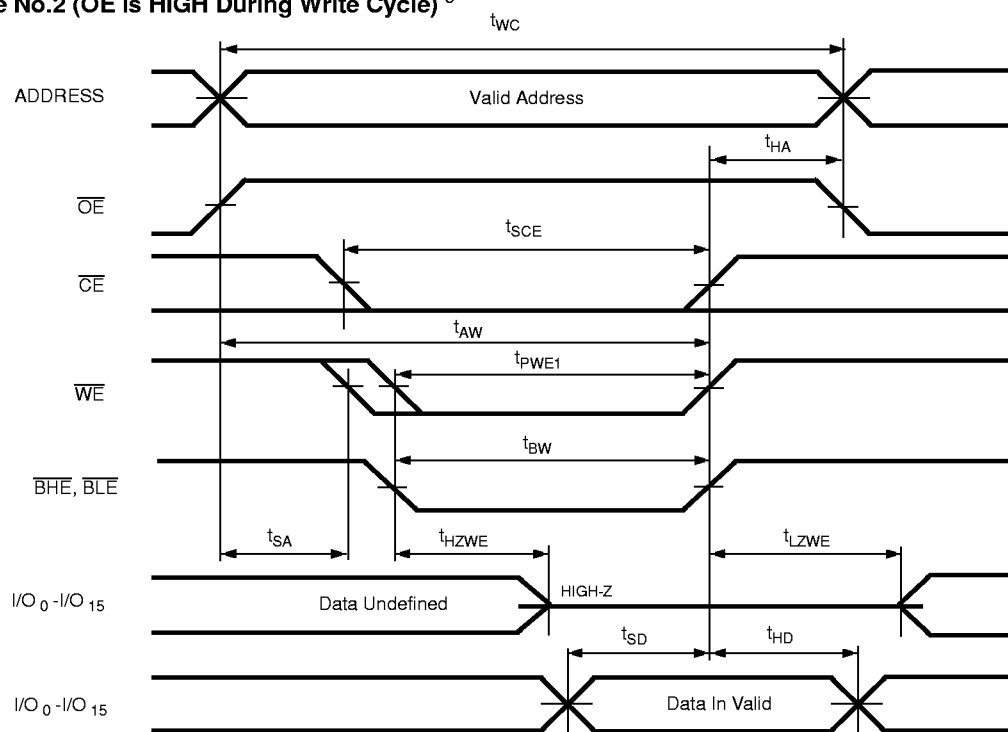
Switching Waveforms (continued)

Write Cycle No.1 ( $\overline{CE}$  controlled,  $\overline{OE}$  is HIGH or LOW) <sup>9</sup>



9A104-7

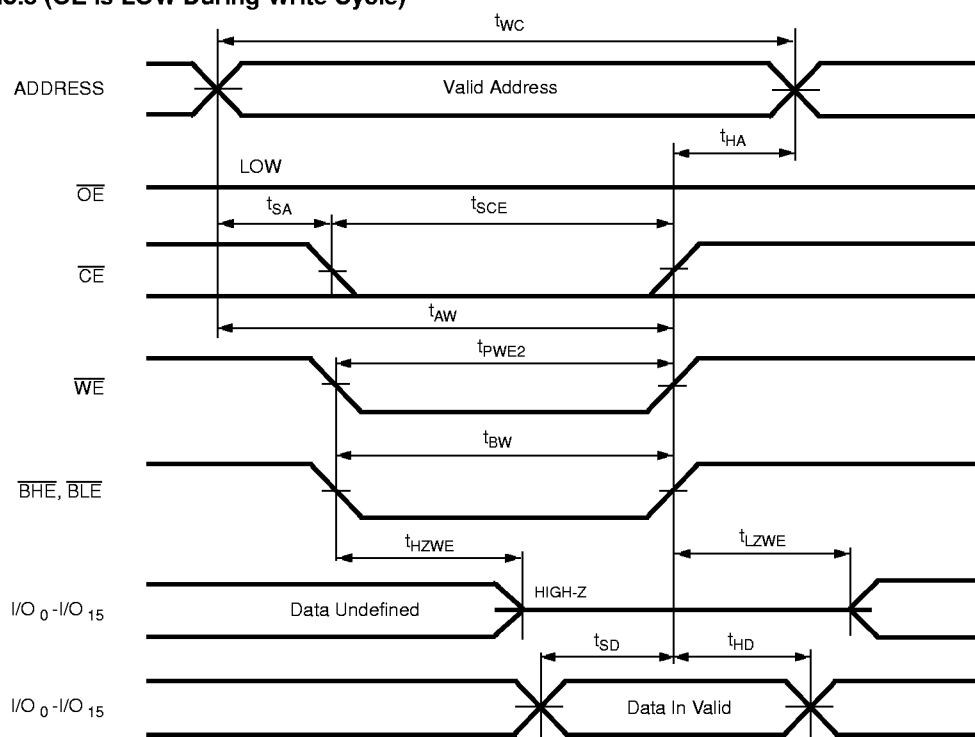
Write Cycle No.2 ( $\overline{OE}$  is HIGH During Write Cycle) <sup>9</sup>



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Switching Waveforms (continued)

Write Cycle No.3 ( $\overline{OE}$  is LOW During Write Cycle) <sup>9</sup>



9A104-9

**Truth Table**

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	I/O <sub>0</sub> - I/O <sub>7</sub>	I/O <sub>8</sub> - I/O <sub>15</sub>	Power
Standby	H	X	X	X	X	High-Z	High-Z	I <sub>SB1</sub> , I <sub>SB2</sub>
Low Byte Read (I/O <sub>0</sub> - I/O <sub>8</sub> )	L	L	H	L	H	D <sub>OUT</sub>	High-Z	I <sub>CC1</sub> , I <sub>CC2</sub>
High Byte Read (I/O <sub>9</sub> - I/O <sub>15</sub> )	L	L	H	H	L	High-Z	D <sub>OUT</sub>	I <sub>CC1</sub> , I <sub>CC2</sub>
Word Read (I/O <sub>0</sub> - I/O <sub>15</sub> )	L	L	H	L	L	D <sub>OUT</sub>	D <sub>OUT</sub>	I <sub>CC1</sub> , I <sub>CC2</sub>
Word Write (I/O <sub>0</sub> - I/O <sub>15</sub> )	L	X	L	L	L	D <sub>IN</sub>	D <sub>IN</sub>	I <sub>CC1</sub> , I <sub>CC2</sub>
Low Byte Write (I/O <sub>0</sub> - I/O <sub>8</sub> )	L	X	L	L	H	D <sub>IN</sub>	High-Z	I <sub>CC1</sub> , I <sub>CC2</sub>
High Byte Write (I/O <sub>9</sub> - I/O <sub>15</sub> )	L	X	L	H	L	High-Z	D <sub>IN</sub>	I <sub>CC1</sub> , I <sub>CC2</sub>
Output Disable	L	H	H	X	X	High-Z	High-Z	I <sub>CC1</sub> , I <sub>CC2</sub>
	L	X	X	H	H	High-Z	High-Z	I <sub>CC1</sub> , I <sub>CC2</sub>

**Ordering Information**<sup>10</sup>

Speed	Part Number	Package Name	Package Type	Temperature Range
10	AP9A104-10VC	V44.1	44-Pin Small Outline J-Bend	Commercial
	AP9A104-10TC	T44.1	44-Pin Thin Small Outline Package	Commercial
12	AP9A104-12VC	V44.1	44-Pin Small Outline J-Bend	Commercial
	AP9A104-12TC	T44.1	44-Pin Thin Small Outline Package	Commercial
15	AP9A104-15VC	V44.1	44-Pin Small Outline J-Bend	Commercial
	AP9A104-15TC	T44.1	44-Pin Thin Small Outline Package	Commercial
20	AP9A104-20VC	V44.1	44-Pin Small Outline J-Bend	Commercial
	AP9A104-20TC	T44.1	44-Pin Thin Small Outline Package	Commercial

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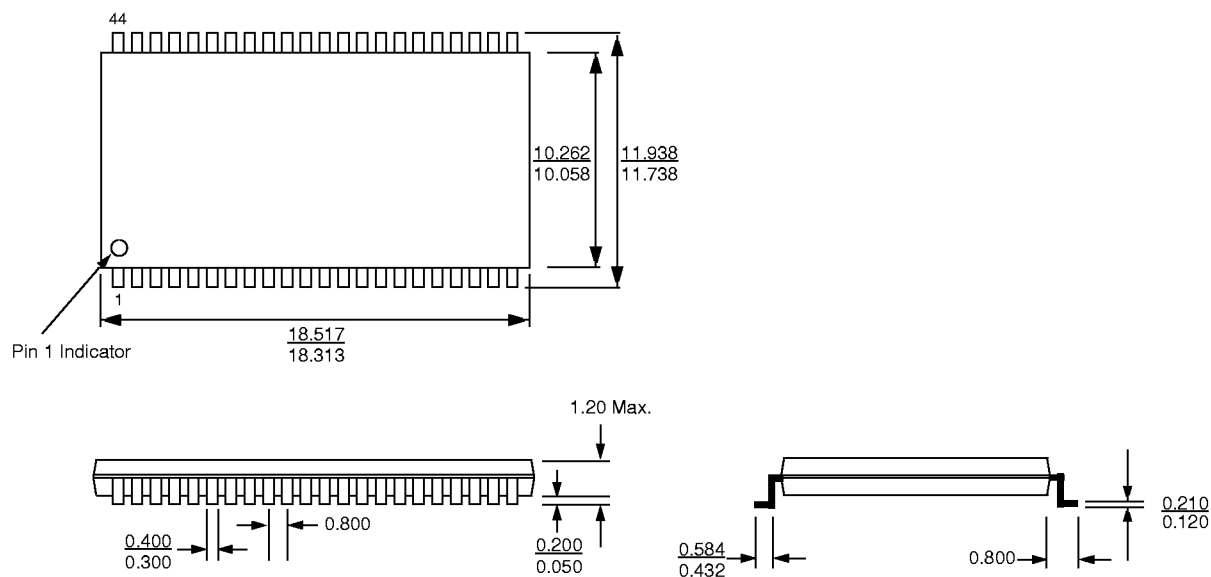
**Note:**

10. For information regarding additional temperature ranges, please contact factory.



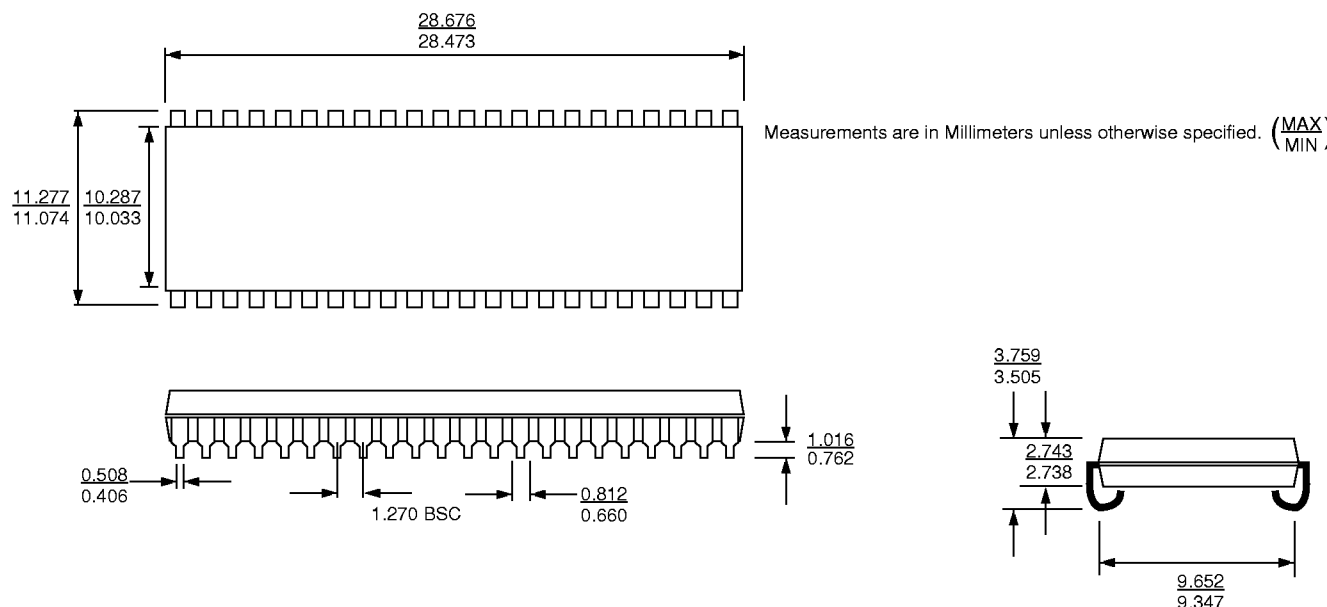
Package Diagrams

T44.1 - 44-Pin (400-Mil) Thin Small Outline Package (TSOP)



Measurements are in Millimeters unless otherwise specified. (MAX / MIN)

V44.1 - 44-Pin (400-Mil) Small Outline J-Bend (SOJ)



Measurements are in Millimeters unless otherwise specified. (MAX / MIN)